

Design, Simulation and FPGA Implementation of a Novel Router for Bulk Flow TCP in Optical IP Networks

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Abstract - Architecture of a novel optical router is designed in RTL and implemented in FPGA for the use of bulk flow TCP in optical IP networks. Various functional blocks of optical router like fabrication of flow from the incoming packets, processing the flow for routing process, contention resolution, buffering the packet or flow based on the wavelength and channel availability and transmission of the flow for destination have been successfully designed in RTL and implemented in FPGA. The numbers of slices utilized by various flow stages have also been simulated. The proposed optical router is tested for its performance in terms of frequency of operation and the area of utilization by various functional units. We have also implemented the central control unit for this optical router. From the observation it is found that in steady state, the optical router for bulk flow TCP exhibits better performance in terms of congestion behavior and wavelength aware flow to form a global optical network infrastructure.

Index Terms - Bulk flow TCP, contention resolution, Field Programmable Gate Arrays (FPGA), Optical packet switching (OPS), Time-To-Live (TTL), variable-sized packets, wavelength conversion, Optical router.

I. INTRODUCTION

Optical packet switching is an attractive technology for the integration of data and optical networking. The enormous bandwidth provided by the optical networking and the capability to switch packets directly at the optical layer make a powerful combination for the next-generation internet [1] where scalability, dexterity and performance are equally important. Bit-synchronous and fixed-size packet switching were investigated in-depth for optical-packet switching technologies in the earlier stage [2]. More recently, Internet protocol (IP)-over-optical has emerged as a novel concept that targets the seamless integration of data and optical networking. The accommodation of variable-length optical packets on all-optical packet switching routers allows IP packets on an all-optical network while avoiding the repeated packet segmentation and reassembly are seen commonly in

conventional routers. Asynchronous optical switching and variable-length packets in the optical domain gaining momentum in the recent past [3-5] are due to optical switching and variable-length packets in the optical domain gaining momentum in the recent past [3-5] are due to wider availability of bandwidth and minimized loss rate. It greatly simplifies the optical router system by eliminating the needs for flow synchronization and optical-electrical-optical (O/E/O) conversion. In addition, it reduces processing overhead and bandwidth loss due to the segmentation and assembly of variable-length packets at the optical router node. At the same time, it also poses new challenges for designing the optical router to support asynchronous, flow based switching process.

The analysis for heavy data transfer rate is of incredibly important to fulfill the ever increasing network traffic [6-8]. Data transmitting protocols like TCP/IP, UDP and asynchronous Transfer Mode (ATM) are considered for higher transmission rate. Among all the protocols, TCP plays major role in the higher data transfer rate. In order to get the higher data transfer rate, various parameters are to be concentrated. They are, channel capacity or bandwidth, number of nodes in the network, number of electro optical converters present in the network, data transfer rate in each node, various network components and some quality of Service (QoS) parameters. The corrupted flow, packet out of order, delay in arriving the packet at the destination which causes unnecessary retransmission of packets, small window regime etc., are some of the limitations to the electronic band width resources. In order to utilize the enormous bandwidth available in the optical domain, an all optical networks have to be developed. Many researchers [9] are working in this area for the efficient utilization of the optical bandwidth. The wider bandwidth available with the optical domain may optimally be utilized by a modification in the existing TCP structure such that the packets are assumed to have very limited time for processing in the router. The reported work [10] suggested that the packets can be consolidated as a flow and hence the size can be increased for flow and the time required for processing of flow in the router can be minimized to a larger extent. This technique has a uniform delay, very flexible and scalable routing and it also produces very good throughput and contention resolution [11]. A novel optical router capable of accepting and processing bulk flow TCP has to be designed and implemented which will receive the flow and performs the routing operation. The flow size in Bulk flow TCP in the proposed work is five to seven times larger than the conventional packet size to maintain the order of packets. The proposed router unit which has been designed such that the

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Bulk flow TCP of variable sized flows are accepted and routing/switching process took place with minimized processing time, eliminated segmentation and reassembly of Bulk flow TCP [12]. This also suggests solution in resolving contention which occurs when more than one flow tries to exit from same output port, wavelength and time [11].

The rest of the paper has been organized as follows: Section 2 deals about the proposed optical router architecture in detail. The implementation of optical router is presented in section 3. The simulation part is described in section 4. The performance study is presented in section 5. The results and discussions are presented in section 6. Conclusion with further scope on research is presented in section 7.

II. OPTICAL ROUTER FOR BULK FLOW TCP

The proposed optical router for bulk flow TCP is presented in Fig. 1. The architecture consist of the following units

- Fabrication Unit
- Flow Processing Unit
- Flow Transmission Unit and
- Buffering Unit

A. FLOW FABRICATION

This unit receives all incoming packets and the same has been forwarded to the processing unit with First in First out (FIFO) fashion. Once the packet is received by the input port of the router, it has been sent to the flow fabrication unit to fabricate the flow. The flow consists of source address, destination address, data length and the number of hops which the packet has to travel. This information is essential in-order to consolidate the packet as flow. The processing unit, after receiving all such information, it groups the similar packets by affixing the head and tail information. All packets are to wait in FIFO until the flow fabrication process is completed. The flows are fabricated based on the priority level. First priority is given for the packets which has common source and destination addresses, the second priority is for common source and destination router addresses and the least priority is given to common source and destination hops. The flow parameters like flow direction, end point aggregation, protocol layout and flow time period are considered with respect to unidirectional, double end point flows and network port etc. The length for flow is normally decided based on the delay tolerance level and the optimal utilization of the available bandwidth. Based on our earlier work [10], the flow size would be from 5 to 7 times greater than the normal packet size.

B. FLOW PROCESSING

The control unit or processing unit takes the complete responsibility of the transmission of the flow which consists of flow fabrication and flow transmission [13]. Flow processing is used to co-ordinate with all other modules. The total processing time (T_{Total}) for L number of packets in a Bulk flow TCP is written as [14]

$$T_{Total} = T_{base} + T_{group} + \sum_{S \in L} T_s \quad (1)$$

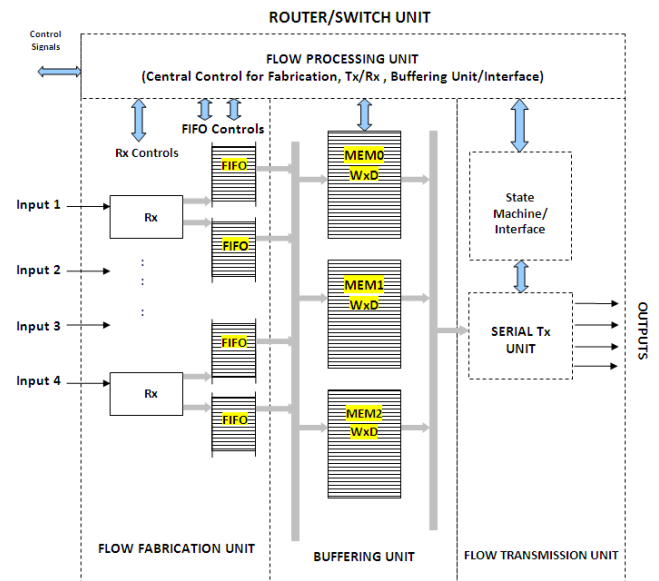


Fig.1. Architecture of Proposed Optical Router

where, T_{base} is the basic delay of the standard network router, T_{group} is the delay time that represents the packet to be grouped under same flow and T_s is the sum of processing time for each packet in a flow. The processing unit will look for various parameters like time, space and wavelength, in order to transmit the flow without any contention. Here, we have assumed that the router consists of four different ports with four wavelengths $\lambda_1, \lambda_2, \lambda_3$ and λ_4 . [15]

In response to the early flow discarding technique [16], the processing unit will try to send all the flows through the first channel and with the first frequency. If the previous channel exceeds its threshold value then the next channel is selected and this process continues until the existence of available free ports (here four) or available wavelengths ($\lambda_1, \lambda_2, \lambda_3$ and λ_4). The flows are forwarded to the buffering unit, if there is no availability of free port and wavelength in the router. In this way, flow control processing unit takes its utmost responsibility to fabricate, channelize, store and forward the flow from the initial stage to the final stage.

C. FLOW TRANSMISSION

Flow transmission or flow transmission algorithm is designed such that the router frequently updates the information with respect to other routers/switches in the network. This routing work frame will support different types of interior or exterior routing protocols. The routing table information is updated with the help of these routing protocols and forwarding table information is computed based on this routing table. The flow transmission takes place with a bitmap structure, control signals and forwarding table information. Once the information is loaded successfully, the processing will route the flow through the predefined port. The signaling system will support the protocols which help in routing and

forwarding the flow in the optical Bulk Flow TCP. The flow oriented routes are used by the quality of service (QoS) guaranteed applications and the flow are transmitted through the network for further processing. The control unit will receive signal from this transmission unit, checks its authenticity and availability of ports and wavelengths, then the required control signals for transmission is passed from the control unit to the transmission unit.

D. BUFFERING UNIT

The operation of fabrication, processing and routing requires a sequence of store and forward operation. The optical fibre line delay has to be simulated for this purpose at the input stage where the incoming packets are queued till the flow fabrication process is completed, then the flow has to wait until the desired port with wavelengths are available in the transmission unit. In the initial stage, a contiguous chunk of memory is allocated for this buffering. Out of this, half is allotted memory for transmission (Tx) process and half is allotted for receiving (Rx) process. A specific hardware with drivers is used to fix base and index values to access a particular flow.

The initial portion of memory is allocated for storing the address of packets or flow. Address or index is provided to retrieve the flow quickly from the location in the buffer. However the maintenance of index / address pool is a major task in the retrieving the flow from the buffer, it is also designed such that the receiver buffer allocation will not take place until the completion of send operation.

E. IMPLEMENTATION OF OPTICAL ROUTER

An optical router prototype on Xilinx XCV500E field programmable array (FPGA) can be implemented with four channels and four wavelengths by incorporating all the modules as mentioned in the previous section. The input unit has got four ports along with Ethernet Line Cards (LCs) capable of operating at the speed of 2.4 Gbps with multicast routing capacity. The LC helps in conversion, encoding, parallel to serial and optical to electrical conversions that are required for transmission through fiber.

The switches and router which are available in the commercial markets have complicated queuing mechanisms. In this work, a general purpose processor called Smart Port Cards (SPC) with field programmable port extenders are used for programming (FPXs). The Programmable Port Extender (FPX) is a hardware device which processes the incoming packets, examines and consolidates the flow between the switch back plane and the Ethernet Line Card. The proposed router consists of Network Interface Unit. The function of the NIU is to process and control how flows are routed through the modules and are implemented on a Xilinx vertex XCV 500 E FPGA devices. This comprises of four port input unit to transfer data, flow look-up tables (LUTs) on each port to route the flows in a programmed fashion. An on-chip processor fabricates, transmits and receives flow over the network and contention control mechanism.

The flow fabrication and processing took place in modular hardware components. These modules are implemented on the FPGA logic with reprogrammable capacity. An interface has been created which processes the streaming data in the packets as they are consolidated and interfaced with on-chip memory for buffering. Thus the Module has got complete control over buffering units.

The Optical router for Bulk Flow TCP with the implementation details as mentioned above are designed such that the focus is on the flow fabrication and the other factors which has already been reported [10]. The Pin diagram shown below in Fig. 3 incorporates all functionality as mentioned.

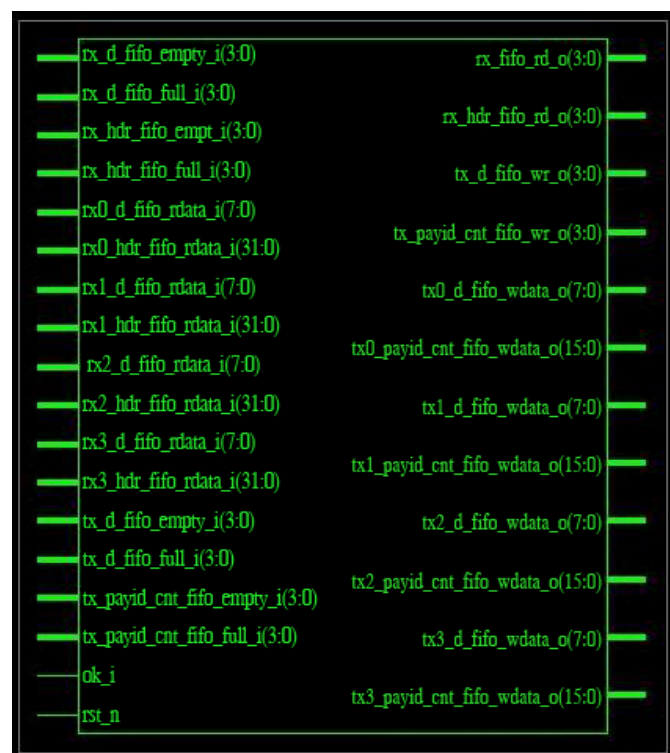


Fig.3. Pin Diagram for Optical Router Bulk Flow TCP

III. SIMULATION OF OPTICAL ROUTER FOR BULK FLOW TCP

A. FLOW FABRICATION

Register-Transfer Level (RTL) schematic is shown in Fig. 4 generates the bit stream which is suitable for the flow fabrication. It is shown that the changes made at the RTL level could make the difference as required. The corresponding control signals are mapped to the 4-LUT in Xilinx FPGA which is also convenient to have manual editing at FPGA editor. The LUT equation is appropriately changed such that the count value is modified according to the flow. The bit stream is generated by referring to the first bit stream and is loaded on the program control.

The fabricator simulates four channels with input/output fiber port, with each carrying four wavelength channels. The required number of flow processors, port managers and the

channel controllers are generated with the Xilinx ISE tool. This will receive the packets from the previous node or router and the same will be forwarded to the buffering unit with the necessary control signal information.

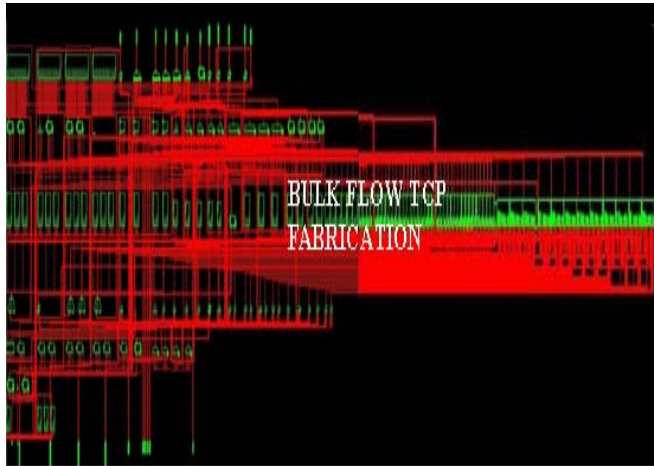


Fig.4. Bulk Flow TCP Fabricator RTL Schematic

B. FLOW PROCESSING

The schematic diagram is shown in Fig.5 describes the assessment of flow with respect to the Time (T), Space(S) and Wavelength(W) and hence the contention issues are carefully handled in this stage itself. The clock value is the deciding factor by which the flow processing takes place under this RTL.

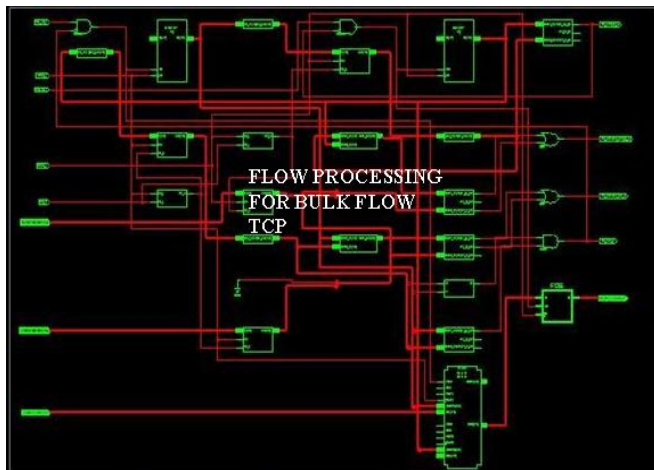


Fig.5. Bulk Flow TCP Flow Processor RTL Schematic

The proposed optical router has four number of ports as reported earlier in [10] near to the corresponding links, four different wavelengths for wavelength division multiplexing (WDM) and two local ports with a line speed of 2.5Gb/s to ingress local traffic and there is no packet loss at local ports which means egress edge router has a sufficient number of ports to accommodate local packet. For any specific localport, there is one dedicated traffic source to generate IP packets following a realistic IP packet length distribution.

C. FLOW TRANSMITTER

The simulation for this flow transmitter has been developed on Xilinx environment. This can be modified according to the different flow sizes and to identify the perfect match. The system is then executed through implementation of RTL and the components are to be matched with the objective routed to the specific channel as shown in Fig.6. The debugging is done successfully and the bit stream is downloaded into the FPGA for implementation.

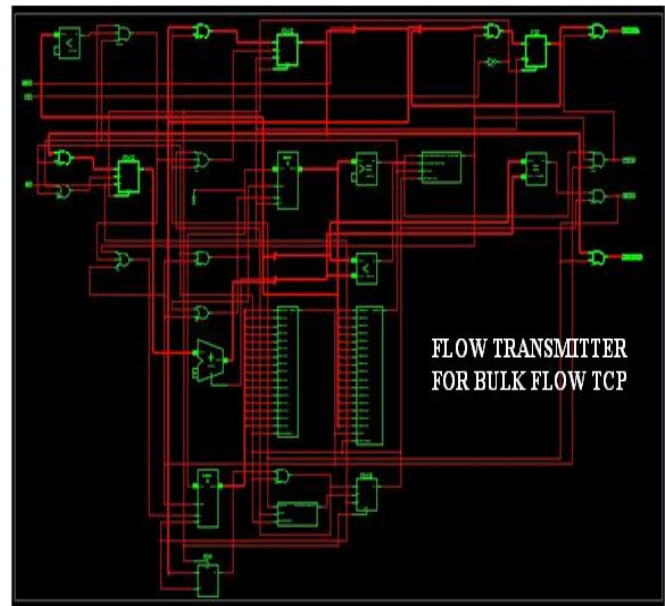


Fig.6. Bulk Flow TCP Transmitter RTL Schematic

The simulation looks for any free channel availability, if the channel is not available then the flow wavelength is converted into the freely available wavelength and the free channel is allocated for transmission. If there is no free wavelength or the channel then the flow is allowed to go through the buffering unit and the exponential time delay is allowed for the retransmission. Even after coming back from buffering unit if the flow could not find any channel of wavelength then the flow is ultimately discarded.

IV. PERFORMANCE OF OPTICAL ROUTER

A. PERFORMANCE OF FLOW FABRICATOR

Fabrication of flow as per bulk Flow TCP plays a vital role in the design of optical router. Table 1 shows the device utilization summary for the implementation of proposed optical Router on the Xilinx xcv500E FPGA chip. The number of slices occupied by the flow fabricator and the transmitter are shown separately in Table 1a and in 1b. The look up table (LUT) mappings for flow fabricator and the transmitter are almost in the same level. The Input / Output Blocks (IOB) have got a major responsibility of 226 numbers in flow fabricator whereas in flow transmitter it is just 114 numbers. A

single Global Clock Pin (GCLK) will serve for the purpose of flow fabrication.

Table1. Device Utilization Summary for Flow Fabricator

1.a. Flow Fabrication				1.b.Flow Transmission			
Logic Utilization	Used	Available	Utilization (%)	Logic Utilization	Used	Available	Utilization (%)
Number of Slices	230	6912	3%	Number of slice Register s	238	19200	1%
Number of slice Flip flops	175	13824	1%	Number of Slice LUTs	433	19200	2%
Number of 4 input LUTs	420	13824	3%	Number of Fully used LUT-FF pairs	237	434	54 %
Number of Bonded IOBs	226	316	71%	Number of Bonded IOBs	114	220	51 %
Number of GCLKs	1	4	25%	Number of BUFG/ BUFG CTRLs	1	32	3%

B. PERFORMANCE OF THE FLOW PROCESSOR

The device utilization summary shows the number of slices and flip flop used for processing the Flow. Nearly 79 LUTs are edited for the FIFO flow processing which can ensure faster functioning of the circuit. The flow processor performance depends nearly 50% on the global Clock.

Table2. Device utilization summary of the Flow Processor

Logic Utilization	Used	Available	Utilization (%)
Number of Slices	56	6912	0%
Number of slice Flip flops	56	13824	0%
Number of 4 input LUTs	79	13824	0%
Number of Bonded IOBs	33	316	10%
Number of GCLKs	2	4	50%

The flow fabricated in the first stage will undergo the processing under FIFO fashion. FPGA for processing or any other issue can be measured in terms of requirement to run the simulation and the area occupied.

C. PERFORMANCE OF FLOW TRANSMITTER

The processor used in this work is Xilinx xcv500E FPGA along with local memories. The simulation has been carried out for the study of performance of the flow transmitter unit of the optical router. The simulation will also study the behaviour of the optical router suitable for bulk flow TCP. The flow produced by this technique using HDL code is found to be equal or same as that of packets. However, modifications in the design in FPGA editor have greatly changed the performance of the router.

The major responsibility of the transmitter unit in the optical router is based on the 4-input LUT which is restricted to a maximum of 236 and the utilization is again based on the global clock. Out of the available LUTs and Flip Flops the 93 Flip Flops have been used for this flow transmitter [17]. This derives the concept of producing variable sized flows at a totally different bit file. The organization of LUT in the FPGA has been changed to a larger extent and this implicates at the RTL level. Thus the programmes configured in the LUTs will yield a better result.

Table3. Device Utilization Summary for Flow Transmitter

Logic Utilization	Used	Available	Utilization (%)
Number of Slices	132	6912	1%
Number of slice Flip Flops	93	13824	0%
Number of 4 input LUTs	236	13824	1%
Number of Bonded IOBs	45	316	14%
Number of GCLKs	1	4	25%

V. RESULTS AND DISCUSSIONS

A hardware optical router prototype is experimented on Xilinx XCV500E field programmable gate array (FPGA) by incorporating all the three stages as mentioned above with four channels and four wavelengths.

Fig.7 shows the frequency of operation with various units viz. flow fabrication, flow processing and flow transmission. Here, flow fabrication unit requires more frequency to do various operations such as receiving packet, consolidating a flow, ordering a flow, forwarding to processing or buffering unit etc. But for the case of processing unit, it requires less frequency to complete various operations viz. receiving flow from fabrication unit, looking for available port or wavelength, taking measures to resolve contention, forwarding the flow to the buffering unit or transmission unit etc. However the transmission unit requires less frequency of operation than the other two units.

Fig. 8 shows the area occupied by various stages of the optical router. Fabrication unit of the optical router requires more area or more number of flip flops. This is due to the fact that the frequency of operation of the flow fabrication unit is

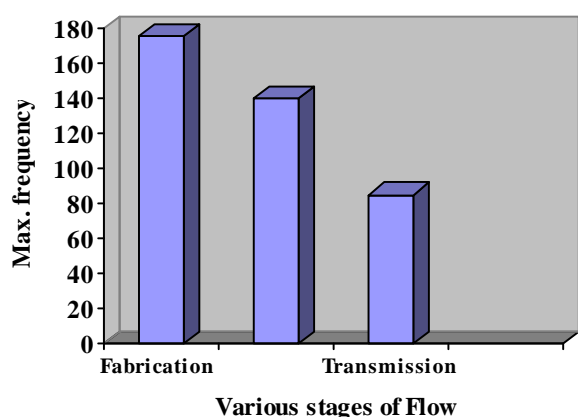


Fig. 7 Frequency of Operation with Various Stages of Flow.

than the other two units. Many numbers of operations are required for the optical router is initiated by the flow fabrication unit. In our case, the flow fabrication utilizes 486 slices. But in the case of flow processing and flow transmission units, they utilize 53 and 145 slices respectively.

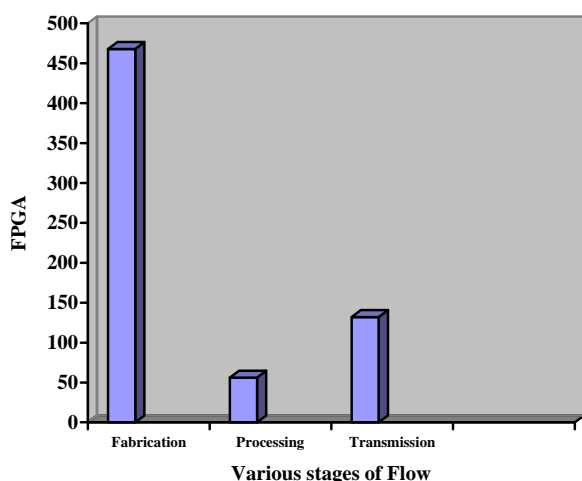


Fig.8 Area utilization of different stages of Optical Router.

The performance of the optical router controller is depicted in Fig.9. Due to major responsibility of flow fabrication unit, it takes more memory of the control unit. These responsibilities include signal generation, passing of control signal to all other units for processing, buffering and transmission. It occupies 65% of the control unit. But the processing unit and transmission unit take only 35% and 15% respectively. The responsibility of the processing unit is signal generation for buffering, channelizing, wavelength availability analysis and forwarding flow to the transmission unit. The transmission unit will control the activities on maintaining routing table information, forwarding information, transmission of flow etc.

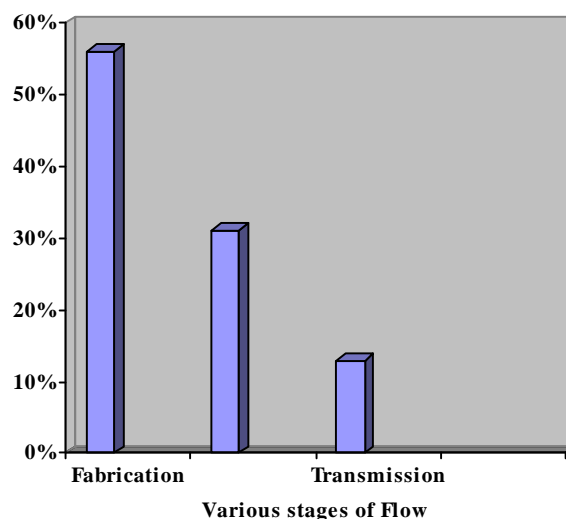


Fig. 9 Performance of Optical Router Controller.

VI.CONCLUSION AND FUTURE RESEARCH

Architecture, simulation and implementation of an optical router for the bulk flow TCP suited to optical IP networks were implemented. The optical router overhead and the performance for packet consolidation and the performance were studied experimentally. Various design stages of optical router viz. flow fabrication unit, flow processing unit and flow transmission units have been studied. The number of slices utilized for various flow stages have also been simulated in the FPGA environment. Frequencies of operations of various flow stages have also been studied. The performances of area utilization and optical control unit have also been tested. The design of RTL has been implemented in FPGA which has got the capability to resolve contention. This optical router will support a variable sized flow based TCP with better contention resolution to ensure excellent and fair wavelength aware flow. This work can further be carried out for all optical scenarios where O/E/O is not required.

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