Actively Tunable Lossless Floating Inductance Simulator Using Voltage Differencing Buffered Amplifiers

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***Abstract*— This work describes the topology for simulating the floating inductance simulator circuit based on employing voltage differencing buffered amplifiers (VDBAs) as new active components. The realized floating inductance simulator circuit uses two VDBAs and only one grounded capacitor. The synthetic circuit is resistorless and canonical structure as well as attractive for integration. The resulting equivalent inductance value of the proposed simulator can be adjusted electronically through the transconductance parameter of the VDBA. As illustrative application example, the proposed tunable floating inductance simulator is employed to realize the second-order *RLC* bandpass filter. Simulation results using standard 0.35-μm BiCMOS process model are included to verify the theoretical analysis.**

***Index Terms*— Voltage Differencing Buffered Amplifier (VDBA), voltage-mode circuit, floating inductance simulator**

I. Introduction

Floating inductance simulation circuit is one of the most important circuit elements widely used in many applications such as oscillator design, filter design and cancellation of parasitic elements. However, unfortunately, a large-valued physical inductor is not allowed to fabricate in the integrated circuit technology because of a large chip area and high-cost requirements. Although on chip spiral inductors with low quality factor (Q) can be performed to alleviate this restriction, their values are very small, usually in order of 1 nH. Accordingly, to overcome this problem, many actively simulated floating inductor circuits using various high-performance active devices have been reported in literature [1]-[10]. However, all of them need a large number of active and passive elements for their realizations.

Lately, the new active building block called voltage differencing buffered amplifier (VDBA) is introduced in [11], to provide the alternative possibility of electronically controllable voltage-mode analog signal processing circuits and solutions. Several applications based on using VDBAs as active elements in mainly analog signal processing have been developed [12]-[20]. This work presents an actively floating lossless inductance simulator topology using only two VDBAs and one grounded capacitor. The proposed synthetic floating inductor is electronically tunable through the transconductance gains of the VDBAs. The performance of the proposed floating simulator circuit is provided for illustrative example of the active *RLC* bandpass filter design. PSPICE simulation results with standard 0.35-μm BiCMOS process parameters are obtained to confirm the theory.

Manuscript received May 10, 2016; revised June 13, 2016.

This work was supported by Faculty of Engineering, Department of Electronic and Telecommunication Engineering, Rajamangala University of Technology Isan (RMUTI), Khon-kaen Campus.

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II. Description of the VDBA

As symbolically shown in Fig.1, the VDBA is a four-terminal versatile active building block, which consists of high-impedance voltage differencing input terminals p and n, high-impedance current output terminal z, and low-impedance output of voltage buffer noted as w. The terminal relations of the VDBA can be expressed by the following matrix equation :

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_w \end{bmatrix} \quad (1)$$

In (1), the parameter g_m refers to the transconductance gain of the VDBA, which normally is controlled by electronic means through the external supplied current or voltage.

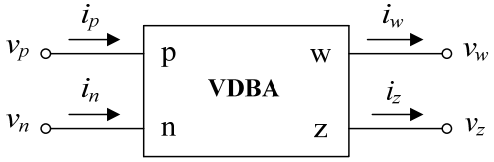

Fig. 1. Circuit representation of the VDBA.

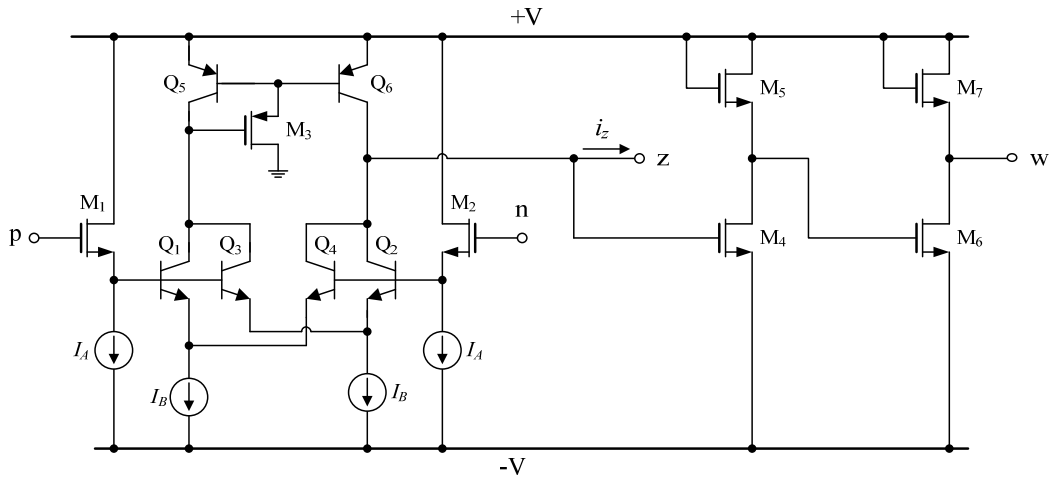

Fig.2 BiCMOS implementation of the VDBA.

Fig.2 shows the schematic BiCMOS realization of the VDBA [21], which mainly consists of the input stage consists of input transistors M_1-M_2, Q_1-Q_4, and current mirror transistors Q_5-Q_6, M_3. Transistors M_4-M_5 andM_6-M_7 represents the output stage, which constitute the terminal w. In this structure, the effective small-signal transconductance (g_m) can be derived as :

$$g_m = \frac{I_B}{2V_T} \tag{2}$$

where $V_T \cong$ 26 mV at 27°C is the thermal voltage. It may be easily visualized that the g_m-value is tunable linearly and electronically by an external DC bias current I_B.

Moreover, if we assume that the transistors M_4-M_7 are biased to operate in the active region. As a result, the small-signal voltage gain between v_w and v_z is approximated to :

$$\frac{v_w}{v_z} \cong \frac{g_4 g_6}{g_5 g_7} \tag{3}$$

where g_i denotes the conductance of transistor M_i (i = 4, 5, 6, 7). Also assume that $g_4 \cong g_5$ and $g_6 \cong g_7$, thus $v_w \cong v_z$ as expected.

III. Proposed Floating Inductance Simulator

Fig.3 shows the proposed floating inductance simulator circuit constructing only two VDBAs and one grounded capacitor without needing any external passive resistors. The synthetic inductor is, therefore, canonical number of active and passive components and also preferable for further integration point of view. Circuit analysis yields the input impedance for the proposed floating inductor in Fig.3 as :

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{sC_1}{g_{m1}g_{m2}} \tag{4}$$

where g_{mi} is the transconductance value of i-th VDBA (i = 1, 2). Thus, it can be realized that the circuit of Fig.3 simulates a floating inductor with an equivalent inductance (L_{eq}) :

$$L_{eq} = \frac{C_1}{g_{m1}g_{m2}} \tag{5}$$

It is clearly seen from (5) that the L_{eq}–value can be adjusted electronically by controlling the values of g_{m1} and/or g_{m2}.

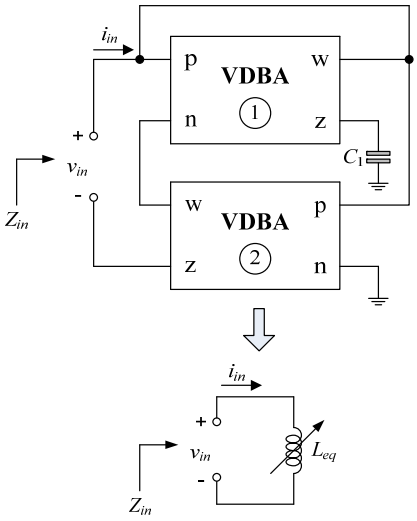

Fig. 3. Proposed lossless floating inductance simulator using VDBAs.

IV. Non-Ideal Effects of The VDBA

A. Non-Ideal Transfer Gain Effects

Considering the non-ideal transfer gains of the VDBA, the port relationship from (1) can be re-expressed by the following matrix equation :

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_w \end{bmatrix} \quad (6)$$

where α and β are the transconductance inaccuracy and the non-ideal voltage gain of the VDBA, respectively. The simulator of Fig.3 is re-analyzed using (6), and the non-idel input impedance function is modified to be :

$$Z_{in} = \frac{sC_1}{\alpha_1\alpha_2\beta_1\beta_2 g_{m1} g_{m2}} \quad (7)$$

Normalized various sensitivities of Z_{in} with respect to active and passive components calculated from (7) are given by :

$$S_{g_{m1}}^{Z_{in}} = S_{g_{m2}}^{Z_{in}} = -1 \quad (8)$$

$$S_{\alpha_1}^{Z_{in}} = S_{\alpha_2}^{Z_{in}} = S_{\beta_1}^{Z_{in}} = S_{\beta_2}^{Z_{in}} = -1 \quad (9)$$

and

$$S_{C_1}^{Z_{in}} = 1 \quad (10)$$

which are all no more than unity in absolute value. Therefore, it can be realized that the proposed inductor in Fig.3 exhibits low sensitivity performance.

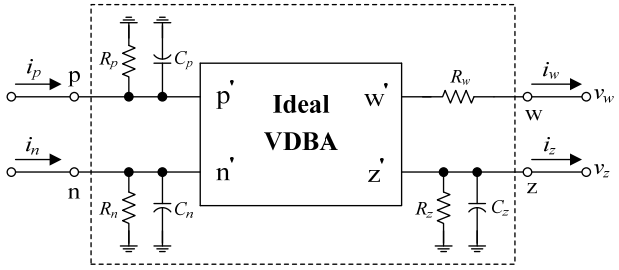

Fig. 4. Non-ideal model of the VDBA including its parasitic elements.

B. Parasitic Impedance Effects

The effects of various parasitic impedances of the VDBA used in the proposed inductor is taken into consideration. In practice, the behavior model of the VDBA consisting various non-ideal parasitic elements can be shown in Fig.4. Let R_p, R_n, R_z and R_w represent the parasitic resistances and C_p, C_n and C_z denote the parasitic capacitances of the corresponding terminals of the VDBA. The proposed inductor of Fig.3 is re-analyzed taking into consider the above parasitic effects. In this case, it can be seen that, at the terminal z of the VDBA1, the parasitic impedances R_z//C_z appearing in parallel with the external grounded capacitor C_1 bring an extra parasitic pole (ω_p) to the synthetic inductor circuit. Assuming $C_1 >> C_z$, the extra pole ω_p can be defined as :

$$\omega_p \cong \frac{1}{R_z C_1} \quad (11)$$

It should be noted from (11) that the high-frequency performance of the proposed floating inductor would be affected because of this parasitic pole. However, to prevent this effect, the following condition should satisfy such that :

$$\frac{1}{sC_1} << R_z \quad (12)$$

V. Performance Simulations and Discussions

To verify the theoretical prediction, the proposed circuit in Fig.3 was simulated with PSPICE program. To implement the VDBA device in the following simulation purpose, the BiCMOS technology structure depicted in Fig.2 has been employed using 0.35-μm BiCMOS technology [21]. Transistor aspect ratios (W/L in μm/μm) were set as : 14/0.7 and 28/0.7 for all NMOS and PMOS transistors respectively. The DC supply voltages and bias currents were respectively chosen as : +V = -V = 1 V and I_A = 25 μA.

The proposed floating inductor in Fig.3 was simulated with the following active and passive component values : C_1 = 10 nF and $g_m = g_{m1} = g_{m2} \cong$ 0.98 mA/V, 1.92 mA/V, 2.88 mA/V, ($I_B = I_{B1} = I_{B2} \cong$ 25 μA, 50 μA and 75 μA), which results in : L_{eq} = 12.3 mH, 2.7 mH and 1.2 mH, respectively. Fig.5 shows simulated time-domain responses for v_{in} and i_{in} of the input impedance of the proposed inductor. The results obtained from the simulation show that the current i_{in} lags the voltage v_{in} by 89°. Fig.6 shows the simulated frequency characteristics for the input impedance of the proposed inductor, which demonstrate that the useful frequency range is approximately from 10 kHz to 800 kHz.

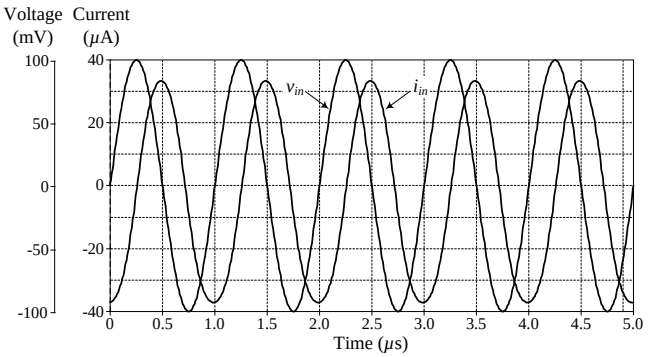

Fig. 5. Simulated time-domain responses for v_{in} and i_{in} of the proposed floating inductor of Fig.3.

VI. Application to Filter Realization

As an application example of the synthetic floating inductance simulator of Fig.3, it is applied in the RLC bandpass filter as shown in Fig.7. The L_{eq} is simulated with: C_1 = 10 nF and $g_m = g_{m1} = g_{m2} \cong$ 1.92 mA/V ($I_B = I_{B1} = I_{B2} \cong$ 50 μA), yielding $L_{eq} \cong$ 2.7 mH. Fig.8 shows the idea and simulated frequency responses of the bandpass filter in Fig.7, which appear that the simulated values are in good agreement with the ideal values. Furthermore, in order to demonstrate the electronic controllability of the proposed

floating inductor, the simulated gain responses of the bandpass filter in Fig.7 with tuning L_{eq}-value are shown in Fig.9. The value of L_{eq} in Fig.7 was respectively adjusted to 12.3 mH, 2.7 mH and 1.2 mH, by changing g_m = 0.98 mA/V, 1.92 mA/V, 2.88 mA/V (I_B = 25 μA, 50 μA and 75 μA). This adjusting leads to obtain the center frequency $f_c \cong$ 45.3 kHz, 96.7 kHz and 145.1 kHz, respectively.

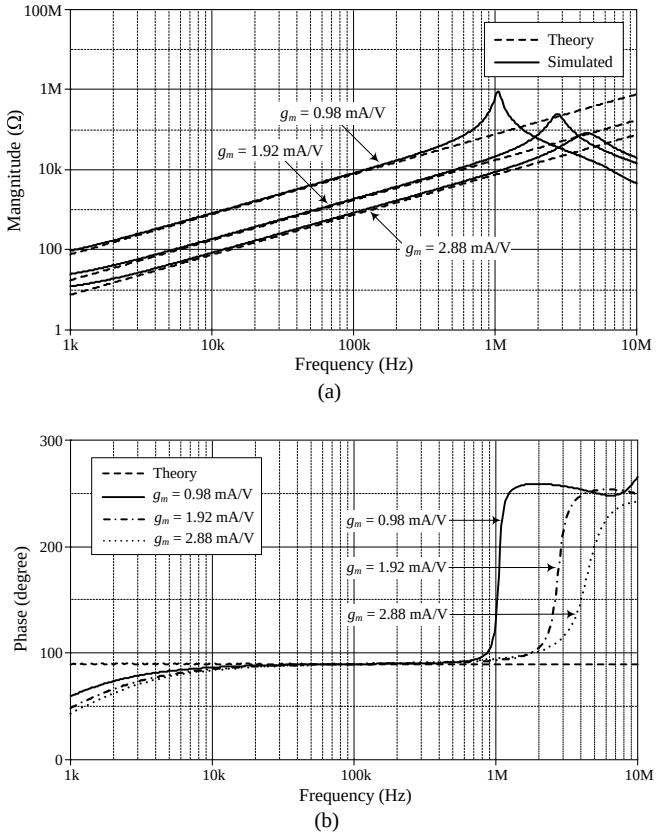

Fig. 6. Simulated frequency responses for Z_{in} of Fig.3 with various VDBA biasing currents.
(a) magnitude responses (b) phase responses.

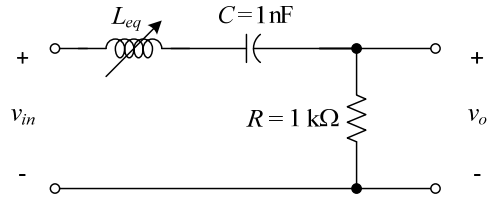

Fig. 7. RLC bandpass filter realized with the synthetic floating inductor of Fig.3.

VII. Conclusion

The synthetic lossless floating inductance simulator has been presented in this paper. The simulator contains only two VDBAs and one grounded capacitor, which is desired for further integrated circuit implementation. The equivalent inductance values can be adjusted electronically through the g_m-values of the VDBAs. The usefulness of the proposed circuit is demonstrated on the RLC bandpass filter design example. The workability of the proposed structure has been supported by PSPICE simulations using standard 0.35-μm BiCMOS technology.

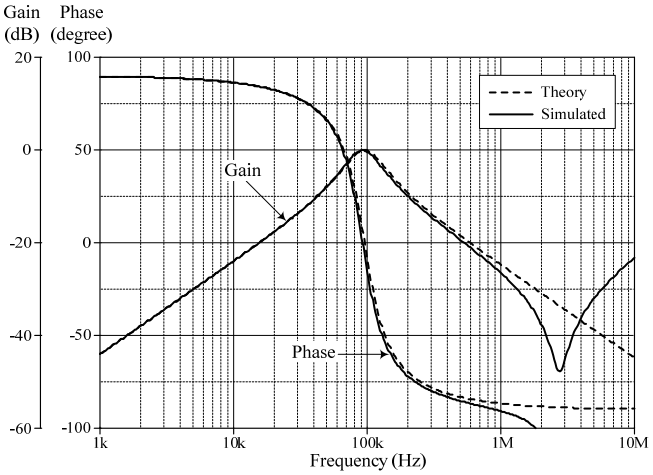

Fig. 8. Simulated frequency responses of the bandpass filter in Fig.7 at $f_c \cong$ 96.7 kHz.

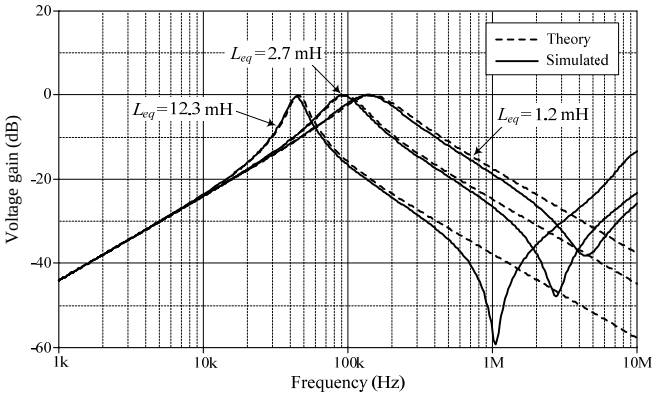

Fig. 9. Gain responses of Fig.7 with electronically variable L_{eq}.

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