The Performance of a Digital Sliding Mode Controller in Mitigating Beat Frequency Oscillation in Voltage Regulator Modules

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***Abstract*—With the prevalence of digital signal processors and computers performing at high sampling rate, controlling physical plants digitally such as switched-mode power supplies becomes a breakthrough from the classical analog control. Voltage regulator modules (VRMs) is a special class of power supplies that operate at non-standard voltage values, high load currents, and fast load transients. Sometimes, VRMs suffer from beat frequency oscillation (BFO), wherein the load transient frequency is almost equal to the switching frequency. BFO produces high magnitude and low-frequency oscillations detrimental to the operation of the VRM. In this work, the concept of designing and implementing a digital fixed-frequency sliding mode controller to mitigate the BFO in VRMs is studied and evaluated extensively. Since sliding mode controllers are focused on achieving the correct coefficient values in stabilizing a system plant, digital controllers become more advantageous than analog controllers. Extensive simulations show that the digital fixed-frequency sliding mode controller is able to mitigate the high magnitude and low-frequency effects to the VRM while maintaining voltage regulation with minimal ripple and equal sharing among various converter phases of the VRM.**

***Index Terms*—beat frequency oscillation, voltage regulator module, sliding mode control, fixed-frequency, load sharing.**

I. Introduction

VOLTAGE regulator modules (VRMs) comprise of multiple step-down (buck) power converters that are connected in parallel to achieve tighter regulated output voltage, to allow faster response times, and to supply a higher load current that is equally shared by the various converters of the module [1]. Equal load sharing has always been a characteristic or a target objective when power converters are placed in parallel. Parallel power supplies also offer modularity, redundancy, and stress reduction [2]. Moreover, VRMs have higher component density [3]. Unlike conventional paralleled power supplies, VRMs operate on non-standard supply voltage values and demand high-valued currents, e.g., 130–150 A with a switching frequency of 0.2–1.2 MHz [4].

While the VRM is experiencing high-frequency load transients, normally in the vicinity of the switching frequency, it must still maintain equal current sharing among its modules. However, during a high-frequency and periodic transient loading, there exists an unwanted phenomenon called the beat frequency oscillation (BFO), which is low in frequency and high in amplitude [5]. BFO is obtained by subtracting the load transient frequency from the converter's switching frequency [6]. BFO can also be introduced by paralleling DC-DC power converters with varying switching frequencies [7]. When BFO occurs, its amplitude normally surpasses the maximum allowable semiconductor devices ratings leading to irreparable damages.

Time-varying PWM sampler can produce beat frequency oscillation [5], [8]. When generating the necessary duty cycle, the control voltage (moving with the load frequency) intersects the ramp with the switching frequency, then regulates, according to the change in load, the output voltage. The load and switching frequencies both affect the duty cycle and output voltage, as evidenced from the inductor current. Therefore, the beat frequency goes back to the compensator due to the modulator.

With the rise of powerful and fast digital processors, designing and implementing parallel switch-mode power supplies become attractive and easy. Since the design of SMC focuses on determining the sliding coefficients, digital controllers become advantageous because the control is insensitive to environment and component changes. Digital controllers are also repeatable, predictable, and flexible. Additionally, there is a great reduction in the size of the developed power supply [9]. In this regard, digital SMC-based derived controllers will not contradict classical PWM controllers that follow linear control laws.

In this research work, we investigate the performance of digital fixed-frequency sliding mode controllers applied to switched-mode power supplies. Particularly, we tackle its effects on meeting the VRM specifications such as voltage regulation, current sharing, voltage ripple, and mitigation of the beat frequency oscillation (BFO) effects. The major contributions of this work are given below.

1) We derived and implemented the digital fixed-frequency sliding mode controller given the sensing states of voltage, current, and steady state errors of a two-phase voltage regulator module. The two-phase VRM can further be extended to n parallel buck converters. Digitization is achieved by utilizing the backward difference equation.
2) From the linear combination of the three sensing states to determine the sliding surface, the design process minimized the choice of controller gains into two. This reduction allows designers to have limited combinations when choosing controller gains.
3) The designed digital fixed-frequency sliding mode controller reduced the peak currents in each of the phases of the VRM to a value less than twice the current amplitude. We have also shown that the VRM's output

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voltage regulation, ripple, and current sharing capability are well within acceptable limits. More importantly, we reduced/eliminated the beat frequency oscillation phenomenon.

4) Tables of summary for choosing controller gains are presented to provide designers a look-up table detailing the effects when one controller gain is varied while the other one is constant.

The paper is outlined as follows: Section II presents a brief literature review on what has been done to voltage regulator modules employing the sliding mode control theory. Section III derives the switching control for a digital SMC using the backward equation. Section IV discusses the simulation results for various static and dynamic loading conditions. Finally, Section V concludes the research work and provides future research direction.

II. Review of Related Literature

Sliding mode control (SMC) is a non-linear controller intended for variable structure systems [10] such as switched-mode power supplies [11] and three-phase voltage source converters [12]. Compared to other traditional control methods such as Proportional-Integral-Derivative (PID) and lag-lead controllers, SMC guarantees stability and robustness in the presence of disturbances and changes in system parameter. The achievable response is independent from load variation and line changes. When compared to its non-linear controller counterparts, SMC is relatively easier to implement due to its high degree of flexibility. Because of the inherent variable structure of switched-mode power supplies (SMPS), SMC controllers are highly applicable to SMPS. Traditional controllers tend to linearize the model of the SMPS to small signal analysis, while neglecting to focus on large signal analysis. Though, there have already research studies that presented an improved controller through the combination of PID and SMC for non-linear applications. In [13], an improved PID-SMC controller has been designed to reduce the effects of external disturbances. In another study [14], the chattering in the output of a DC motor has been decreased by implementing a smooth function of the SMC.

Since most dynamic systems have high dimensions, linearization is done first to simplify the non-linear plant such as the switched-mode power supply [15], [16]. Linearization of these converters function at an ideal operating point only and fails when there are variations and disturbances to the load. A related study done by [17] compared the performance of classical control method against two non-linear control approaches. Proportional-Integral (PI) control was evaluated against fuzzy logic control and fixed-frequency sliding mode control. The classical PI control failed to deliver acceptable performance under load and line disturbances in contrast with the non-linear controllers. By substituting linear controllers with SMCs, there is a better performance against varying line and load disturbances, while achieving voltage regulation and load current delivery. However, despite the advantages of using SMC as a control method for DC-DC converters, it is rarely applied to DC-DC converters. One of the most obvious reasons is its infinite frequency requirement. This is needed to achieve zero steady-state error at the output voltage by following a sliding surface in the phase plane [18]. When a high and varying switching frequency is employed in a system, unwanted and degrading concerns become inevitable, e.g., unnecessary switching losses, inductor and transformer core losses, and electromagnetic interference (EMI) matters [19]. Aside from these issues, the input and output filter designs become dependent on the switching frequency. From the lowest frequency, the inductor and capacitor values are obtained and tend to produce sub-optimal designs [1].

A number of papers [20], [21], and [22] have been dedicated to the design and implementation of sliding mode control utilizing a fixed-frequency pulse-width modulation. In [20], the framework for the design equations of sliding mode controller applied to buck converter was laid. In [21], the authors extended the study to buck, boost, and buck-boost converters. For both [20] and [21] continuous conduction mode case was only considered. On the contrary, the discontinuous conduction mode was analyzed in [22]. For these three papers, the study was limited to voltage mode controlled converters and low output current modules.

The research field in the application of SMC to voltage regulator modules is still an open problem [23]. Few cases of research publication for VRM applications were reported and most especially one that is devoted to attenuating the problem of beat frequency oscillation. One of the earlier works that attempted to apply sliding mode control in VRM is that in [24]. It attempted to solve the start-up problem for VRMs and the output variation during high frequency transient. However, this did not address the problem of beat frequency oscillation. The work in [25] also applied sliding mode to a VRM but only focused on the static and low frequency transient conditions.

III. Derivation of the Sliding Mode Controller Gains

The specifications of a two-phase voltage regulator module and the derivation of the controller gains to be used in the digital fixed-frequency sliding mode controller from the analog SMC counterpart are adopted from [4].

A. Two-phase Voltage Regulator Module Specifications

The voltage regulator module (VRM) is composed of two buck (step-down) converters connected in parallel. Each converter can take 12V in its input and can provide a regulated output voltage of 1.5V. It can also supply a current range of 1–80 A at a regulated output voltage swing range of 1.47525–1.52475 V. The switching frequency is set to 300 kHz. The dynamic load conditions change from full-load to half-load then to no-load scenarios (1A load). The frequency at which the dynamic load changes should be close to the converter's switching frequency to investigate the beat frequency phenomenon. Current sharing between modules is achieved by the average method technique.

B. Derivation of the Analog and Digital Sliding Mode Coefficients

We consider three state variables to monitor the performance of the VRM, namely: 1) current error s_1, 2) voltage error s_2, and 3) steady-state error s_3. We note that other state variables can be controlled, e.g., derivatives of voltage states. The more state variables to monitor, the better the

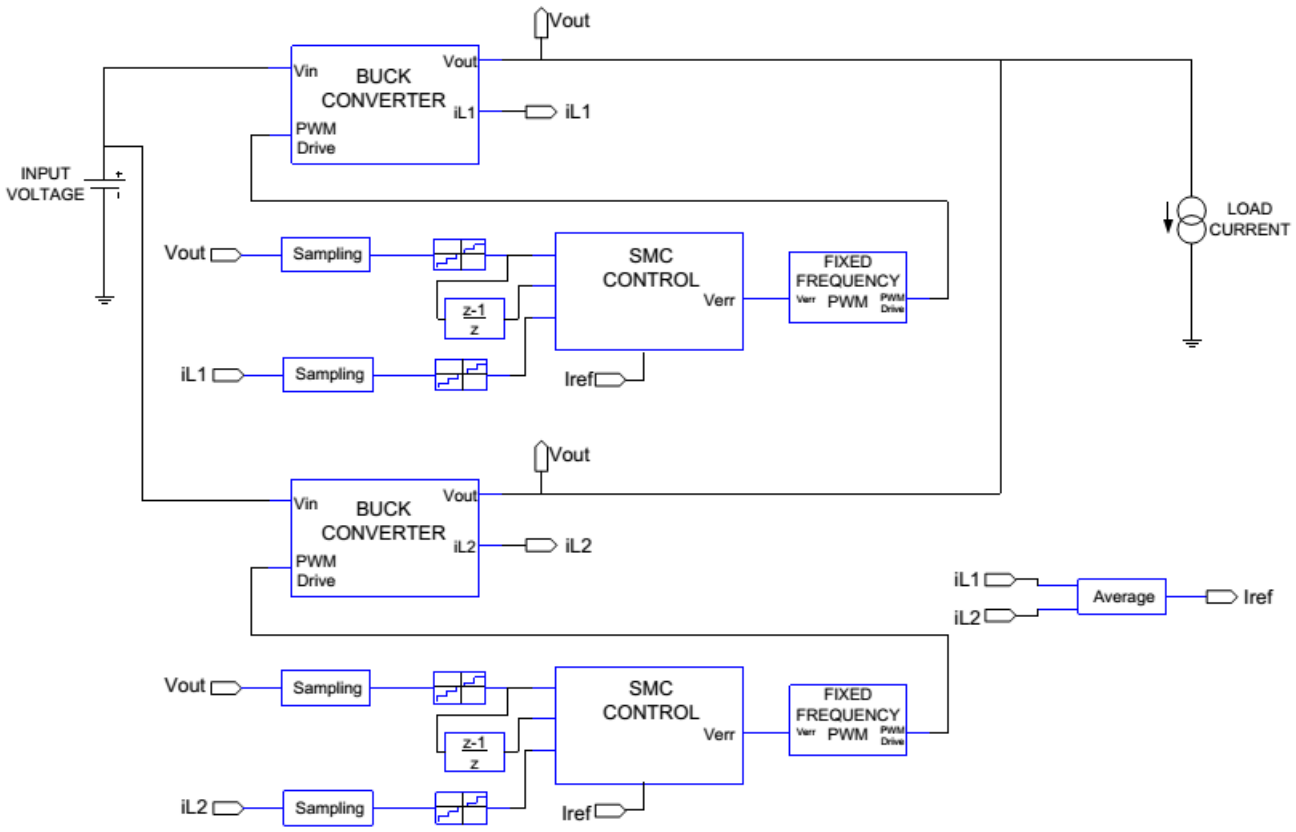

Fig. 1. Control Simulation Blocks for a Digital Sliding Mode Controller for a Two-phase VRM.

VRM performance, but comes at a more complex controller design.

The current error s_1 in (1) checks if there is equal current load sharing, i_L, among the phases of the VRM, given the reference current, i_{ref}. i_L is the averaged inductor current of the VRM. The voltage error s_2 in (2) ensures that at any load conditions, the output voltage, V_{out}, is tightly regulated with the target value V_{ref}. Finally, s_3 in (3) is introduced to monitor the steady-state current and voltage errors because the SMC is operating on a fixed-frequency implementation.

$$s_1 = i_{ref} - \alpha_1 i_L \tag{1}$$

$$s_2 = V_{ref} - \alpha_2 V_{out} \tag{2}$$

$$s_3 = \int \left(i_{ref} - \alpha_1 i_L\right) dt + \int \left(V_{ref} - \alpha_2 V_{out}\right) dt \tag{3}$$

In [1] and [4], the derived switching control for the analog SMC, u is given in (4).

$$\begin{aligned} u = & \frac{V_{out}}{V_{in}} - \frac{K_1 i_C}{\delta V_{in}} \\ & + \frac{K_2}{\delta V_{in}} \left[\left(i_{ref} - \delta i_L \right) + \left(V_{ref} - \beta V_{out} \right) \right] \end{aligned} \tag{4}$$

where $K_1 = \frac{\alpha_1 \beta L}{\alpha_2 C}$ and $K_2 = \frac{\alpha_3 L}{\alpha_1}$. α_n's are the sliding coefficients while β and δ are sensing gains. At steady-state, the SMC switching control u is equal to the that of the linear controller, where $u = \frac{V_{out}}{V_{in}}$.

In (4), the capacitor current is expressed as $i_C = C\frac{dV_C}{dt}$ to avoid additional sensing requirements. It is discretized by using the backward difference equation as seen in (5).

$$i_C(k) = \frac{C}{T_S}\left[V_{out}(k) - V_{out}(k-1)\right] \tag{5}$$

where $V_{out}(k)$ and $V_{out}(k-1)$ are the output voltages at discrete times k and $k-1$, respectively. T_S is the sampling period.

Therefore, the digital SMC employing the Direct Z-transformation is given in (6), where T_S is the sampling period.

$$\begin{aligned} u(z) = & \frac{V_{out}(z)}{V_{in}(z)} - \frac{K_1 C}{\delta T_S V_{in}(z)}\left[V_{out}(z) - z^{-1}V_{out}(z)\right] \\ & + \frac{K_2}{\delta V_{in}(z)}\left[\left(i_{ref}(z) - \delta i_L(z)\right)\right] \\ & + \frac{K_2}{\delta V_{in}(z)}\left[\left(V_{ref}(z) - \beta V_{out}(z)\right)\right] \end{aligned} \tag{6}$$

(6) is implemented in Fig. 1 in the 'SMC CONTROL' block. It is noted that in digital SMC, the gains are varied in the implementation. This is shown in Fig. 2 highlighted by the solid rectangle. The sampling of the capacitor current in (5) is implemented by the dotted rectangle.

An important consideration in the digital implementation is the sampling rate. As per Nyquist theorem, the minimum sampling frequency should be twice the highest signal frequency. However, practical hardware limitations do not allow the sampling to be too high. As a work around, the sampling must be synchronized with the PWM pulse. When the sampling is synchronized, what is really sampled is the average of the signal. This will be sufficient for the

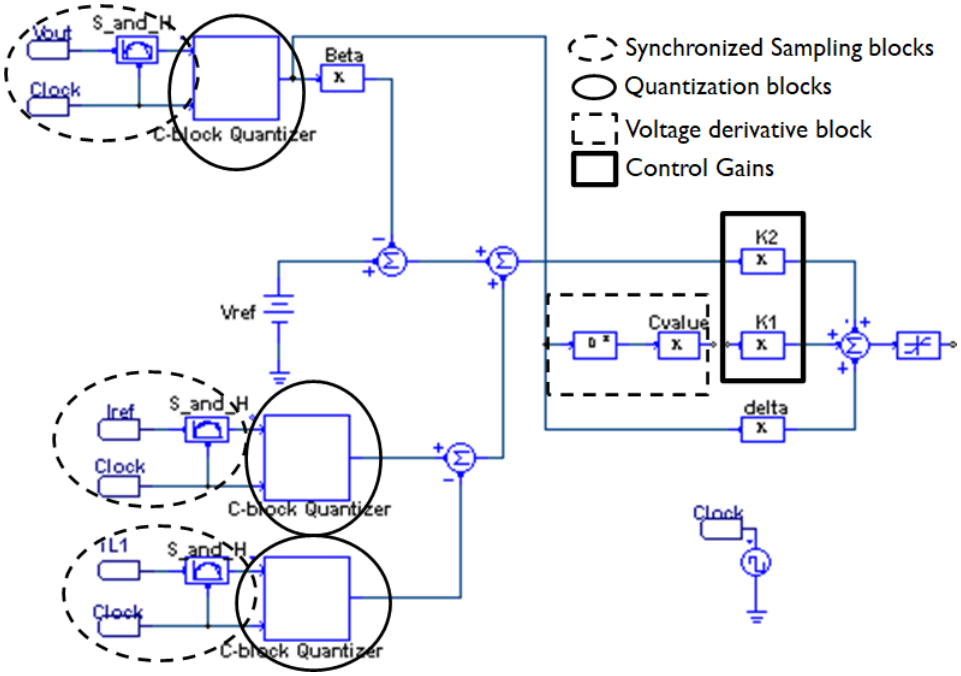

Fig. 2. Inside the siding mode controller block (SMC CONTROL).

reconstruction of the signal. Synchronization, as shown in Fig. 3 shown by the dotted circle, is carried out by using phase delay, ϕ (computed in (7)), where the middle of the ON time is used as the delay point of the control, thus, nullifying the effect of aliasing. A sampling block with synchronization trigger is used to allow for synchronized PWM and sampling.

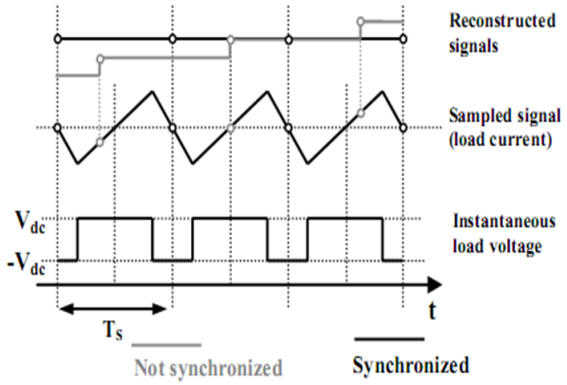

Fig. 3. Synchronization of the sampling with the PWM pulse.

$$\phi = \frac{\frac{Duty_{CCM}}{100\%} \times 360}{2} \tag{7}$$

where $Duty_{CCM}$ is the duty cycle of the VRM at continuous conduction mode expressed in percentage.

Choosing the sampling frequency prevents aliasing in the reconstructed signal from the sampled signal and assures regulated output and equal current sharing. Several experiments have been conducted by varying the sampling frequency to a minimum of twice the switching frequency but these did not yield the desired performance of the VRM. However, when the sampling frequency was synchronized with the 300 kHz switching frequency, the VRM worked properly. Intuitively, the reader might say that the Sampling Theorem is violated with synchronized sampling. In practical applications, however, hardware limitations do not allow the sampling frequency to be too high. Since the duty cycle is allowed for a double update on the PWM, the sampling frequency cannot be higher than twice the switching frequency. The solution then is to synchronize the sampling with the switching frequency.

After the synchronous sampling, the effect of quantization is next considered. In this study, any signal is quantized to 10 bits. Although the PSIM simulation engine has a quantizer block, it does not have the option to work in conjunction with the Sampling Block with synchronization trigger, therefore, a separate C-block has been created to emulate the quantizer block since synchronized trigger is needed. This is shown by the solid circle.

To achieve stability, the constants K_1 and K_2 (solid rectangle) are chosen by following the conditions set in (8), which are derived from (6) using the Routh-Hurwitz criterion. L, C, and r_L are circuit parameters of the buck converter.

$$\begin{aligned} K_2 \frac{\delta + \beta r_L}{\delta L C r_L} &> 0 \\ K_1 &> -\frac{\delta L}{r_L} - \delta K_2 \end{aligned} \tag{8}$$

It is noted that choosing K_2 comes first before picking a K_1 value. K_2 is always positive, while K_1 is always negative. Compared with the analog implementation [4], the range of control gain values for K_1 and K_2 are smaller because the sampling process reduced the usable gain of values for the digital implementation.

IV. Extensive Simulation Results and Discussion

In this section, we present results gathered from extensive simulations performed in PSIM. Since the control gains in (8) present a wide range of possible control values, control gain

iterations have been done to achieve the desired performance of the VRM and determine the effects when the controller gains are increased or decreased. The VRM is also subjected to various static and dynamic loading conditions.

A. Static Loading Conditions

Fig. 4 shows the regulation at various loading conditions, i.e., 10%, 50%, and 100% load. It is noticeable that for various values of K_1, the output voltage regulation stays constant for increasing K_2 values. Incrementing the value of control gain K_2 leads to a higher value of regulation. However, with the $\pm 1.65\%$ band in consideration, the output voltage regulation fails to meet the criteria for regulation. Ideally, the output voltage is 1.5V nominal for all loading conditions. Several factors attribute to the high regulating point of the output voltage during this load condition. First, for the given load current, the inductor value is rather small, thus, it cannot hold out much energy and instead delivers it immediately to the load side.

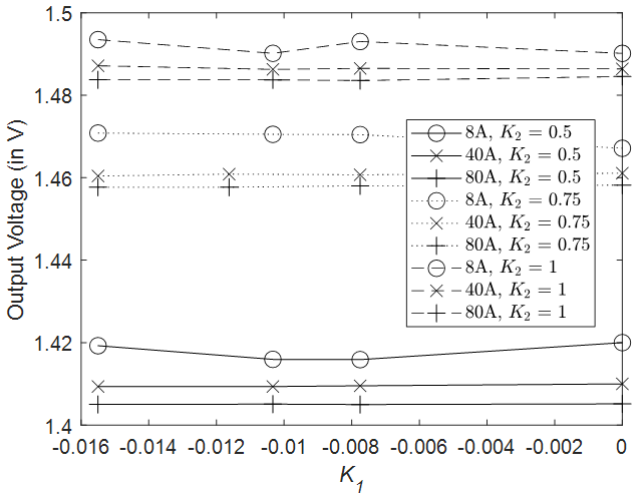

Fig. 4. VRM Output Voltage for varying control gain K1 at 8A, 40A, and 80A loading conditions.

Another factor is that the power section design was intended for continuous conduction mode (CCM) operation where duty cycle is a function of input and output voltages and independent of inductance. Generally, CCM is achieved after a certain minimum load. However, below this minimum load, the converter operates in discontinuous conduction mode (DCM). During DCM, the duty cycle is affected by the inductance value; thus this is an entirely different plant from CCM.

Fig. 5 shows the output voltage regulation at half load condition. Results show that the output voltage, $Vout_{sense}$, became lower in its regulation but still within the pre-defined voltage specifications. The inductor currents, i_1 and i_2, are also tracking each other during this condition.

On the other hand, Fig. 6 illustrates what happens when the designed control gains are exceeded. Even though the output voltage, $Vout_{sense}$, is regulated, overshoots and oscillations are visible in its amplitude.

We next investigate the output voltage ripple as illustrated in Fig. 7. For the three loading conditions under study, the output ripple voltage of the two-phase VRM satisfies the 15

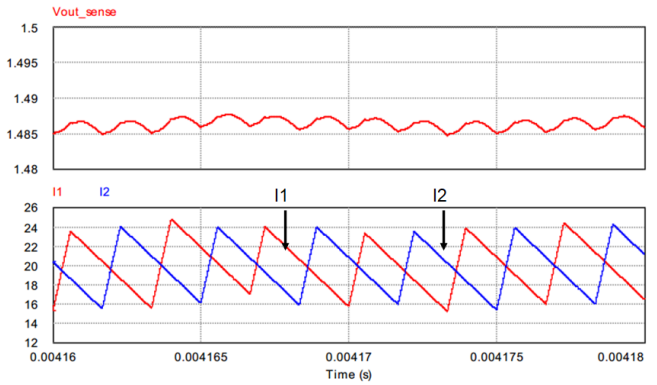

Fig. 5. Operation of VRM at 40A load with K_2=1 and K_1=–0.0.1033.

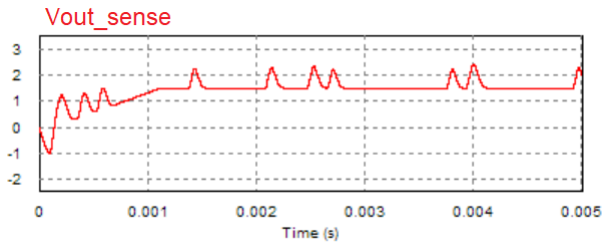

Fig. 6. Operation of VRM at 40A load with $K_2 > 1$ and K_1=–0.0.1033. Oscillations and peaking become quite visible.

mV pk-pk limit and is even lower than the required output voltage ripple. During full load condition, a constant K_2 and decreasing K_1 values reduce the output voltage ripple. This observation is the same when there is 50% load.

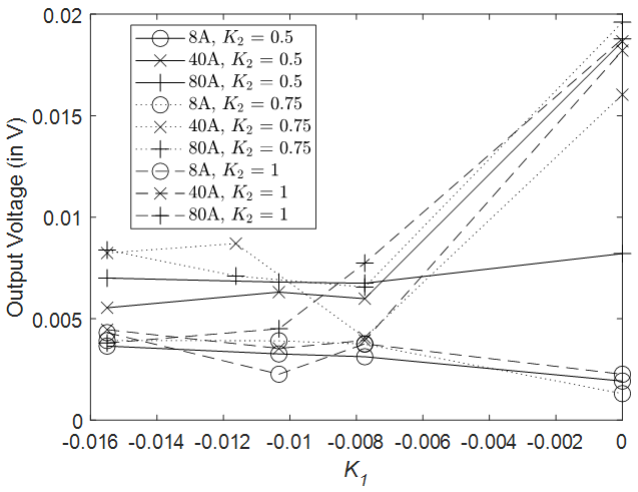

Fig. 7. Output Voltage Ripple for Different Control Gains at Various Loading Condition

The current sharing accuracy is one requirement to determine the efficacy of the control particularly during both static and high frequency transient loading. As with the analog control, a maximum error of five percent (5%) is defined as the maximum limit. Again, the same loading conditions apply to the current sharing accuracy test. The current sharing error is determined in (9).

$$\%CS_{error} = \left| 1 - \frac{I_{o1}}{\frac{I_{Total}}{n}} \right| \times 100\% \tag{9}$$

where I_{o1} is the converter's output current, I_{Total} is the total load current, and n is the number of phases in the VRM.

Fig. 8 shows the VRM current sharing accuracy with Digital SMC for half and full loads. It is seen that the error percentages with K_2 and K_1 have an erratic pattern and no trend is clear as to what values of the control gains result in high and low error. A general observation is that even with this erratic behavior the current sharing error for the digital SMC meets the 5% requirement.

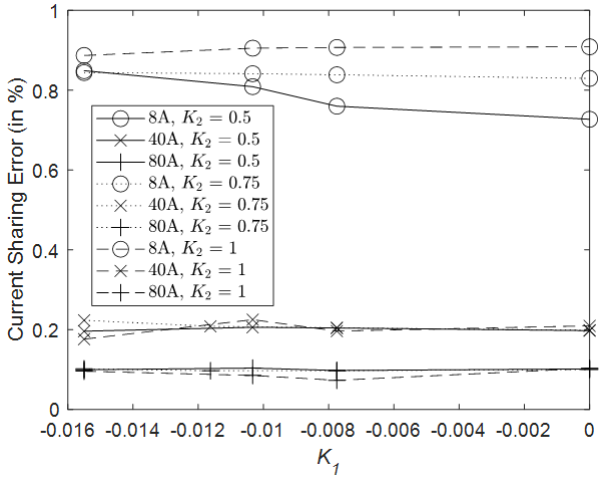

Fig. 8. Current sharing error for varying control gain K_1 at at 8A, 40A, and 80A loading conditions.

The current sharing capability of the VRM employing the sliding mode controller is evidenced by Fig. 9. As can be seen, the inductor currents (I1 and I2) are equally shared and the output voltage is well-regulated. Despite the acceptable performance for current sharing, our extensive simulation experiments would suggest that the current sharing error cannot entirely be used to observe the effects of varying the control gains but by the other parameters.

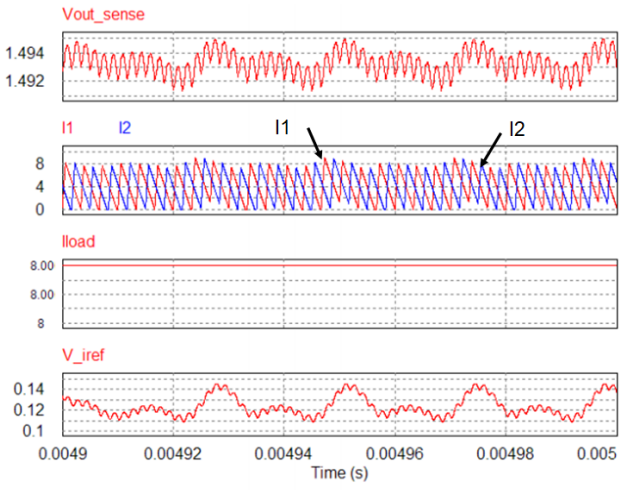

Fig. 9. Operation of the VRM at 8A load with K_2=1 and K_1=–0.01033.

B. Dynamic Loading Conditions

The performance of the digital sliding mode control during transient loading conditions has also been tested. Step load tests are done on the converter and the overshoot and the undershoot voltage of the converters are observed. Fig.10 shows the transient response for varying K_1 while K_2 is held constant. It is seen that for the lower load to the higher load transition (1–41A and 40–80A load), the trend shows an increase in the undershoot voltage with an increase in K_1. This trend is observed as well in decreasing load from 80–40A. The trend line for 41–1A loading condition also shows an increasing magnitude of the undershoot except when the value of K_1 is set to zero. The output voltage transient ripple (overshoot and undershoot) for the three chosen control gains shows that the digital implementation has higher ripple when compared with its analog counterpart.

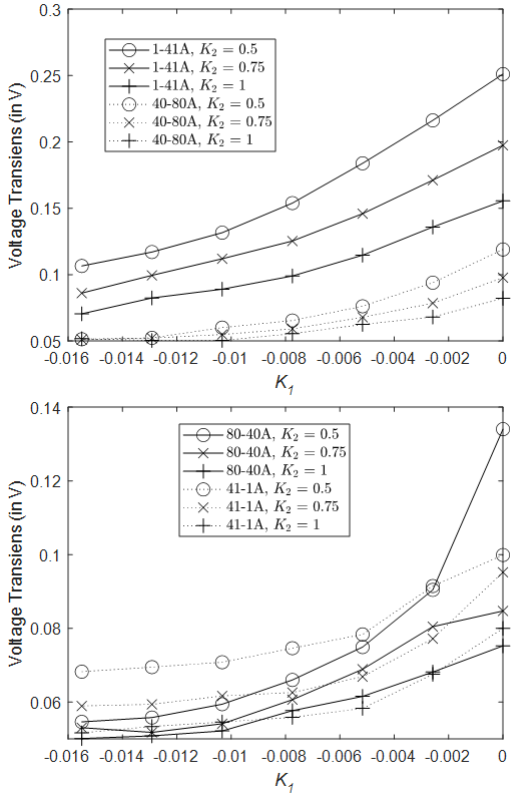

Fig. 10. Transient response for varying K_1 when K_2 is constant at values equal to 0.5, 0.75, and 1.

The dynamic test results and dynamic loading conditions are illustrated in Fig. 11. During stable operation, the undershoot is seen to reach 1.42 V while the overshoot has peaked at 1.54 V. Note that the output voltage ripple is minimal, and the desired output voltage is regulated. These observations are valid for all the load cases except when the load transition becomes 41 A to 1 A. When the load experiences a dynamic condition of 41-1A, the VRM output voltage has gone out of regulation once it is stepped to 1A. During this transition, the buck converter transfer function has traversed from continuous conduction mode (CCM) to discontinuous conduction mode (DCM). This causes the output voltage to go to a higher value. From the middle graph, we can examine that the inductor currents are equal (because they are superimposed), thus, effectively sharing the load equally.

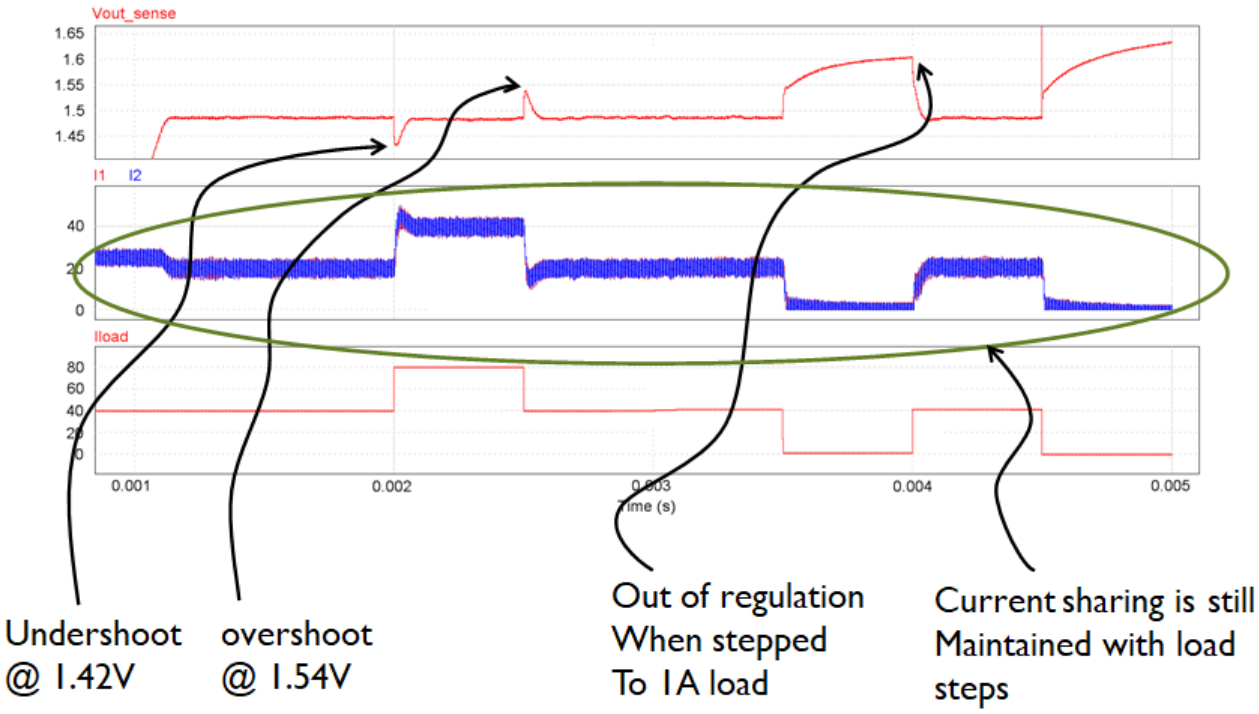

Fig. 11. Dynamic loading conditions when K_2 = 1 and K_1 = –0.01033. (Note that currents I1 and I2 have the same response, i.e., equal current sharing.)

C. Beat Frequency Oscillation

Finally, the performance of the digital fixed-frequency sliding mode controller during high frequency transient loading is observed. The two-phase VRM is loaded from half load up to full load with a frequency near the switching frequency of the converter. Tables I–III show the beat frequency data when the load frequency is varied from 290–310 kHz loading.

It is seen that for all three transient loading frequencies, there is no manifestation of beat frequency oscillation. This claim is further supported by the Fig. 12. It shows the high frequency transient loading behavior of the VRM. The load current, 'Iload', is going from half load to full load with a frequency of 290 kHz. The output voltage, $Vout_{sense}$, is within the regulation band. Taking a closer look at the inductor currents, it can be seen that there is no visible low frequency oscillation and the amplitude also does not show high peak currents, which happens when there is an outright imbalance in the load sharing. What can be seen instead is the equal load sharing of the inductor currents.

Unlike the analog control in [4], it is observed in the digital sliding mode control, the presence of cycle skip and double pulsing are no longer visible in the converter. The gate drive pulses show a consistent train of pulses, in turn, allowing the inductor currents to alternately deliver the needed load current. The frequency of the converter has also maintained its value as opposed to its analog counterpart where the frequency of the converter was halved to react to the high frequency transient loading.

Due to the sampling process inherent to the digital sliding mode control, the high frequency load transient appears as a normal perturbation to the plant. Since there is only one sampling instance as presented to the plant, the high frequency transient is then seen as average instances and not as instantaneous in nature. In contrast, for the analog sliding mode control, the perturbation is tracked continuously, and the control must react to every error instance that it sees in the plant.

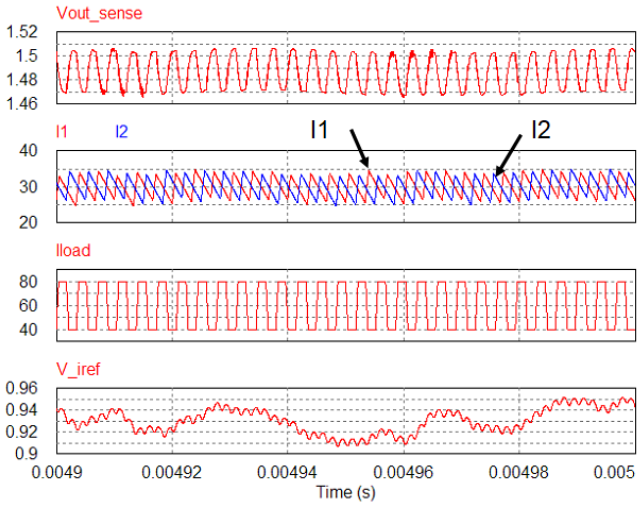

Fig. 12. High Frequency Transient (290kHz) Loading Condition K_2 = 1 and K_1 = –0.01033.

Likewise, the digitization has eliminated the double pulse issue that was observed in the analog sliding mode counterpart. Since the digital control has a clock source that it follows per instruction, the pulse is generated only once on the clock cycle. Also, the cycle skip problem seen in the analog counterpart is likewise removed due to digitization.

D. Summary of Findings

The digital sliding mode control performance are summarized below. Compromises in the control gains are made to meet most of the requirements.

TABLE I
BEAT FREQUENCY DATA FOR 290 KHZ LOAD TRANSIENT FREQUENCY

Control Gains		Output Voltage		Inductor Currents		Freq. of Osc (kHz)	Cycle Skip	Double Pulse
K_1	K_2	V_{outmax}	V_{outmin}	I_{1max}	I_{2max}			
0	0.5	1.4761	1.3271	41.989	41.6697	None	None	None
-0.0078	0.5	1.4292	1.3544	36.579	36.398	None	None	None
-0.0116	0.5	1.4295	1.3617	36.676	36.4	None	None	None
-0.0155	0.5	1.4288	1.3631	36.891	36.837	None	None	None
0	0.75	1.519	1.3856	42.374	42.093	None	None	None
-0.0078	0.75	1.4783	1.4369	34.735	29.115	None	None	None
-0.0116	0.75	1.4807	1.4389	35.189	29.378	None	None	None
-0.0155	0.75	1.4818	1.4389	35.189	29.378	None	None	None
0	1	1.5345	1.4229	41.929	41.811	None	None	None
-0.0078	1	1.4821	1.461	34.927	29.31	None	None	None
-0.0155	1	1.5063	1.461	36.231	26.969	None	None	None

TABLE II
BEAT FREQUENCY DATA FOR 300 KHZ LOAD TRANSIENT FREQUENCY

Control Gains		Output Voltage		Inductor Currents		Freq. of Osc (kHz)	Cycle Skip	Double Pulse
K_1	K_2	V_{outmax}	V_{outmin}	I_{1max}	I_{2max}			
0	0.5	1.479	1.3238	42.284	42.297	None	None	None
-0.0078	0.5	1.4291	1.3544	36.579	42.297	None	None	None
-0.0116	0.5	1.4269	1.3623	35.757	35.72	None	None	None
-0.0155	0.5	1.4269	1.3632	36.042	35.552	None	None	None
0	0.75	1.5223	1.3856	43.01	42.988	None	None	None
-0.0078	0.75	1.4802	1.4404	32.392	27.722	None	None	None
-0.0116	0.75	1.4774	1.4401	34.697	28.821	None	None	None
-0.0155	0.75	1.4805	1.4156	37.005	37.065	None	None	None
0	1	1.5404	1.4258	42.368	42.539	None	None	None
-0.0078	1	1.5034	1.4662	34.72	29.243	None	None	None
-0.0155	1	1.5063	1.461	36.231	26.967	None	None	None

TABLE III
BEAT FREQUENCY DATA FOR 310 KHZ LOAD TRANSIENT FREQUENCY

Control Gains		Output Voltage		Inductor Currents		Freq. of Osc (kHz)	Cycle Skip	Double Pulse
K_1	K_2	V_{outmax}	V_{outmin}	I_{1max}	I_{2max}			
0	0.5	1.4817	1.3218	42.537	42.665	None	None	None
-0.0078	0.5	1.4296	1.3558	36.308	36.881	None	None	None
-0.0116	0.5	1.4293	1.3628	35.846	36.337	None	None	None
-0.0155	0.5	1.4287	1.364	36.618	36.367	None	None	None
0	0.75	1.5203	1.386	42.594	42.772	None	None	None
-0.0078	0.75	1.4829	1.413	36.823	37.005	None	None	None
-0.0116	0.75	1.4822	1.413	36.823	37.005	None	None	None
-0.0155	0.75	1.4817	1.4165	37.972	37.156	None	None	None
0	1	1.5351	1.4259	41.941	41.797	None	None	None
-0.0078	1	1.5077	1.4389	37.674	37.535	None	None	None

1) Output voltage ripple is shown within the specified 15mV limit.
2) Voltage regulation under minimum load failed to meet the 1.65% output voltage regulation band. This is attributed to the plant operating in discontinuous conduction mode. In the cases where there is sufficient load, the output voltage regulation is within the specified specification.
3) Current sharing accuracy meets the 5% error limit defined.
4) Dynamic performance still meets the requirements though not as well as the analog counterpart. The transient ripple increase observed in the digital equivalent can be as high as 100mV.
5) The control is shown to mitigate/eliminate the beat frequency oscillation given a very limited set of control gain values that are usable.

Tables IV and V provide the summary of the effects when the control gains K_1 and K_2 are varied. Just like any controller design, a compromise must be set by the applications engineer. We reiterate that K_1 and K_2 are dependent on the circuit parameters shown in (8).

TABLE IV
DESIGN GUIDE FOR CHOOSING K_2 VALUES WHEN K_1 IS CONSTANT.

K_1 Constant	Parameters		
K_2	Output Voltage	Output Voltage Ripple	Current Sharing
↑	↑	↑	–
↓	↓	↓	–

TABLE V
DESIGN GUIDE FOR CHOOSING K_1 VALUES WHEN K_2 IS CONSTANT.

K_2 Constant	Parameters		
K_1	Output Voltage	Output Voltage Ripple	Current Sharing
↑	↑	↑	–
↓	↓	↓	–

V. Conclusion

In this study, a digital fixed-frequency sliding mode controller has been designed and implemented to stabilize a two-phase voltage regulator module and eliminate the effects of beat frequency oscillation in the presence of fast transient loading. Digital control is achieved by employing the direct Z-transform on the analog switching control and designating the capacitor current as the derivative of its voltage. Extensive simulation results have shown that the digital fixed-frequency sliding mode controller has been able to eliminate beat frequency oscillation, double skipping in PWM generation of gate drives, occurring of double pulses, and providing acceptable results such as voltage regulation and equal sharing between phases. With these promising results, what is left is to implement the digital fixed-frequency sliding mode controller in an actual hardware.

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