Reconfigurable First-order Multifunction Active Filter Based-on DDAs and Their Applications

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***Abstract*— The purpose of this article is to describe the design and implementation of a reconfigurable voltage-mode first-order multifunction active filter based on a differential difference amplifier (DDA). The proposed multifunction filter is designed and constructed with two commercially available DDA integrated circuits: AD830, one resistor, and one grounded capacitor. By applying the input signals, the output responses are fully realized first-order functions such as low-pass, high-pass, inverting all-pass, and non-inverting all-pass responses. Because the input and output ports have high and low impedances, the proposed filter is an excellent choice for voltage-mode operation. Furthermore, the resistance and capacitance values of the proposed filter can be easily adjusted to control the pole frequency. Furthermore, as an example of an application, the construction of a sinusoidal oscillator based on the proposed first-order filter is demonstrated. The proposed circuit's performance is validated using the PSPICE program and through experimentation. The Monte Carlo Analysis is used to conduct a statistical analysis of the effect of tolerance errors on pole frequency and phase responses. The results of simulations and experiments clearly supported the theory, making it an excellent foundation for teaching and learning about electronics and electrical practice.**

***Index Terms*— First-order filter, DDA, High input impedance, Low output impedance**

I. INTRODUCTION

ANALOG signal processing systems [1–13] make extensive use of first-order multifunction filters, which are the most commonly used. This kind of filter is available in three different types, including low-pass (LP), high-pass (HP), and all-pass (AP). The LP filter is used to suppress signals with frequencies higher than the pole frequency and can also be used to construct a multiphase sinusoidal oscillator (MSO) in its simplest form [1-5]. Similarly, the HP filter suppresses signals below the pole frequency and is used to design the MSO [6–8]. Additionally, the AP filter is used to adjust the phase of signals while maintaining a constant amplitude across all frequencies [9–13]. A phase-lagging all-pass filter is called an inverting all-pass filter, while a phase-leading all-pass filter is defined as a non-inverting all-pass filter. These AP filters are often utilized to construct quadrature sinusoidal oscillators, MSOs, and high-Q band-pass filters [9-13]. As a result of the reasons outlined above for the usefulness of the first-order filters, they are widely studied and published in the literature [1-32]. They will be looked at in more detail in the next few paragraphs, with a summary in Table I.

The realizations of first-order active filters that operate in voltage-mode configurations are presented in references [14-32]. The proposed circuit in [14] has only one active element, which is comprised of one floating capacitor and one modified current differencing unit (MCDU), and it is extremely simple to build. The circuit can also be controlled electrically by using current gain. Unfortunately, MCDU implementation necessitates the use of six second generation electronically controllable current conveyors (ECCIIs) and one diamond transistor, resulting in an extremely complex configuration. Two subtractors, one resistor, and one capacitor are used in the circuits shown in [15]. Because the circuits produce all three output responses at the same time, the output response is fully functional for filters such as the LP, HP, and AP. HP and AP output responses are directed to connect with other circuits due to their low impedance. [16] shows one application example of z-copy controlled-gain voltage differencing current conveyor (ZC-CG-VDCC), in which a first-order filter is built using only one ZC-CG-VDCC and one grounded capacitor. It can also be controlled by adjusting the circuit's current gain and transconductance gain. The ZC-CG-VDCC behavioural model can be implemented using commercially available integrated circuits (ICs). However, the ZC-CG-VDCC requires three diamond transistors (OPA860) and one ECCII (EL2082), and it is difficult to implement due to the large number of ICs and active elements required. The OTRAs are used in the [17] reconfigurable first-order filters. This demonstrates that the circuit can produce first-order low-pass, high-pass, and all-pass responses all at the same time. The circuit also contains three floating capacitors and six floating resistors. This is an excessive number of passive elements, necessitating an increase in power consumption. In order for the filters to function properly, the resistor and capacitor values must be set identically. Despite this, the input port is not high impedance, necessitating the use of a voltage buffer at the input voltage node. A voltage-mode first-order filter with simultaneous output responses of all types is demonstrated in [18]. The proposed circuit design utilizes two differential voltage current conveyors (DVCCs), one

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resistor, and one capacitor. The output responses of HP and LP are necessary for load isolation by the voltage buffer. The high input impedance first-order filter is constructed from a single DVCC, a single grounded capacitor, and two resistors in [19]. The circuit is capable of producing three distinct output responses simultaneously: LP, AP, and HP. However, the output responses are reliant on the voltage buffer for linking and connecting to the subsequent stage or a loading device. The filter topologies proposed in [20] utilize two electronically controllable second-generation voltage conveyors (CVCIIs), one capacitor, and one resistor. Gain and center frequency can be electrically controlled using voltage and current biases, respectively. In the first circuit, the LP and AP topologies are presented, while the LP and HP topologies are presented in the second circuit. However, they utilize a floating capacitor, which is not optimal from the perspective of integrated circuits, and the topologies must be differentiated to achieve success with three types of filters. One digitally controlled differential voltage current conveyor (DCDVCC), three resistors, and three capacitors are used to build the filter described in [21], which is a voltage-mode reconfigurable fully differential first order multifunctional filter. Digital control is available for the reconfigurable, fully differential LP, HP, and AP filter responses at the same time. Nonetheless, the operation of the circuit is required to maintain the matching values of passive elements. In addition, the proposed circuit makes excessive use of passive elements, and their connections are floating, which renders it unsuitable for an integrated circuit. The filter in [22] is configured with one of the M-CCCCTA, a resistor, and a capacitor to produce an electrically controlled first-order multifunction filter. The output response is determined by the definition of the LP, HP, and AP input signals. The output port lacks a low impedance, and the input port lacks a high impedance, both of which are unacceptable for voltage-mode operation. Additionally, the active element used in this design must be modified from the standard version. Using a single CCDDCCTA and a single capacitor, the design in [23] implements a first-order universal filter. The voltage and current output responses are simultaneously accessible by selecting the appropriate input signals. Electronic adjustments for pole frequency and phase angle are also obtainable. However, the output response of HP and AP is accomplished by feeding the input signal through a floating capacitor, which lacks low impedance and is susceptible to parasitic influence. In addition, the output voltage is acquired at ports with a high output impedance, which is necessary for the voltage buffers to connect to other circuits. Using a single OTRA, two resistors, and capacitors, [24] depicts the construction of a multiple-input, single-output, first-order filter utilizing multiple inputs. In order to acquire LP, HP, and AP at the output port, the output response is determined by the selected signals. However, the circuit employs floating passive elements, and the input signal must pass through them for the circuit to function properly. The first-order filter in [25] is depicted as being electronically adjusted with respect to the pole frequency of the filter. The proposed design has a single CCDDCCTA

TABLE I
SUMMARY OF PREVIOUS RESEARCH

[a]	[b]	[c]	[d]	[e]	[f]	[g]	[h]	[i]	[j]
14	MCDU	1	0+1	No	AP, HP	No	No	Yes	No
15	Subtractor	2	1+1	Yes	AP, LP, HP	Yes	Yes (HP, AP), No (LP)	No	Yes
16	ZC-CG-VDCC	1	0+1	Yes	AP, LP	Yes	Yes	Yes	Yes
17	OTRA	3	6+3	No	AP, LP, HP	No	No	Yes	No
18	DVCC	2	1+1	Yes	AP, LP, HP	Yes	Yes (HP, AP), No (LP)	No	No
19	DVCC	1	1+2	Yes	AP, LP, HP	Yes	Yes (HP), No (LP, AP)	Yes	No
20	Fig. 2, CVCII	2	3+1	No	LP, AP	-	Yes	No	No
	Fig. 3, CVCII	2	3+1	No	LP, HP	-	Yes	No	
21	DCDVCC	2	3+3	No	AP, LP, HP	No	No	No	No
22	M-CCCCTA	1	1+1	Yes	AP, LP, HP	Yes	No	No	No
23	CCDDCCTA	1	0+1	No	AP, LP, HP	Yes	No	No	No
24	OTRA	1	2+2	No	AP, LP, HP	No	Yes	No	No
25	CCDDCCTA	1	0+1	No	AP, LP, HP	No	No	No	No
26	Fig. 2 a, DPDVCC	2	2+2	No	LP, AP	Yes	No	No	No
	Fig. 2 b, DPDVCC	2	2+2	Yes	HP, AP	Yes	No	No	No
27	OTA + ECCII	3	0+1	Yes	AP, LP	Yes	No	No	No
28	LT1228	1	2+1	No	AP, LP, HP	No	Yes	No	Yes
29	VD-DIBA	1	2+1	No	AP, LP, HP	No	Yes	No	Yes
30	OTA	2	1+1	Yes	AP, LP, HP	Yes	No	No	Yes
31	DVCC	1	1+1	Yes	AP	No	No	No	No
					LP	No	No	No	No
					HP	Yes	No	No	No
32	OTA	1	1+2	No	AP	No	No	No	Yes
					LP	Yes	No	No	Yes
					HP	No	No	No	Yes
Proposed circuit		2	1+1	Yes	AP, LP, HP	Yes	Yes	No	Yes

Remarks:
[a] References, [b] Type of active elements, [c] Number of active elements, [d] Number of resistor and capacitor,
[e] Only grounded capacitor, [f] Function of filter, [g] High input impedance, [h] Low output Impedance,
[i] Matching conditions, [j] Confirmation by experiment.

and one capacitor, so it has a very simple structure. The input impedance of node V_{in1} has a direct effect on the changing of the pole frequency, whereas the input impedance of V_{in2} is dependent on the presence of a passive capacitor that is inappropriate for use in voltage-mode operation. Fully differential first-order circuits using the DPDVCC are shown in [26], with the circuits being controlled by a digital control word. Two DPDVCC, two resistors, and two capacitors have been designed to develop both circuits. The first circuit is fully differential in terms of AP and LP responses, while the second circuit is fully differential in terms of AP and HP responses. The first circuit, which is regrettably used for floating capacitors, necessitates the use of a high-impedance output port for the AP response. In the same way, the second circuit uses capacitors connected to low impedance ports, which is a bad idea because these ports may have an internal resistor in series with the grounded capacitor, and the output node of AP responses is not low impedance, which requires voltage buffers for cascading. For the electronic reconfiguration of a first-order filter, the circuit design of [27] uses two OTAs, a single ECCII, and a single capacitor. The pole frequency can be used for electronic tuning, but the g_{m1} and R_x values must be fixed, which makes it inconvenient to utilize the frequency for tuning. The outputs AP and LP are also obtained at high-impedance ports, which can be utilized to connect to other circuits through a voltage follower. In [28], a single LT1228, one capacitor, and two resistors are used to construct a proposed voltage-mode first-order multifunction filter. The circuit characteristics include low output impedance and electronic control, as well as output response that is completely functional for all types of filters, including LP and HP, as well as inverting and non-inverting AP. However, since the input voltage signals are fed through passive elements, the input ports of V_{in1} and V_{in3} do not have a high input impedance. Furthermore, the function of AP works as if the values R_f and R_1 are kept in the same ratio. A voltage-mode first-order universal filter is the aim of the proposed circuit in [29]. One VD-DIBA, one capacitor, and two resistors are used in the construction of the circuit. The pole frequency and phase response can be controlled electronically, and it has a low output impedance. The output response filters, such as the LP, HP, and AP, are fully dependent on the input signals. The input ports of V_{in2} and V_{in3} are, on the other hand, fed by passive elements, such that the input impedance is not high, which is dependent on the passive element values. Furthermore, if the values of R_1 and R_2 are the same, the function of AP is corrected. The voltage mode first-order multifunction filter in [30] is constructed using two OTAs, one resistor, and one capacitor. It can be operated in three responses: HP, LP, and AP, depending on the input signals. In addition, it can be electrically controlled and the input ports have high impedances. However, the circuit has a very high output impedance port, which means that a voltage buffer is needed to connect or link the other stages or circuits. The proposed circuit in [31] is constructed with a single DVCC, one resistor, and one capacitor. The input port V_{i1} has a high impedance, but the impedance of input port V_{i2} is dependent on a resistor, and the output port is also not low impedance, which needs a voltage follower for connecting to the other circuits. The OTA-C filter shown in [32] is operated for three responses: HP, AP, and LP, depending on the input signals used. It includes one OTA-C, one resistor, and two capacitors. Unfortunately, the output port needs a voltage buffer, and the input impedance of port V_{i2} depends on the capacitance.

In this paper, the first-order active filter is introduced and its design and implementation are discussed. The first-order active filter is realized using a differential difference amplifier (DDA), which allows for greater flexibility. In the circuit design with two DDAs, one resistor and one capacitor are utilized. By feeding the input signal into the proposed filter's input nodes, the filtering output functions low-pass, all-pass, and high-pass responses can be selected. The circuit's output and input ports have low and high impedances, respectively. Utilizing computer software and experiments utilizing commercially available integrated circuits, the performance of the proposed filter is assessed (ICs). The results agree well with those of the theoretical analysis, making them ideal for use in the classroom and lab when teaching and learning electronic and electrical engineering.

II. PROPOSED CIRCUIT

The AD830 [33] from Analog Devices is a differential difference amplifier (DDA) compatible integrated circuit that is currently available commercially. The electrical symbol and pin layout of the device are shown in Fig. 1. The input ports include differential inputs with high impedances labeled X_1, X_2, Y_1, and Y_2, respectively. It is a differential amplifier with a wideband output that is packaged in an 8-pin design and operates from a supply voltage of ±5V to ±15V. The output voltage port is low impedance. The electrical characteristics of AD830-DDA can be expressed mathematically as

$$V_{OUT} = A_0\left((V_{X1} - V_{X2}) + (V_{Y1} - V_{Y2})\right), \qquad (1)$$

where A_0 is the open loop gain of the DDA. A negative feedback loop can be introduced by connecting V_{Y2} to V_{OUT} ($V_{Y2} = V_{OUT}$) as shown in Fig. 2. With this topology, the output voltage is given by

$$V_{OUT} = V_{X1} - V_{X2} + V_{Y1}. \qquad (2)$$

The schematic design of the proposed filter circuit for the first-order multifunction active filter is shown in Fig. 3. It is comprised of two AD830s, a single resister, and a single grounded capacitor. It is found that the proposed circuit is constructed the commercially available integrated circuit (IC) that is easy to implement and test in order to evaluate the performance of the circuit utilizing laboratory equipment. The proposed filter has two nodes of input signals: V_{in1} and V_{in2}, as well as a single node of output signal, denoted as V_O. The input signals have been directly delivered to the high impedance ports, and the output signal has been given to the low impedance port, making it an

excellent design for use in a voltage-mode configuration [34-35]. Using Eq. (2) for determining the output voltage, V_O of the proposed filter, it yields

$$V_O = \frac{V_{in1} - sC_1R_1V_{in2}}{sC_1R_1 + 1}. \quad (3)$$

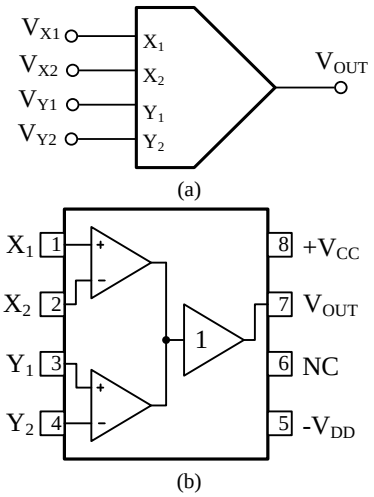


Fig. 1. DDA (a) electrical symbol, (b) pin layout

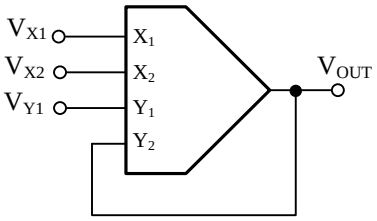


Fig. 2. Closed-loop connection

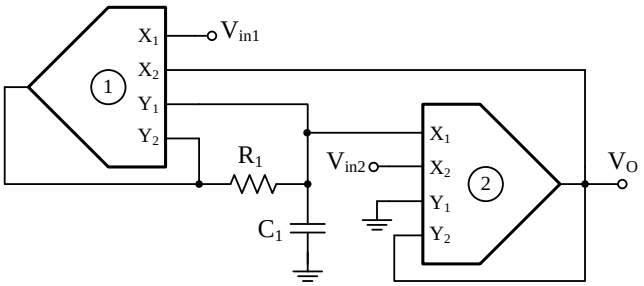


Fig. 3 Proposed first-order multifunction active filter

By feeding the input signal to input voltage nodes, V_{in1} and V_{in2}, the output responses of low-pass, high-pass, and all-pass can be achieved. The following methods can be used to describe the input signal configurations required to obtain the necessary filtering output responses.

The input signal is fed into the node, V_{in1}, and the node, V_{in2}, is joined to the ground. Thus, the output response is successful as a low-pass (LP) response. The LP voltage transfer function can be represented as in Eq. (4).

$$LP = \frac{V_O}{V_{in1}} = \frac{1}{sC_1R_1 + 1}. \quad (4)$$

The high-pass response can be successfully achieved by feeding only the input signal to node V_{in2}, while node V_{in1} is connected to the ground. The voltage transfer function of the high-pass (HP) response can be seen as follows:

$$HP = \frac{V_O}{V_{in2}} = -\frac{sC_1R_1}{sC_1R_1 + 1}. \quad (5)$$

The output response for an inverting all-pass filter ($AP_{(-)}$) is given by feeding the input signal to nodes V_{in1} and V_{in2}. The $AP_{(-)}$ voltage transfer function can be presented in Eq. (6).

$$AP_{(-)} = \frac{V_O}{V_{in}} = \frac{-sC_1R_1 + 1}{sC_1R_1 + 1}. \quad (6)$$

The non-inverting all-pass filter ($AP_{(+)}$) can be obtained by feeding the inverting input signal to nodes V_{in1} and V_{in2}. In this case, an inverting amplifier with a gain of one is used to invert the input signal. The $AP_{(+)}$ voltage transfer function is denoted by

$$AP_{(+)} = \frac{V_O}{V_{in}} = \frac{sC_1R_1 - 1}{sC_1R_1 + 1}. \quad (7)$$

Additionally, the pole frequency of the transfer function can be examined and given by Eq. (8)

$$\omega_p = \frac{1}{C_1R_1}. \quad (8)$$

Equation (8) shows that it's easy to adjust the pole frequency by changing the values of passive elements like resistors, capacitors, or both.

The phase responses for each filtering function can be obtained as follows:

$$\theta_{LP} = -\tan^{-1}(\omega C_1R_1), \quad (9)$$

$$\theta_{HP} = \tan^{-1}(\omega R_1C_1) - 180^\circ, \quad (10)$$

$$\theta_{AP(-)} = -2\tan^{-1}(\omega C_1R_1), \quad (11)$$

and

$$\theta_{AP(+)} = 180^\circ - \tan^{-1}(\omega C_1R_1). \quad (12)$$

The sensitivity of the pole frequency in Eq. (8) is given by

$$S^{f_p}_{C_1,R_1} = -1. \quad (13)$$

III. A Non-ideal Analysis

The non-idealities of the proposed filter are discussed in this section. The impact of the tracking errors and parasitic elements in DDA is considered. The voltage tracking errors are β_{X_1}, β_{X_2} and β_{Y_1}. Considering these errors, the output voltage in Eq. (2) becomes

$$V_{OUT} = \beta_{X_1}V_{X1} - \beta_{X2}V_{X2} + \beta_{Y1}V_{Y1}. \quad (14)$$

In an ideal case, these voltage tracking errors would equal one. The parasitic elements of DDA are shown in Fig. 4, which include resistors and capacitors linked to the ground at high impedance ports and a series resistor at a low impedance port.

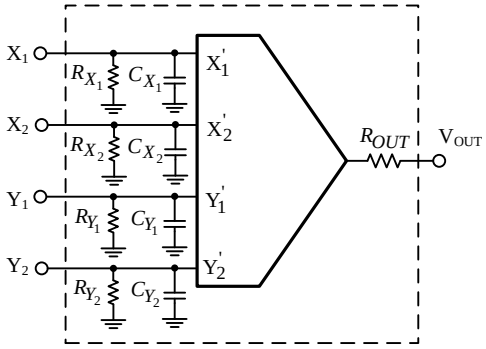


Fig.4. Parasitic elements of DDA

The output voltage of the proposed circuit will be reanalyzed to evaluate its efficiency in the presence of tracking errors and parasitic elements. The output voltage with tracking errors and parasitic elements is given by

$$V_O = \frac{\beta_{X_{11}}\beta_{X_{21}}G_1V_{in1} - N(s)\beta_{X_{22}}V_{in2}}{D(s)}, \qquad (15)$$

while $N(s) = (C_1 + C_{Y11} + C_{X21})s + G_{Y11} + G_{Y21} + G_1 - \beta_{Y_{11}}G_1$,

$D(s) = (C_1 + C_{Y11} + C_{X21})s + G_{Y11} + G_{Y21} + G_1 + \beta_{X_{12}}\beta_{X_{21}}G_1 - \beta_{Y_{11}}G_1$

, $R_{X12}, R_{X21}, R_{Y11}, R_{Y21}, R_1 >> R_{OUT}$, $G_1 = 1/R_1$,

$G_{X_{12}} = 1/R_{X_{12}}$, $G_{X_{21}} = 1/R_{X_{21}}$, $G_{Y_{11}} = 1/R_{Y_{11}}$ and

$G_{Y_{21}} = 1/R_{Y_{21}}$.

The pole frequency with tracking errors and parasitic elements can be expressed in the following manner:

$$\omega_p = \frac{G_{Y11} + G_{Y21} + G_1 + \beta_{X_{12}}\beta_{X_{21}}G_1 - \beta_{Y_{11}}G_1}{C_1 + C_{Y11} + C_{X21}}. \qquad (16)$$

In practice, the accurate value of the pole frequency can be fixed by making small changes to the values of the resistors or capacitors in the circuit.

IV. Results and Discussions

A first-order multifunction filter circuit was evaluated by simulation using the PSPICE software. Two commercially available integrated circuits: AD830, one resistor, and one capacitor were used to construct the proposed filter. The macro model of the AD830 from Analog Devices was set up according to the specification, while the resistance and capacitance values were set to 1kΩ and 1nF, respectively. The supply voltage was biased by ±5V. The simulation results shown in Fig. 5 demonstrate how the proposed filter obtained a low-pass response by feeding the input voltage signal to node V_{in1}. The phase shift of the pole frequency was 45 degrees, and the pole frequency was roughly 157.90kHz. The gain and phase responses agreed with what was predicted theoretically. Figure 6 shows a high-pass filter's gain and phase responses by feeding the input voltage signal to node V_{in2}. The frequency and phase angle of the -3dB gain response were 158.50 kHz and -135 degrees, respectively. The simulated results matched those of every theoretical calculation exactly. When the input signal is transmitted to both input voltage nodes, as in Figure 7, the simulation results for an inverting all-pass filter are displayed. It is noted that the gain responses were approximately 0 dB, and the pole frequency was approximately 158.50 kHz with a phase shift of -90 degrees. The simulation result is in accordance with the theory.

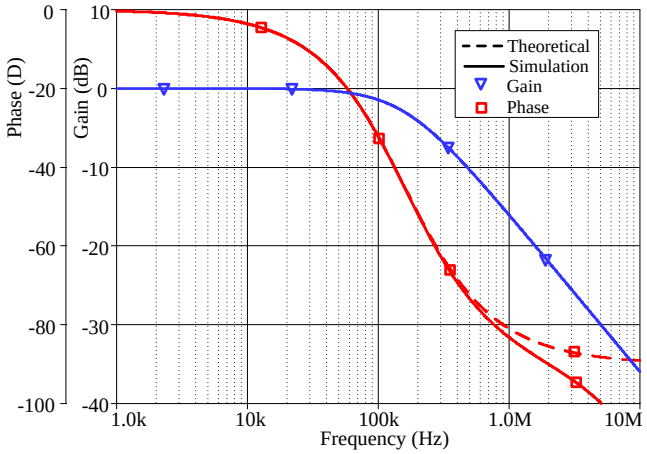


Fig.5. Simulation results of LP

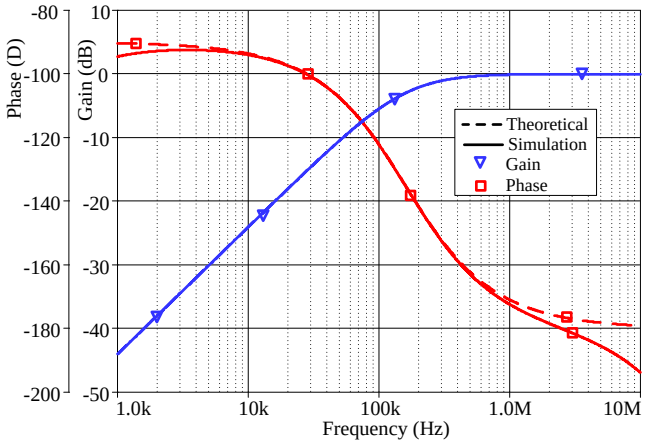


Fig. 6. Simulation results of HP

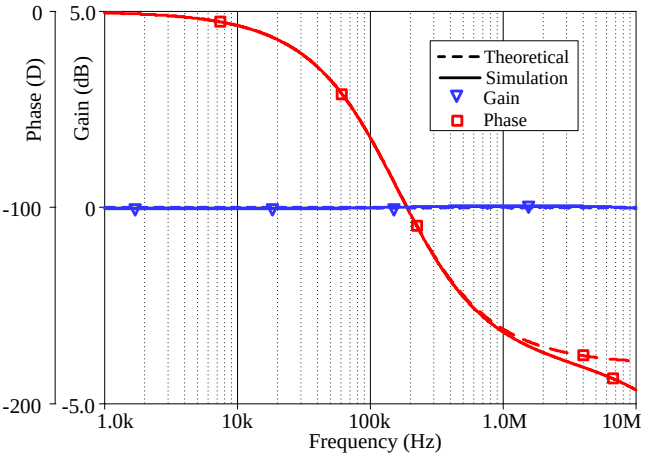


Fig. 7. Simulation results of $AP_{(-)}$

Fig. 8 shows the gain and phase response of a non-inverting all-pass filter. The theoretical and simulation results were slightly different with a phase shift of 90 degrees, the pole frequency of 158.50 kHz and a gain response of 0dB. The adjustment of the phase shift for of an inverting all-pass filter is depicted in Fig. 9. In this example, the phase shift of an inverting all-pass response was adjusted by changing the value of resistor R_1 to 250Ω, 500Ω, 1kΩ and 2kΩ, respectively. The simulation indicates that the phase shift of the proposed filer is adjusted by R_1 as

expected in Eq. (11). At the phase shift of -90 degrees, the pole frequencies from the R_1 values were located at 620.72kHz, 314.44 kHz, 158.50 kHz, and 79.81 kHz, respectively. The simulation in the time domain of an inverting all-pass filter is depicted in Fig. 10, when a sinusoidal signal with a frequency of 158.50kHz and an amplitude of 400mVp-p was applied. The sinusoidal output signal was laggard by -90 degrees and had a similar amplitude as the input signal. Fig. 11 plots the relationship between the percent total harmonic distortion (THD) of a sinusoidal output signal and the input amplitude. The simulation results are appropriate because the %THD is less than 0.01 percent.

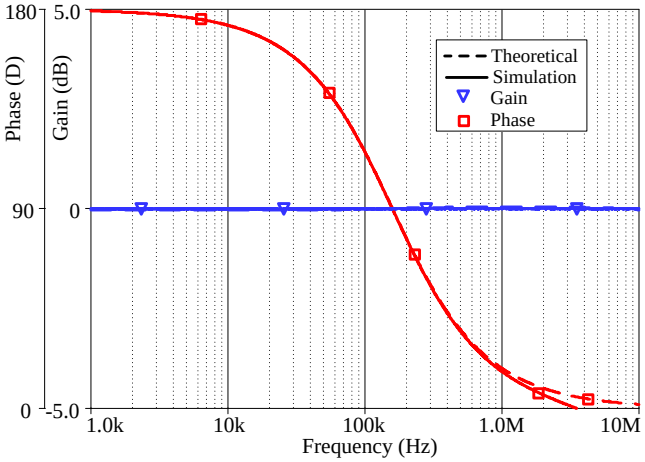


Fig. 8. Simulation results of $AP_{(+)}$

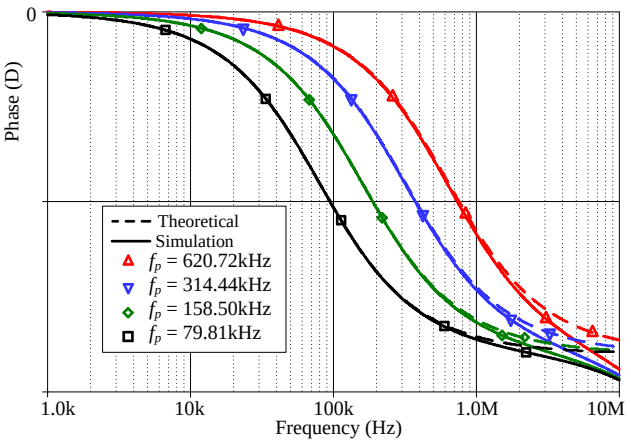


Fig. 9 Phase responses of $AP_{(-)}$

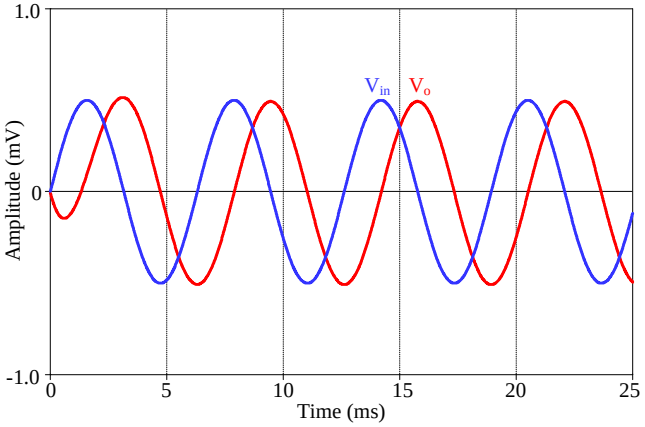


Fig. 10. Time-domain of inverting all-pass filter

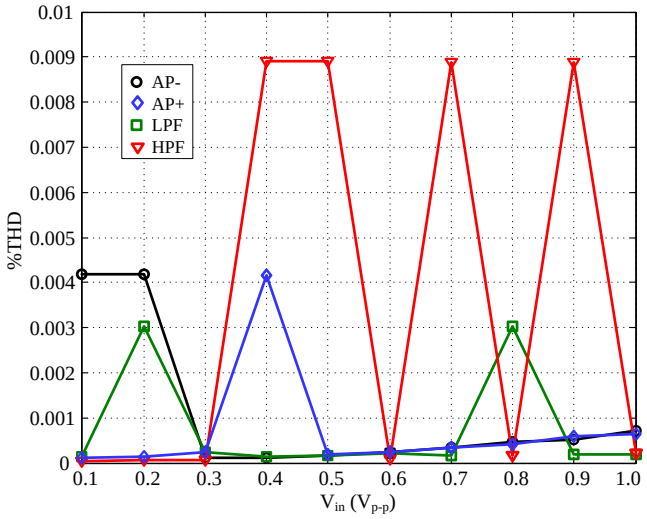
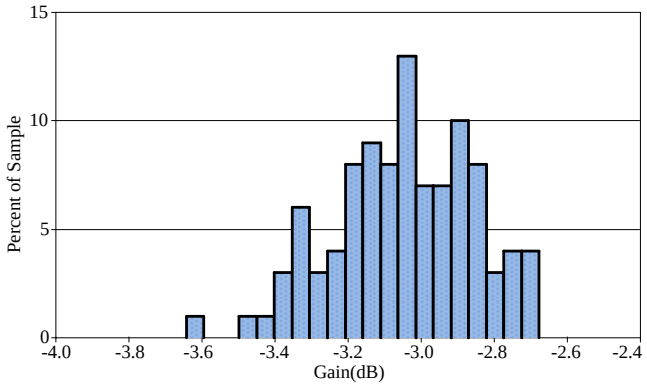
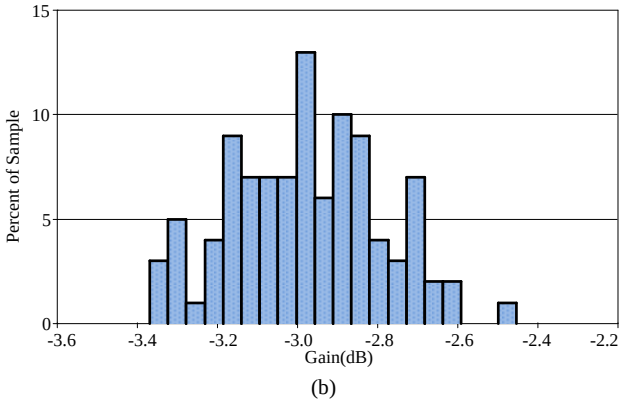


Fig. 11. THD vs amplitude of input signals

The tolerance of passive elements has impacted the capability of the proposed circuit. Thus, the Monte Carlo analysis was used to analyze the gain and phase responses in order to identify the parameters of these responses. The analysis was performed 100 times using the Gaussian Distribution and the tolerances of the passive resistor and capacitor were set to 1% and 5%, respectively. The results in Fig. 12 (a), (b), (c), and (d) plot the histograms of the gain responses at the pole frequency of low-pass, high-pass, inverting all-pass, and non-inverting all-pass filters, respectively. Table II contains a detailed description of the gain characteristics of the pole frequency, as well as a summary of those parameters. There are many definitions of pole frequency characteristics, including the mean, median, minimum, maximum, and standard deviation. In addition, the histograms of the phase responses at the pole frequency of low-pass, high-pass, inverting all-pass, and non-inverting all pass filters are presented in Fig. 13.



(a)



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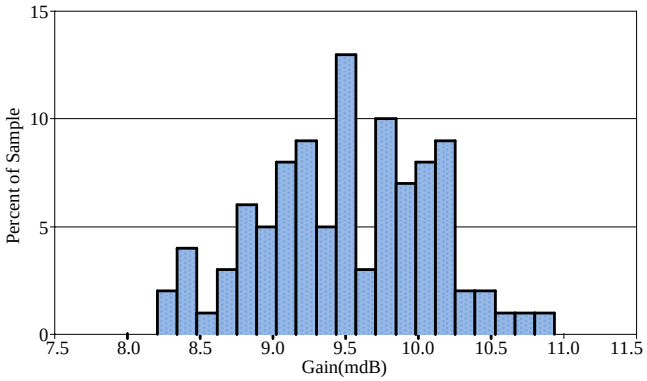

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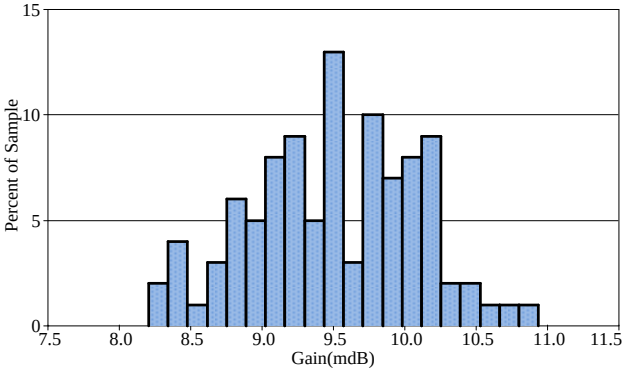
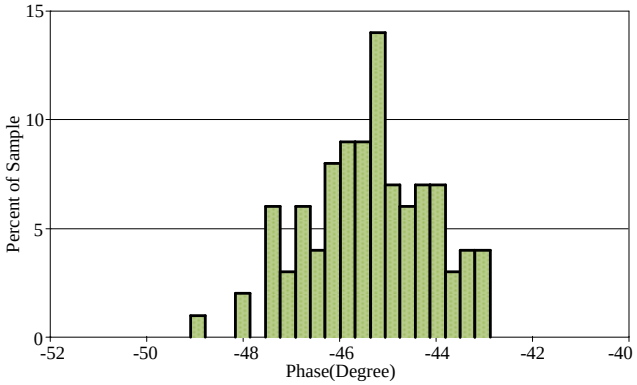


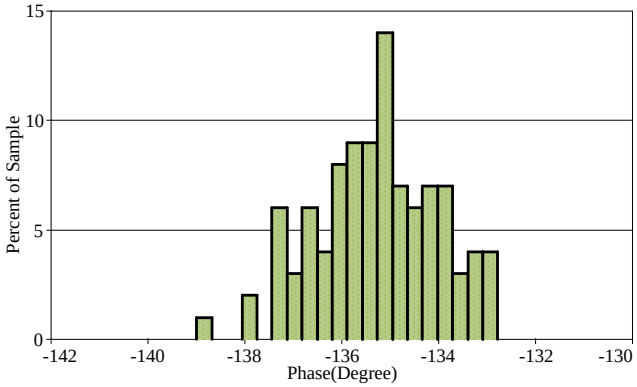
(d)

Fig. 12. The histograms of the gain responses (a) LP (b) HP (c) $AP_{(-)}$ (d) $AP_{(+)}$

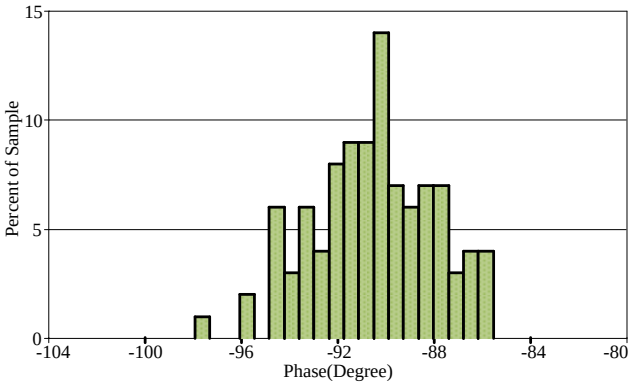
Table III provides a summary of the phase parameters at the pole frequency as well as information on the mean, median, minimum, maximum, and standard deviation of the phase parameters.



(a)



(b)



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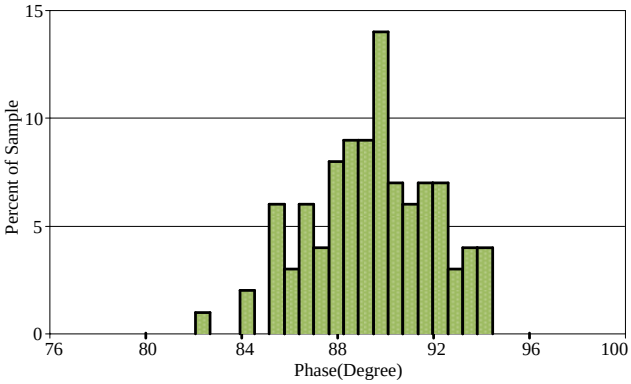


(d)

Fig. 13. The histograms of the phase responses (a) LP (b) HP (c) $AP_{(-)}$ (d) $AP_{(+)}$

TABLE II
GAIN RESPONSES AT THE POLE FREQUENCY

Function of filter	Gain (dB)				
	Mean	Median	Minimum	Maximum	Standard deviation
Low-pass	-3.04	-3.03	-3.64	-2.67	0.19
High-pass	-2.97	-2.98	-3.36	-2.45	0.18
Inverting All-pass	0.009	0.009	0.008	0.010	0.0005
Non-inverting All-pass	0.000	0.009	0.008	0.010	0.0005

TABLE III
PHASE RESPONSES AT THE POLE FREQUENCY

Function of filter	Phase (Degrees)				
	Mean	Median	Minimum	Maximum	Standard deviation
Low-pass	-45.38	-45.35	-49.09	-42.87	1.26
High-pass	-135.28	-135.25	-138.99	-132.77	1.26
Inverting All-pass	-90.55	-90.48	-97.94	-85.55	2.52
Non-inverting All-pass	89.44	89.51	82.05	94.44	2.52

The prototype was used to test the proposed first-order multifunction active filter. An experiment was conducted using an Analog Devices AD830 integrated circuit and standard values of passive elements with $R_1 = 1\text{k}\Omega$ and $C_1 = 1\text{nF}$ were configured. The voltage power supply used in the experiment was a Siglent SPD3303C, which had been set to ±5V. The frequency responses of the proposed filter were measured using the frequency response analyzer feature of the Keysight oscilloscope model DSOX3024T. The frequency response analyzer was adjusted by sweeping from 1kHz to 10MHz with an amplitude of 200mVp-p.

When node V_{in1} received the input voltage and V_{in2} was connected to ground, the experiment investigating low-pass responses was effectively carried out. Fig. 14 displays the results of the gain and phase responses. Figure 15 displays the input and output waveforms with a frequency of 159.15kHz and an amplitude of 200 mVp-p. The experimental gain and phase shift are 2.9dB and -45.56 degrees, while the theoretical pole frequency was at 159.15 kHz with a 3dB decrease in amplitude and a -45 degrees phase shift in the output signal. The waveforms in Figs. 15 (a) and (b) show the input and output waveform in the time domain when the frequencies are set to 10 kHz and 1 MHz, respectively. It is found that the amplitude of the input V_{in1} and the output V_O at frequency of 10kHz has the same amplitude. In the meantime, the amplitude of the output V_O for a frequency of 1 MHz was suppressed by 16dB. This indicates that the results of these experiments agree with the theoretical analysis in Eqs. (4) and (9). The result of the experiment in Fig. 16 shows the high-pass responses when the input signal was fed to node V_{in2} and node V_{in1} is connected to the ground. The time domain can be verified by feeding a sinusoidal signal with a frequency of 159.15 kHz and an amplitude of 200mVp-p, as shown in Fig. 17 (a). The output waveforms were consistent with the theory, with a gain of about 2.8dB amplitude and about a 137.81 degrees phase shift. In addition, the lower and higher frequencies of pole frequency are set to 10kHz and 1MHz, as seen in Figs. 17 (b) and (c), respectively. The voltage gains at 10kHz and 10MHz are 23.6dB and 1.8dB, respectively, and their phases are close to the theoretical analysis in Eq. (10). Inverting all-pass responses were achieved by inputting the input signal into both input nodes. The experimental response is displayed in Fig. 18, which includes the gain and phase responses. The output gain is about 0dB for all frequencies and the phase shifted is changed from -0.04 to -180 degrees. The time domain shown in Fig. 19 (a) verified the inverting all-pass responses by injecting a sinusoidal signal with a frequency of 159.15 kHz and an amplitude of 200mVp-p into the circuit. The phase of the output signal was shifted to about -89.84 degrees, which is theoretically permissible. The input and output waveforms at the frequencies 10kHz and 1MHz are depicted in Figs. 19 (b) and (c) respectively. It is found that the amplitudes of inputs and outputs are closed, and the phases of inputs and outputs agree with theoretical predictions. In addition, the experimental frequency response of a non-inverting all-pass is displayed in Fig. 20, which includes both gain and phase responses. The gain response was about 0 dB, and the phase shift was changed from 179.12 to -43.21 degrees. Fig. 21 (a) illustrates the time domain of a 159.15 kHz frequency with a phase shift of 88.46 degrees. The waveforms shown in Figures 21 (b) and (c) are the input and output signal of 10kHz and 10MHz frequencies, respectively. It is evident that their amplitudes are the same and their phases match to Eq. (12). It can be observed that the experimental results in Figs. 15, 17, 19, and 21 are consistent with the Monte Carlo analysis in Tables II and III.

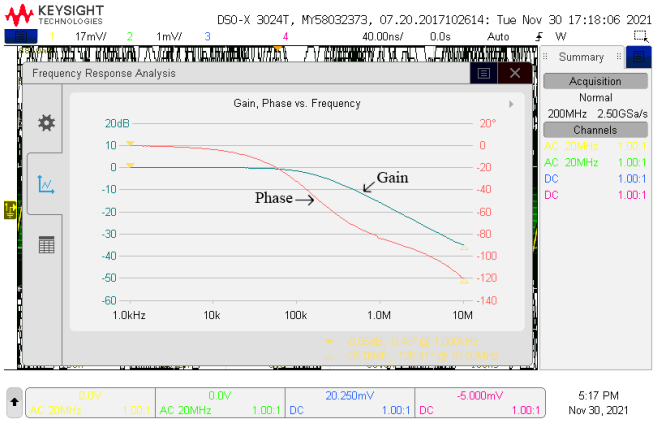
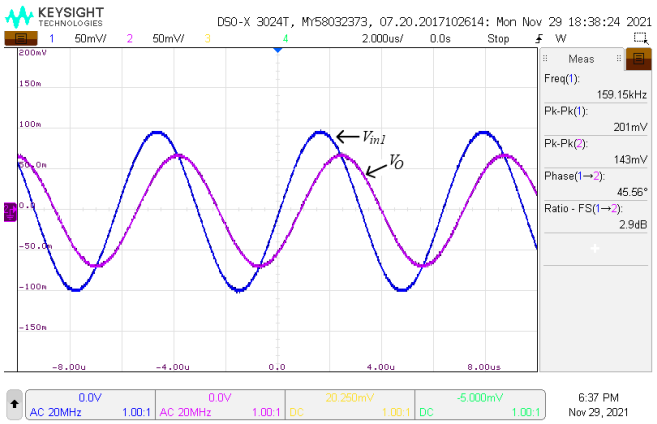
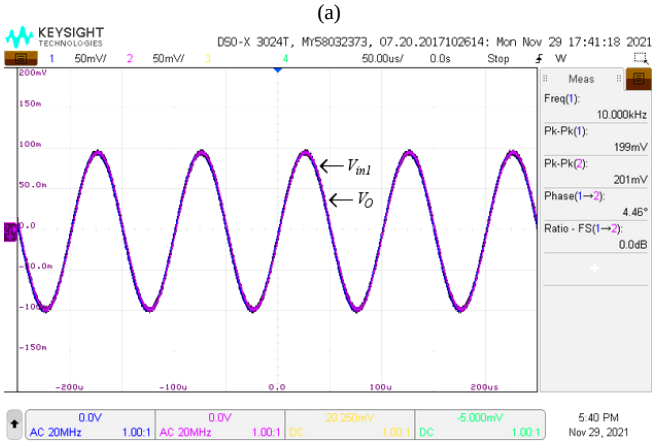


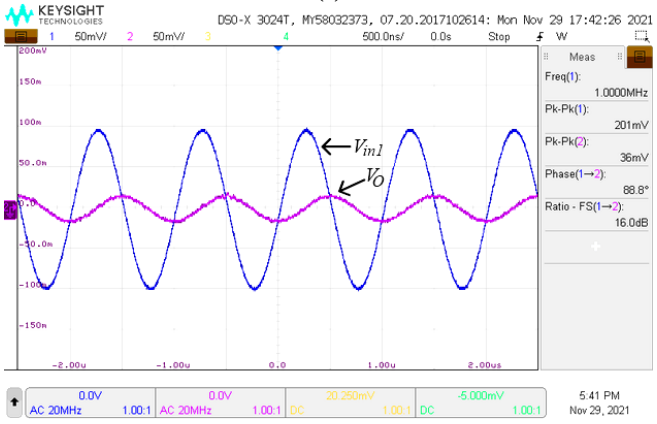
Fig. 14. The frequency responses of gain and phase of LP



(a)



(b)



(c)

Fig. 15. The waveforms of the input and output of LP (a) f = 159.15kHz (b) f = 10kHz (c) f = 1MHz

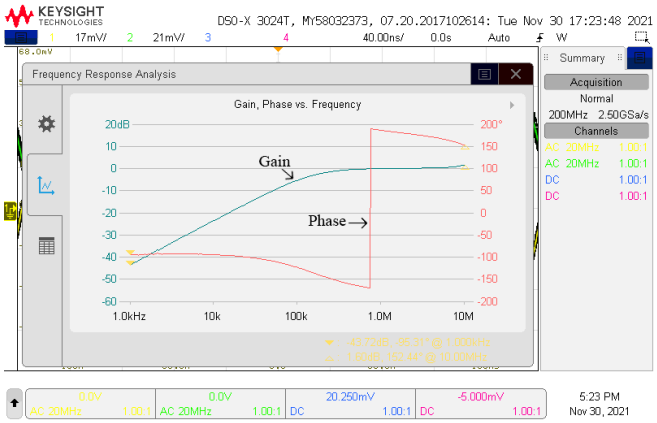


Fig. 16 The frequency responses of gain and phase of HP

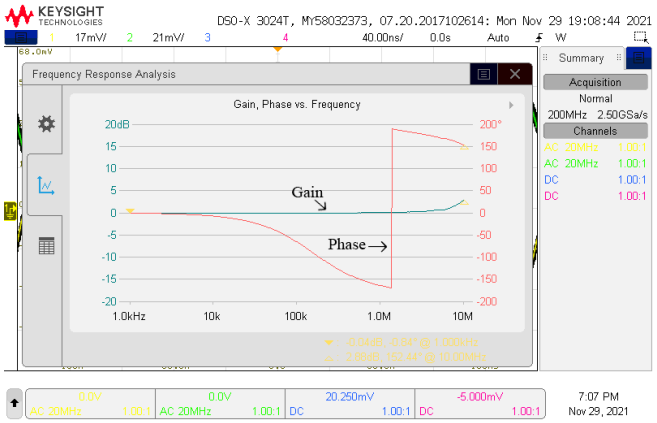
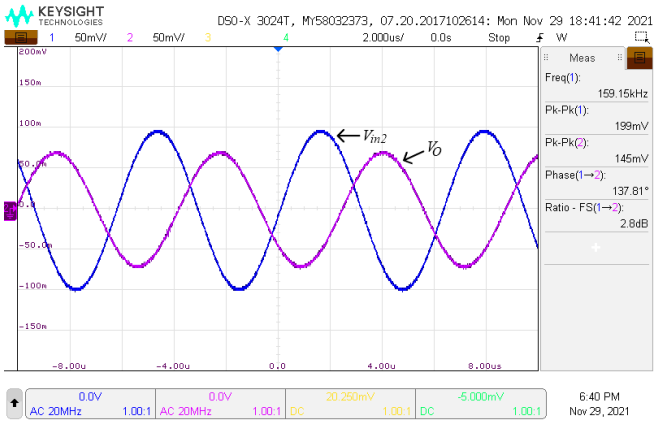
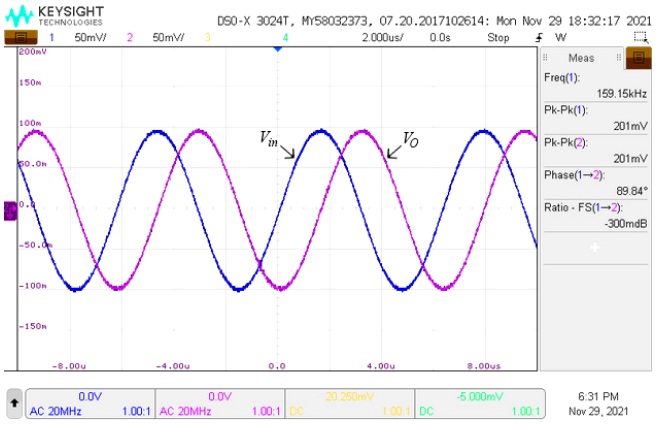


Fig. 18. The frequency responses of gain and phase of $AP_{(-)}$



(a)



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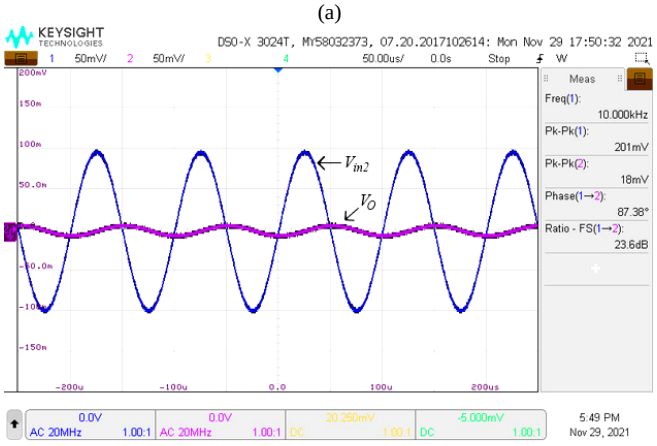

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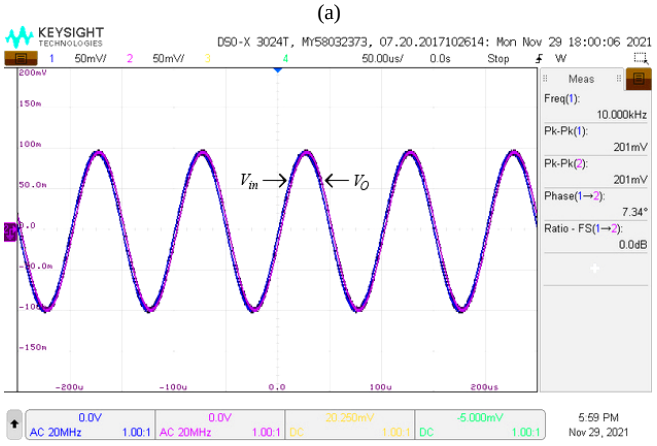

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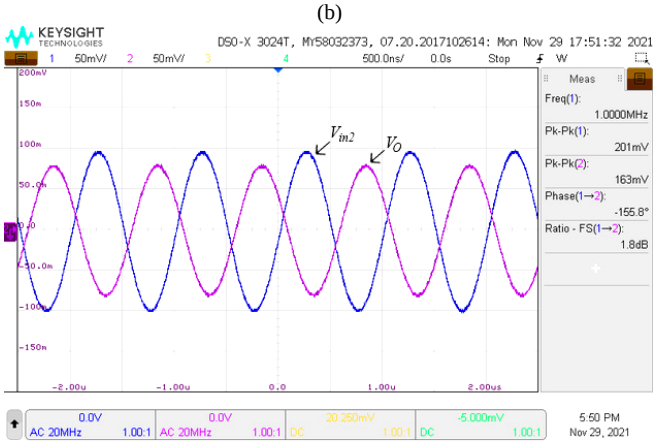
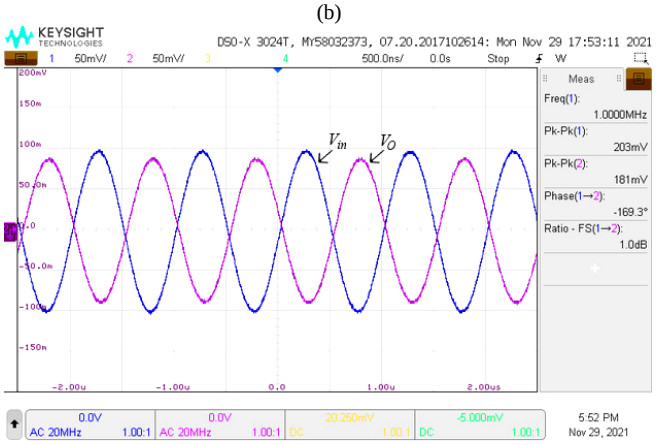


(c)

Fig. 17. The waveforms of the input and output of HP (a) f = 159.15kHz (b) f = 10kHz (c) f = 1MHz



(c)

Fig.19. The waveforms of the input and output of $AP_{(-)}$ (a) f = 159.15kHz (b) f = 10kHz (c) f = 1MHz

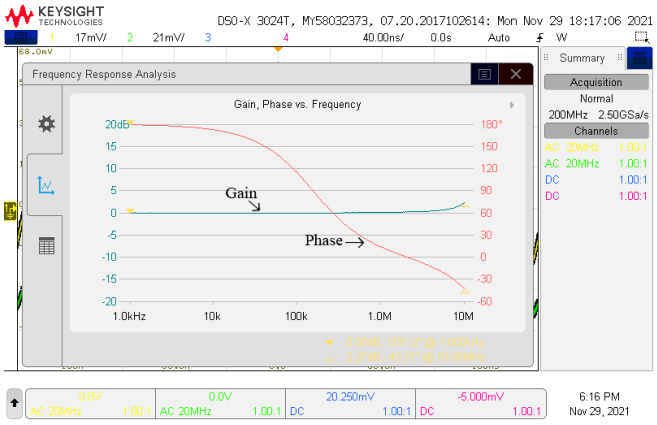


Fig. 20. The frequency responses of gain and phase of $AP_{(+)}$

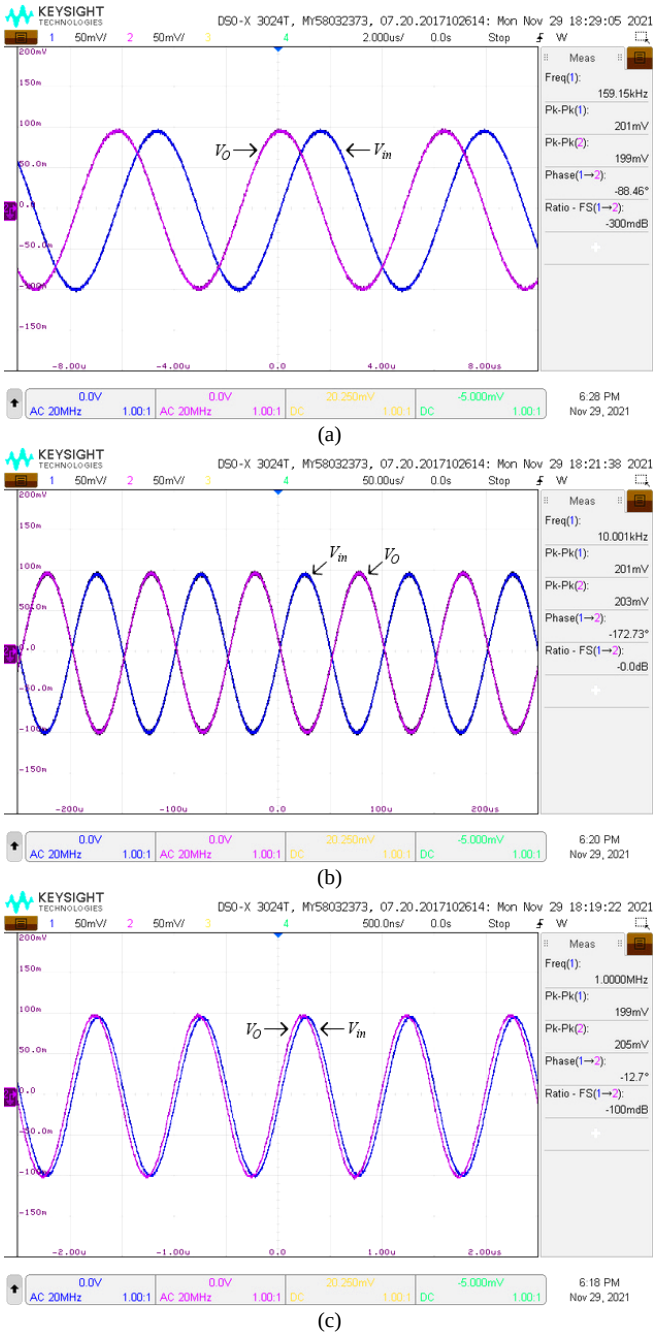


Fig. 21. The waveforms of the input and output of $AP_{(+)}$ (a) f = 159.15kHz (b) f = 10kHz (c) f = 1MHz

Furthermore, the phase response of the proposed filter can be changed by adjusting the values of resistor R_1. Inverting all-pass responses were demonstrated in this study by adjusting R_1 to 500Ω, 1kΩ, and 2kΩ. At the phase shift of -90 degrees, the experimental pole frequencies from the R1 values were located at 309.02kHz, 158.48kHz, and 75.85kHz, respectively, as plotted in Fig. 22. The experimental result indicates that the phase shift of the proposed filer is adjusted by R1 as expected in Eq. (11).

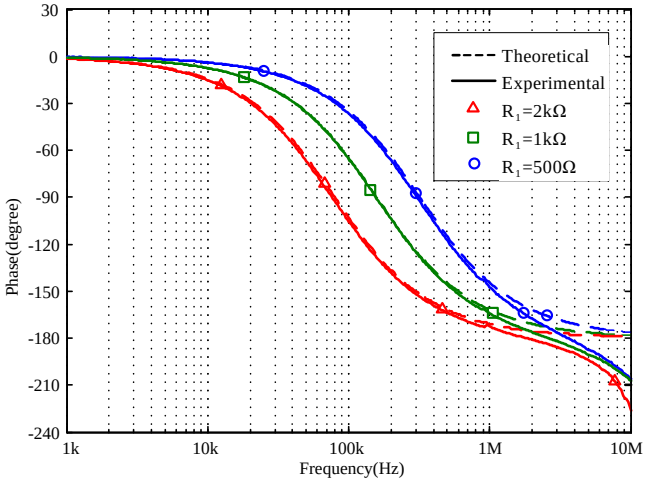


Fig. 22. The variation of phase responses

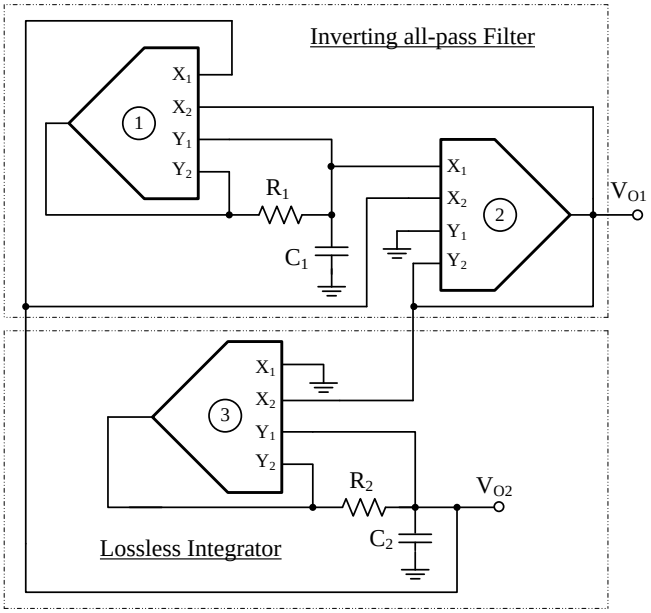


Fig. 23 Sinusoidal oscillator

V. An Example of the Proposed Filter

An application example of a first-order all-pass filter is to design the quadrature sinusoidal oscillator. The oscillator schematic shown in Fig. 23 is constructed using the cascade of an inverting all-pass filter and a lossless integrator. The characteristic equation of the this sinusoidal oscillator can be analyzed and written as follows:

$$s^2 + s\left[\frac{1}{C_1R_1} - \frac{1}{C_2R_2}\right] + \frac{1}{C_1C_2R_1R_2} = 0. . \qquad (17)$$

The oscillator can generate sinusoidal signals if the condition of oscillation is achieved by following condition

$$C_1R_1 = C_2R_2 . \qquad (18)$$

From Eq. (14), the frequency of oscillation is obtained as

$$\omega_{osc} = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}. \quad (19)$$

The voltage transfer function of the sinusoidal output waveform V_{O1} and V_{O2} is expressed as

$$\frac{V_{O1}(s)}{V_{O2}(s)} = \frac{1}{C_2 R_2 s}. \quad (20)$$

From Eq. (20), the phase response of the sinusoidal output waveform V_{O1} and V_{O2} is given by

$$\frac{V_{O1}(j\omega)}{V_{O2}(j\omega)} = \frac{1}{C_2 R_2 \omega} e^{-j90}. \quad (21)$$

According to Eqs. (18) and (19), the passive elements can be configured as $C_1 = C_2 = C$ and $R_1 = R_2 = R$, while the sinusoidal steady states of the magnitude ratio of V_{O1} and V_{O2} are equal, and denoted by

$$\left|\frac{V_{O1}(j\omega_{osc})}{V_{O2}(j\omega_{osc})}\right| = 1. \quad (22)$$

It is interested that the phase difference between the sinusoidal signals is 90 degrees, and the amplitude of the sinusoidal signals is equal.

The performance of a proposed quadrature sinusoidal oscillator was evaluated using the PSPICE software. The quadrature sinusoidal oscillator was constructed by using the commercially available ICs: AD830. The supply voltage of the circuit was set to ±5V. The passive elements of the circuit were configured and designed to satisfy the oscillation condition in Eq. (18), which are $R_1 = R_2 = R = 1\text{k}\Omega$ and $C_1 = C_2 = 1\text{nF}$. The passive elements were designed to achieve the oscillation frequency of 159.15 kHz. The simulation result in Fig. 24 shows the transient response of proposed oscillator, whereas the result in Fig. 25 illustrates the steady state response. The amplitude of the sinusoidal signals of V_{O1} and V_{O2} are equal, which is consistent with Eq. (22). The phase relationship can be represented as a Lissajous Figure as shown in Fig. 26. The simulated frequency of is about 150 kHz. The frequency spectrum of V_{O1} and V_{O2} is presented in Fig. 27. The THD percentages are approximately 0.75% and 2.12%, respectively. The absolute error in the simulated frequency is thought to be about 5.74 % due to tracking errors and the parasitic elements of active devices.

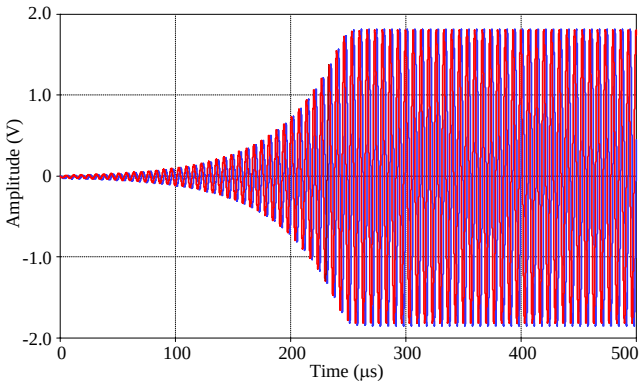


Fig. 24 Sinusoidal signals in transient response

The Monte Carlo analysis is used to simulate the frequency histograms because there are tolerance errors in the passive elements. The resistor and capacitor tolerance errors are set at 1% and 10%, respectively. The frequency histogram with 100 samples and the Gaussian Distribution is displayed in Fig. 28. The maximum and minimum frequencies are 168.68 kHz and 120.45 kHz, respectively, as well as the mean and median frequencies are 146.17 kHz and 146.06 kHz, respectively.

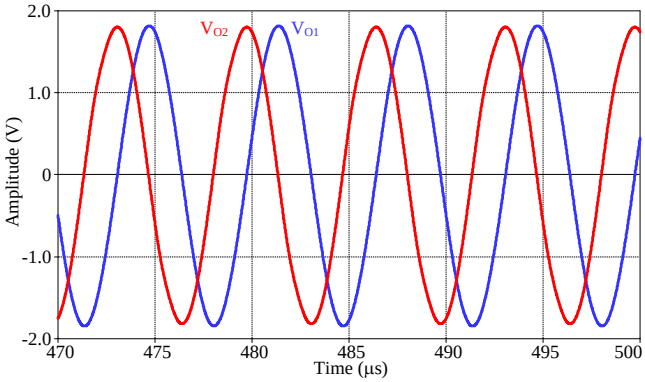


Fig. 25 Sinusoidal signals in steady state response

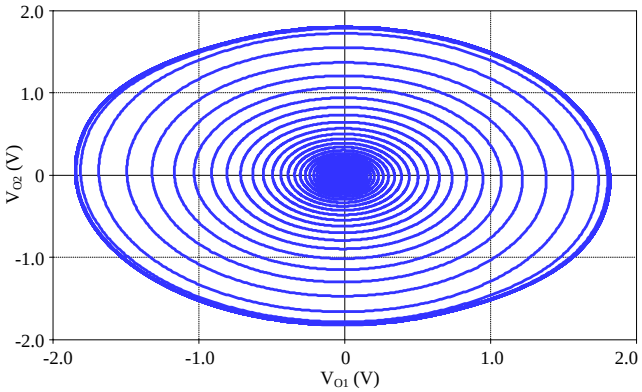


Fig. 26 Phase relation with Lissajous Figure

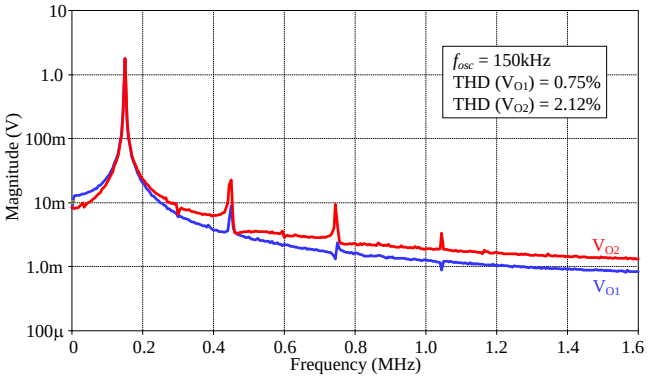


Fig. 27 Frequency Spectrums

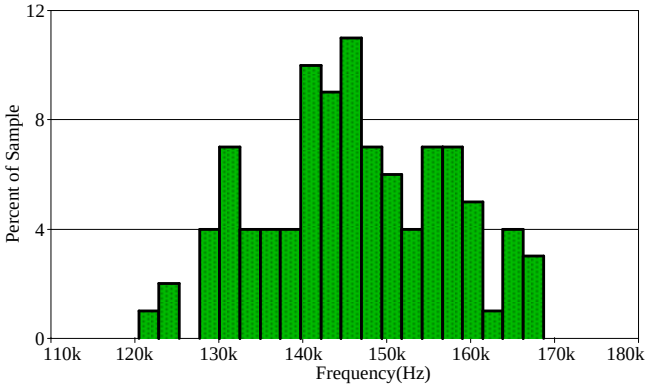


Fig. 28 Histogram of frequency of oscillation

The experimental sinusoidal oscillator was also carried out using the same approach as the simulation. The sinusoidal waveforms shown in Fig. 29 were measured using a Keysight DSOX3024T oscilloscope at a frequency of 154.81 kHz. The theoretical and experimental frequencies were within about 2.72% of an absolute error. This frequency inaccuracy is caused by tolerance errors in the passive elements, as well as parasitic resistance and capacitance in AD830. As can be seen, the phase relationship between the sinusoidal signals V_{O1} and V_{O2} is about 90.64 degrees, which is close to Eq. (21). Furthermore, the amplitude of the sinusoidal waveforms is similar, as described in Eq. (22). The frequency spectrum of V_{O1} is shown in Fig. 30. It is found the THD is approximately 0.28%. Additionally, Fig. 31 depicts the frequency spectrum of V_{O2}, with a THD of approximately 0.44 %. As demonstrated in Fig. 32, the oscillation frequency can be plotted with respect to the change in resistance R, which is similar to the theoretical analysis in Eq. (19).

VI. Conclusions

The reconfigurable multifunction of a first-order filter is presented in this study. The proposed circuit was constructed using two DDAs, one resistor, and one grounded capacitor. The AD830 of Analog Devices Ltd. is a commercially available IC that is used as the DDA. The first-order filtering functions, low-pass, high-pass, inverting all-pass, and non-inverting all-pass filters were completely performed by applying input signals to the input voltage nodes of the filter. The resistor or capacitor values were used to determine the control of the pole frequency and phase shift. Moreover, the input and output impedances of the circuit are low and high, respectively, indicating that it is completely operational in the voltage-mode. The sinusoidal oscillator was introduced by using a first-order all-pass filter. The PSPICE program and experimental testing were used to evaluate the proposed circuit's performance. It is established that the results were particularly pleasing since they matched the theoretical prediction, which is the suitability used to learn or practice in electrical and electronics engineering.

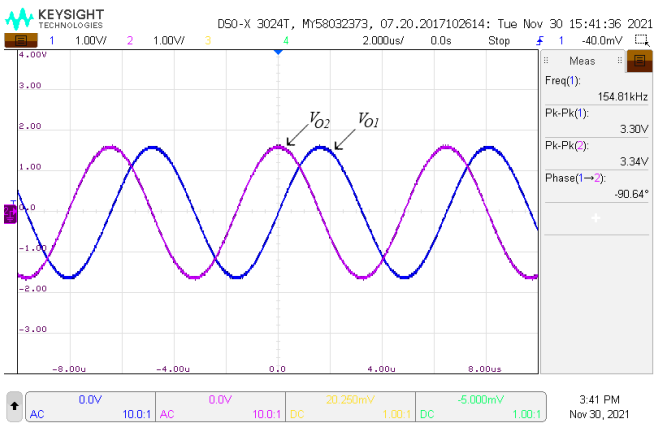


Fig. 29. The sinusoidal waveforms of outputs

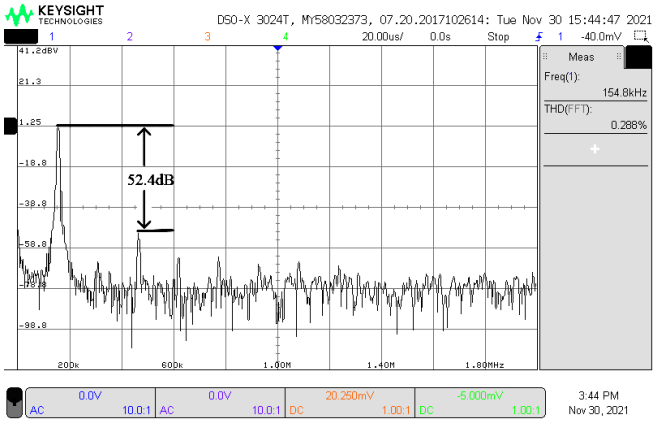


Fig. 30. The frequency spectrum of V_{O1}

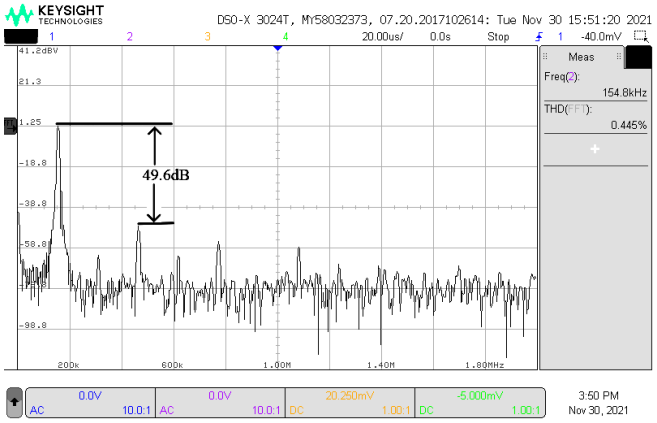


Fig. 31. The frequency spectrum of V_{O2}

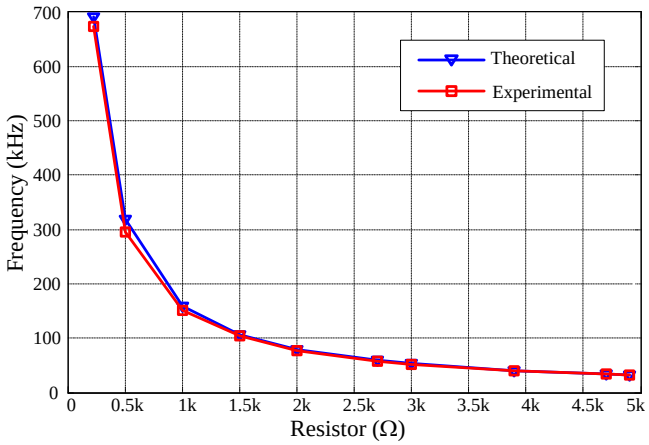


Fig. 32. The oscillation frequency vs resistance R

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