Energy-Efficient FinFET SRAM Design for In-Memory Computing Applications

Deepak Garg*, Rupali Singh and Pankaj Singh

Abstract— **In today's era, lifespan of batteries drops quickly as the power usage of devices improves. Reducing leakage current ($I_{Leakage}$) during integrated circuit design is crucial, despite the exponential growth in demand for low-power devices. FinFET solves this problem by enhancing challenging power versus performance choices. This study recommends using self-controllable voltage-level approaches to create FinFET-based 7-transistor SRAM cells. An SVL circuit can reduce an SRAM cell's standby leakage power. There are two methods, one of which raises the ground potential and the other lowers the supply voltage. The design given gets a minimum power of 24.29 nW and a low leakage current of 9.46 nA by using both USVL and LSVL techniques together. The proposed SRAM cell design saves 10% in power and 31% in leakage compared to SRAM cells made with USVL and LVSL cells, respectively using Cadence Virtuoso software on a 45 nm FinFET process technology.**

Index Terms—**FinFET, LSVL, SRAM, Leakage, USVL, Memory**

I. Introduction

Concerns about the power absorption of portable devices functioning with battery cells have been emphasized by the increase in integrated circuit density and operation frequency brought about by the progress of nanoscale process technology. Power consumption is significant for non-portable equipment due to increased packing costs, cooling requirements, and potential reliability concerns. The primary aim of this circuit design is to achieve performance targets for circuit design engineers while adhering to a low-priced power. Currently, semiconductor memories are the most frequently utilized electronic components in digital structures. In comparison to alternative storage types, semiconductor memories exhibit significantly quicker access times; read/write operations often require merely some nanoseconds. When channel widths are less than 65 nm [1], CMOS technology has been very helpful in solving hard problems like gate-induced drain lowering and threshold leakage current.

Currently, FinFET design technology is mentioned by the noble tri-gate structural design, and it has verified enhanced scalability. Circuit designers face considerable challenges in developing the circuit designs that effectively leverage this advanced technology. The primary elements influencing the IC's industry include price, power consumption, area, concert parameters, and time to market. The design specifications remain consistent over time. With each new process node, design teams strive to develop products that improve in quality, deliver more quickly, and produce at a lower cost. The shift to smaller sizes in the industry might encounter problems because smaller features can lead to more leakage current from short-channel effects (SCEs) and changes in dopant levels. The FinFET design offers important benefits for the future of semiconductor device design by overcoming the challenges of making devices smaller and reducing short-channel effects that are common in today's flat transistor designs. Reputable foundries assess that the additional processing price for 3-D devices is approximately 2–5% higher than the cost associated with fabricating a comparable planar wafer. FinFETs demonstrate operational speeds that exceed conventional transistors by up to 37% while simultaneously achieving a reduction in static leakage current and utilising less than 50% of their dynamic power, as per estimations [2, 3].

FinFET also reduces problematic power-performance trade-offs. The FinFET can function faster and more efficiently with an equivalent power level or reduced power compared to its planar counterpart. Design teams can now optimise power, performance, and throughput to satisfy specific functions' requirements. Therefore, multi-gate FETs are anticipated to assist with leakage and gate length scaling. FinFET appears to be the best option for the coming generation of SRAM because it can be scaled up more easily for the same gate insulator thickness, has better channel mobility, and doesn't have any random dopant fluctuation effects, all without affecting performance. We favour the use of both innovative circuit methodologies and FinFET-based technology to enhance the capacity of conventional cell SRAM. It may be better to use FinFET to make future nanoscale memory circuits because they reduce leakage current and SCEs. We can dynamically adjust the threshold voltage (VTH) of the access transistor to enhance data stability. FinFET can lower VTH variation, but some storage cells are still prone to inconsistency because they are tiny. This feature makes dense integration possible without sacrificing performance or reliability. SRAM is faster and can store more data due to its lack of need for data refresh and its inbuilt positive feedback mechanism [4].

SRAM cells are increasingly sought after due to their enhanced efficiency, which provides a wider write voltage margin and improved data stability at the lowest supply voltages. The VLSI field serves as the backbone for numerous applications, playing a crucial role in almost all electronic devices, such as cameras, cell phones, RFID

Manuscript received December 27, 2024; revised July 2, 2025.

Deepak Garg is a PhD candidate at the Department of Electronics and Communication Engineering of SRM Institute of Science and Technology, Delhi-NCR Campus, Modinagar, Ghaziabad, Uttar Pradesh-201204, INDIA (corresponding author to provide phone: +911232234308; fax: +911232234300; e-mail:deepakgarg1985@gmail.com).

Rupali Singh is an associate professor at the Department of Electronics and Communication Engineering of SRM Institute of Science and Technology, Delhi-NCR Campus, Modinagar, Ghaziabad, Uttar Pradesh-201204, INDIA (e-mail: rupalis@srmist.edu.in).

Pankaj Singh is an associate professor at the Department of Electrical and Electronics Engineering of IIMT University, Meerut, Uttar Pradesh-250001, INDIA (e-mail: singhpankaj76@gmail.com).

systems, laptops, and microsensors [5, 6].

In [7], we present the evaluation of various SRAM cells using varying transistor counts in terms of dissipated power and speed delay. In 90 nm technology, an incredibly stable 2-port 7-transistor SRAM design was made. It has a 7 µ dynamic read noise margin and uses very little power [8–11]. To sustain dynamic power, it is essential to reduce the supply voltage in light of ongoing technological advancements. During scaling, the consumption of power increases due to $I_{leakage}$.

The sub-threshold current is the primary portion contributing to the common leakage current (Ileakage). This study employs the SVL circuit, as demonstrated in previous studies [12–15], to reduce leakage in SRAM cells. The PMOS transistor acts as a switch when the SVL's semiconductors go from the sleep to active state, and the NMOS transistors are set up like resistors in series to lower $I_{Leakage}$. In backup mode, the switch can reduce the applied DC voltage to its lowest level [16]. In operational mode, the switch can increase the supply voltage to connect the highest possible DC voltage to a load. We designed the proposed SVL circuit to minimise SRAM cell backup leakage intensity while adhering to specific speeds and area limitations. We can use an SVL circuit to lower the applied voltage and enhance the ground-level performance in SRAM designs. The technique for adjusting voltage levels uses 3 distinct types of circuits: combination circuits (USVL and LSVL), LSVL load and USVL. This SVL circuit efficiently reduces standby leakage power in SRAM cells, all while having a minimal impact on speed and chip size. SRAM cells use an SVL circuit to raise the ground node potential and lower the supply voltage. Table I presents a comparative analysis of the various SRAM cells.

For in-memory computing purposes, it is crucial to minimise power dissipation, a critical aspect of memory architecture that dictates its intended application. Using the following formula, one can see how a FinFET lowers power consumption.

$$P_S = V_{DD} \times I_{leakage} \quad (1)$$

Where,

P_S = Static Power Dissipation
V_{DD} = Power Supply Voltage
$I_{Leakage}$= Leakage Current

The following is an overview of this article: Sections II and III offer a comprehensive definition of the FinFET device and go into excellent detail about how a 7T SRAM cell using FinFET technology is built and how it works, respectively. Section IV provides a comprehensive analysis of the effects of leakage current. Section V presents the self-controlled voltage level technique. In Section VI, we provide a detailed examination of the complex structures of the proposed 7T SRAM cell, which utilises FinFET technology via the SVL technique, along with an explanation of its functionality. Section VII presents an examination of the findings. The final section, Section VIII, outlines the work's conclusion and future aspects.

Table I
Comparative Analysis of the SRAM cell with different FinFETs

S. No.	Ref. No.	Authors	Power Reduction Technique	FinFETs used	Observations
1.	[17]	Rahebeh Niaraki Asli et al.	Using Back Gate Control	6	Least read power consumption
2.	[18]	Sneha et at.	Supply Voltage Scaling	7	Voltage supply is minimized; there is no requirement for RBL charging.
3.	[19]	Yang et at.	Operation NTV	7	Optimised energy consumption during NTV o peration and an effective design solution for e nhanced performance.
4.	[20]	Monica et at.	Floating of supply voltage	8	Improvement in both reading and writing capa bilities.
5.	[21]	Farkhani et al.	Supply voltage	8	During the circuit design process, the minimis ation of subthreshold swing (SS) is a key cons ideration.
6.	[22]	Kim et al.	Voltage of back gate	8	During the write operation, the activity associa ted with discharging is minimised.
7.	[11]	Ansari et at.	Operation NTV	7	Reduced write time, increased write margins, and enhanced read margins.
8.	[23]	Yang et at.	Operation NTV and yield estimation approach	9	Obtain a minimum operating voltage of 0.3 V.
9.	[24]	Moradi et at.	Multi-threshold	9	Three times reduced power intake
10.	[25]	Oh et al.	Power Gated	9	Reducing the bit cell area results in decreased energy consumption for each write and read o peration.
11.	[26]	Yadav et al.	Feedback mechanism and Biasing of back gate	10	Positive feedback enhances the stability and biasing of the back gate.
12.	[27]	Sharma et al.	Stack Architecture	8	Improve power efficiency while reducing access times.
13.	[28]	S. Birla et al.	Using SG and LP-IG mode	8	At 0.5 V, the SG and IG SRAMs had leakage powers of 12.61 nW and 8.92 nW, respectively.

II. FINFET TECHNOLOGY

Figure 1 depicts the configuration of the FinFET and planar FET devices. FinFET technology improves the controllability in low-voltage processes by incorporating a second gate positioned opposite the normal gate. A FinFET utilises both gates' functionality [29].

FinFET is referred to as a multi-gate device. FinFET operational methodology bears a strong resemblance to conventional MOSFET technology. Gate, drain, and source terminals equip FinFET to regulate current motion.

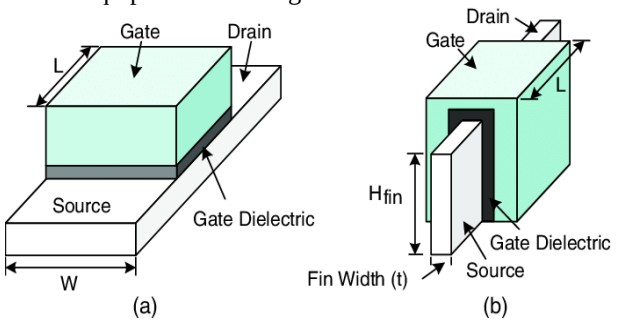

Fig 1: FET Structure (a) Planar (b) Fin.

The conducted channel located in-between the drain and source of a FinFET serves as the distinguishing characteristic that sets it apart from a MOSFET. A "fin" is a 3-D device structure that corresponds to the design of the FinFET channel located on the above section of the silicon bulk. In Figure 2, you can see that the 3-D bar design surrounds the FinFET gate around the channel, creating multiple gate electrodes on both sides. The implementation of these electrodes has the potential to enhance driving current while reducing leakage effects. As per the design framework, the fin height of a single-fin FinFET must be 50% of the channel width (W_{eff}). Also, FinFET technology can deliver stronger drive currents for the same area than traditional flat devices, as long as the effective width (W_{eff}) is big enough to fit several fins side by side. The effective width of a FinFET is determined by equation (2).

$$W_{EFF} = N_{FIN} X (T_{FIN} + 2H_{FIN}) \quad (2)$$

A gate encases the thin, vertically orientated, fin-shaped channel in the FinFET architecture, which facilitates current flow and regulates electron movement. Compared to traditional planar MOSFETs, the vertical architecture makes it easier to control the flow of electrons, which leads to better performance and efficiency.

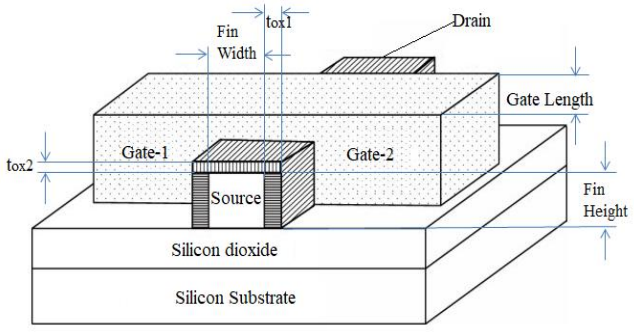

Fig 2: FinFET Structure.

The DG FinFET is called a single-gate design because its fin's width (W_{Fin}) is much larger than its height (H_{Fin}), and the gate oxides on the sidewalls are significantly thicker than those on top. Figure 3 illustrates the two-dimensional structure of a FinFET. The FinFET architecture is generally constructed on a semiconductor substrate commonly composed of silicon. FinFET is characterised by its unique thin, vertical, fin-shaped channel, which functions as the conductor for current flow. Typically composed of silicon material, the fin extends from the substrate. The dimensions of the fin, including height and width, may differ based on the particular manufacturing process and design specifications. The gate, composed of a dielectric material like silicon dioxide (SiO_2), encircles the fin. The gate electrode regulates the current flow through the fin by establishing an electric field. The drain and source regions at both ends of the fin are heavily doped with impurities. This procedure makes it easier for charge carriers (like electrons and holes) to move into and out of the channel. A thin layer of gate dielectric material is positioned beneath the gate electrode, serving to isolate the gate electrically from the channel. Gate dielectrics are usually made up of high-k dielectrics and SiO_2 (silicon dioxide), which has high dielectric constants to keep gate Ileakage to a minimum. Spacer materials serve the purpose of creating a separation between the drain/source and the gate electrode regions. The spacers serve to regulate the gate width and channel length, thereby affecting the performance characteristics of the transistor.

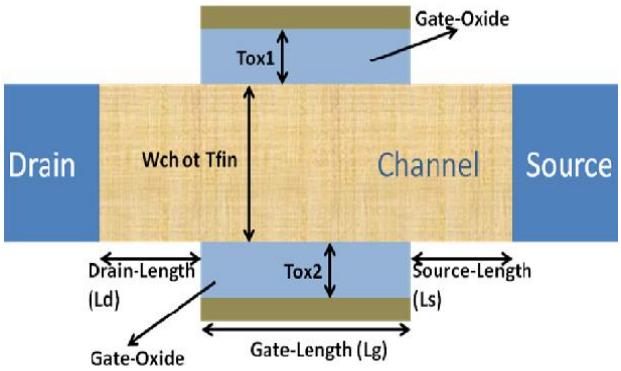

Fig 3: Two-dimensional structure of FinFET.

FinFETs can be categorised into two main types based on their gate configuration: SG (shorted-gate) and IG (independent-gate).

(i) Shorted-Gate: In the shorted-gate FinFET, the two gates on either side of the fin are electrically connected, functioning as a single gate. This configuration provides strong electrostatic control over the channel, reducing leakage currents and improving the device's performance. By tying the gates together, the shorted-gate FinFET minimizes variability and ensures more uniform operation, making it ideal for high-performance and low-power uses. SG functions as a three-terminal device. Figure 4(a) illustrates the structure of the SG FinFET. Both gates in SG FinFET concurrently regulate the electrostatic characteristics of the channel. When Compared to IG FinFETs, Shorted-Gate FinFETs exhibit a higher on-current (I_{on}) and a higher off-current (I_{off}). This structure is widely used in advanced semiconductor designs because it enhances drive current while maintaining excellent control over short-channel effects, which are critical for scaling down transistor dimensions in modern integrated circuits.

(ii) Independent gate: An independent-gate FinFET has four terminals. The two gates on either side of the fin are electrically isolated and can be controlled separately. Figure 4(b) illustrates the symbol of the SG FinFET. The Independent-Gate FinFET exhibits greater flexibility compared to the SG FinFET.

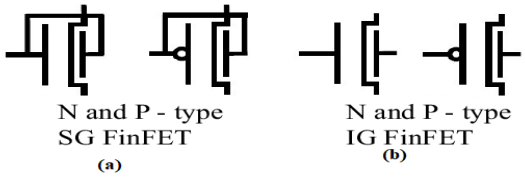

Fig 4: FinFET device symbol.

A voltage difference between the two gates initiates an operation known as IG. The function of the rest gate is to switch components and control the transistor's threshold voltage, V_{TH} [30–31]. It allows the two gates to operate separately, offering greater flexibility for circuit design and enabling innovative applications such as multi-threshold voltage operation or dynamic control of the transistor. These structural variations provide designers with options to optimize devices for specific performance or power requirements, making FinFET an integral component of advanced semiconductor technologies.

III. SRAM Cell Design utilizing FinFET

An SRAM cell generally consists of a pair of cross-coupled inverters, commonly referred to as a flip-flop or latch, together with dual access transistors. These access transistors regulate write and read operations by permitting external signals to interact with the stored data. The cross-coupled inverters provide a bistable circuit, allowing the cell to retain one bit of data in a stable condition. During operation, the access transistors manage the link between the SRAM cell and external circuitry to facilitate reading and writing. The functionality of SRAM is defined by its behaviour during various phases, such as read, write, and standby modes.

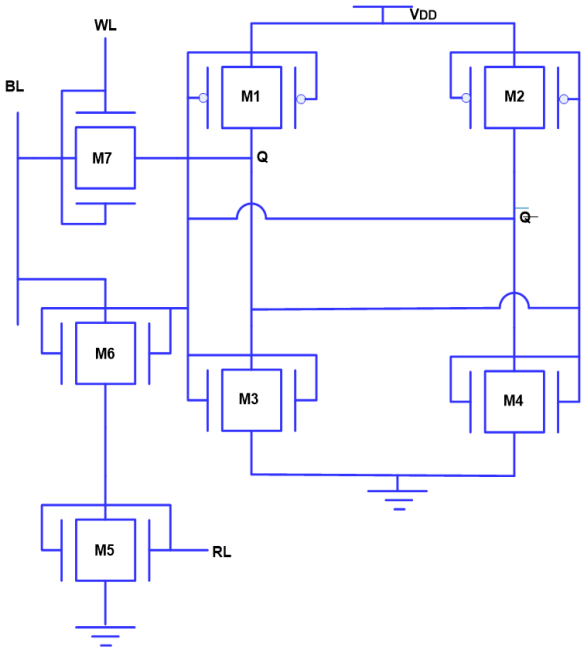

Fig 5: 7T FinFET based SRAM Cell

Figure 5 illustrates a 7T SRAM cell using FinFET technology. This SRAM cell comprises a total of seven transistors, consisting of two P-type FinFETs and five N-type FinFETs. The SRAM cell presented uses double-cross-coupled inverters and double-access transistors, both constructed with FinFET devices. The SRAM cell consists of two sets of cross-coupled inverters, utilizing a total of four transistors (M1, M4, M3, and M2). These four transistors store each bit. The suggested design incorporates a total of seven transistors. For the normal device, four transistors work like the normal one, and the fifth transistor controls the device so that M5 and M6 are switched on while M7 is turned off during read mode. Transistor M5 deactivates in write mode, resulting in a reduction in power consumption [32-33].

Write Operation: The feedback connection between the cross-coupled inverters is used to control the writing operation. This approach necessitates only one transistor pair, with data fluctuations occurring based on the activation state of M2. The reading procedure transpires when both the RL and the bit line (BL) are activated. This operation transpires when the M7 and M6 (access transistors) maintain the word line (WL).

Read Operation: This procedure employs a single transistor pair, where the activation or deactivation of M2 determines the increase or decrease in data levels. The read process is initiated when BL and RL, both lines, are activated.

Hold Operation: During this state, transistors M3 and M4 function as OFF-inverter transistors, providing mutual support to maintain data for an extended period. Consequently, there is no link between the BL, word line and WL with the cross-coupled devices during this phase [34-35].

In an alternative operating state, the power reduction of a 7-transistor SRAM cell is decreased to 50% of that observed in a normal SRAM cell, as it uses only one bit line [36-38]. All three operations of the 7T SRAM cell using FinFET technology is summarized as Figure 6.

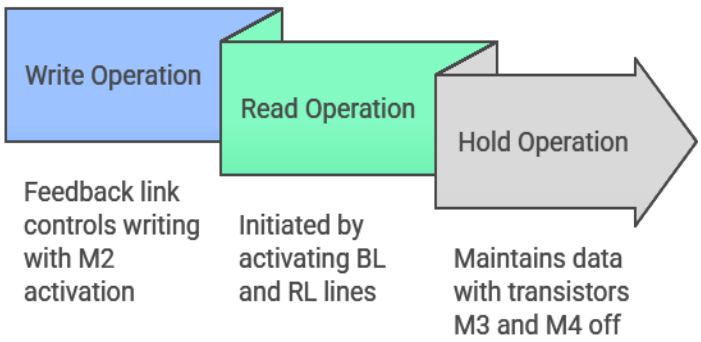

Fig 6: FinFET Operations.

Figure 7 displays the 7T SRAM cell's simulated read waveforms [39]. We have carried out a single-ended procedure. We apply a pulsed input at the Q node and measure the output at BL. For this operation, WL is maintained at LOW and RL at HIGH.

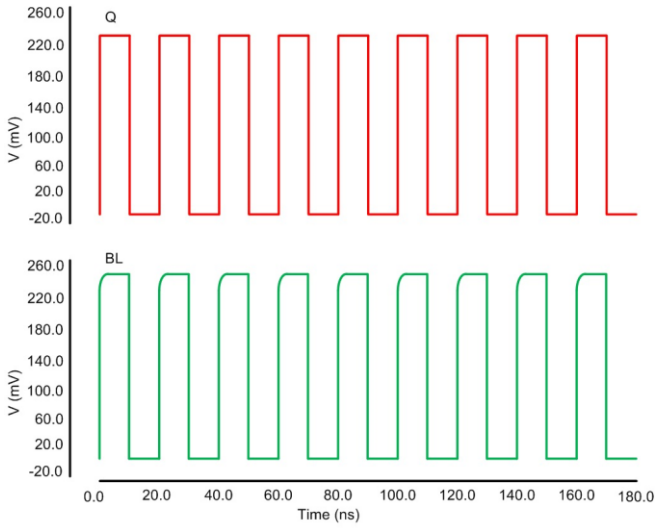

Fig. 7: Read operation 7T SRAM

Figure 8 displays the 7T SRAM cells' simulated write waveforms [39]. We have carried out a single-ended procedure. At the BL node, a pulsed input is applied, and output is measured from Q and $\overline{Q}$. For this operation, WL is maintained at HIGH and RL at LOW. The read, hold, write "0", and write "1" SNM processes of the 7-transistor SRAM design using FinFET are shown in Figure 9 (a-d). Compared to conventional SRAM, the read processes in the proposed SRAM are better. The hold process in FinFET-based SRAM is described by the curve in Figure 9(b). As seen in Figures 9 (c & d), the write 0 and 1 process in SRAM design using FinFET has better SNM as conventional SRAM design. Therefore, the suggested FinFET SRAM design offers the best hold, write, and read characteristics with a high Static Noise Margin value while consuming less static and dynamic power. A square box is fitted into the curve to find the SNM value of various processes.

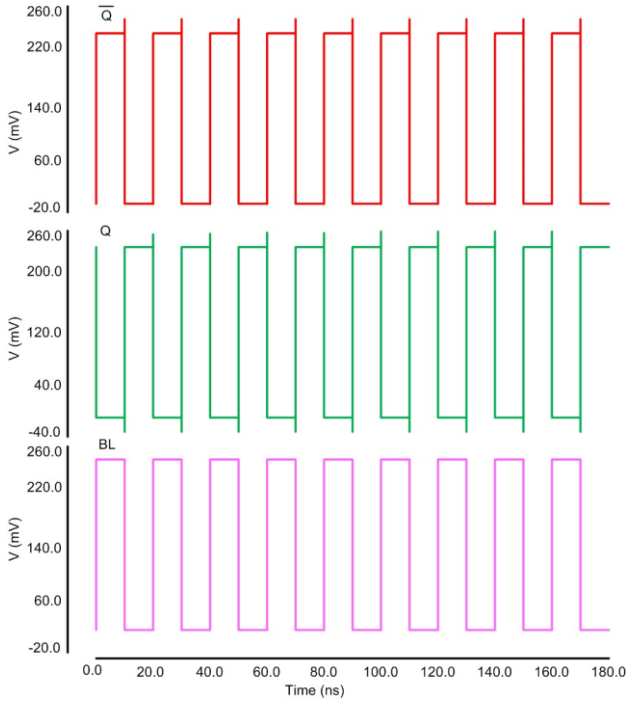

Fig. 8: Write operation 7T SRAM

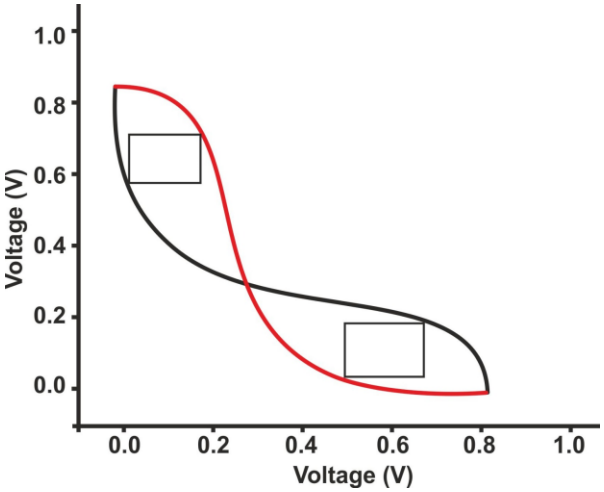

Fig. 9 (a): Read SNM Process

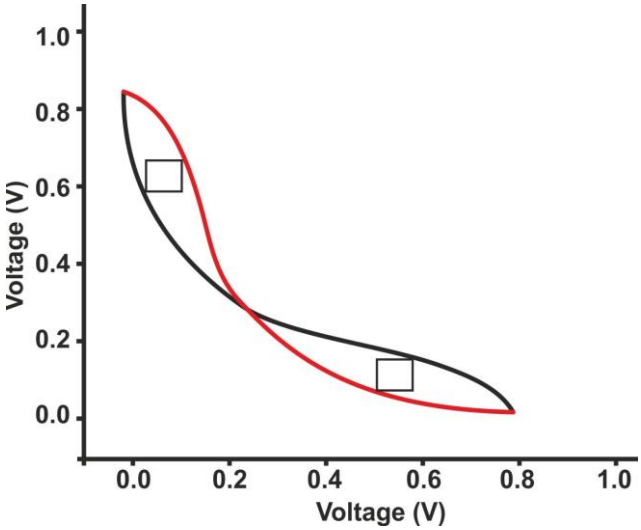

Fig. 9 (b): Hold SNM Process

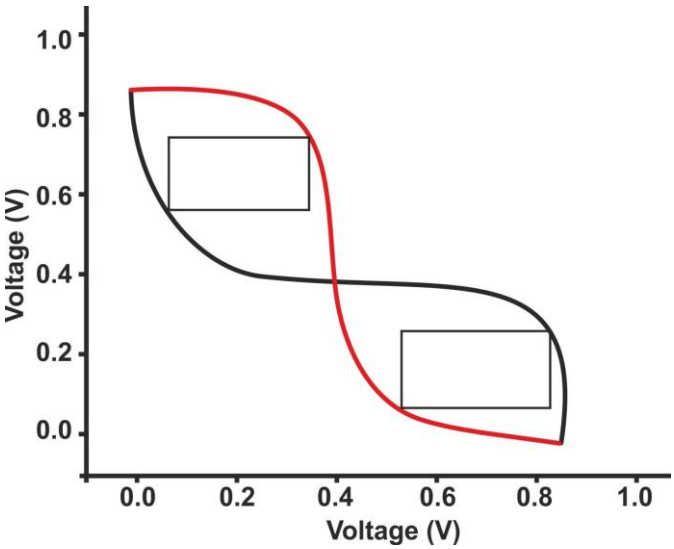

Fig. 9 (c): Write '0' SNM Process

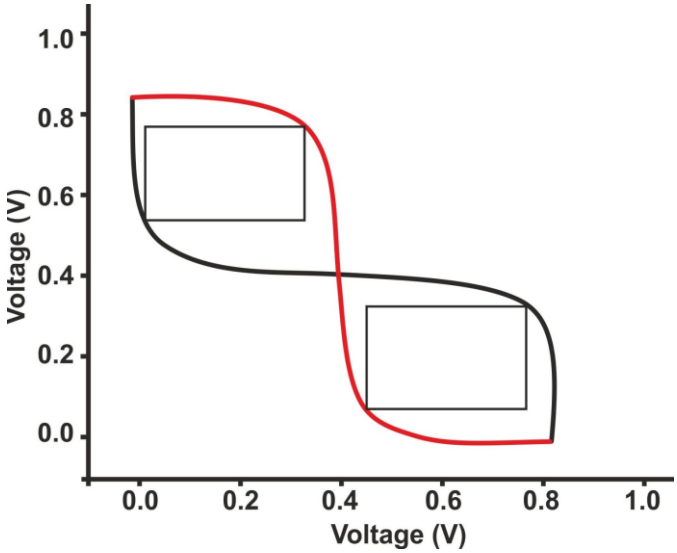

Fig. 9 (d): Write '1' SNM Process

IV. Effect of Leakage Current

Leakage current is a big problem for CMOS (Complementary Metal-Oxide-Semiconductor) technology, particularly as transistor sizes continue to shrink in advanced nanometre-scale designs. It refers to the unintended flow of current in a transistor when it is in the off state, leading to increased static power dissipation. This leakage happens because of different reasons, such as sub-threshold leakage, gate oxide leakage, and junction leakage, and it becomes more significant as devices get smaller and supply voltages drop. The effect of Ileakage is particularly concerning in battery-operated and low-power applications, as it leads to higher power consumption, reduced battery life, and increased heat generation, which can degrade circuit reliability. Additionally, too much leakage can cause differences in performance and affect how well high-density integrated circuits (ICs) work, making it important to use power management methods in today's CMOS designs. To mitigate leakage current, various techniques such as threshold voltage scaling, power gating, and self-voltage level (SVL) approaches are employed to enhance energy efficiency and circuit stability. Figure 10 illustrates all three main causes of leakage current.

Subthreshold Leakage: Subthreshold $I_{leakage}$ is a main contributor to leakage power dissipation in modern CMOS technology, especially as transistor sizes shrink in deep-submicron and nanometer-scale circuits. It occurs when a small drain current flows even though the transistor is in the off state, due to the occurrence of a weak inversion layer in the channel. Sub-threshold leakage refers to the drain-source current (Ids) of a transistor that arises when Vgs is below VTH [40]. In the sub-threshold regime, the drain current exhibits an exponential dependence on Vgs. Equation (2) yields the drain current. The $I_{leakage}$ denotes the unintended motion of current that transpires when the transistor is intended to be in the off state. This leakage occurs owing to numerous processes and can result in heightened power absorption, diminished battery lifetime in portable devices, and impaired reliability in ICs. The effects of subthreshold leakage include more power use, shorter battery life in portable devices, and more heat, which can lower the reliability of integrated circuits (ICs). As technology scales down, controlling subthreshold leakage becomes a major design challenge.

$$I_d \alpha \exp\left(\frac{V_{gs}}{n V_T}\right) \quad (3)$$

$$N = 1 + \frac{C_D}{C_{OX}} \quad (4)$$

Gate Leakage: Gate leakage current is a considerable concern in MOS technology, particularly as transistor dimensions shrink to deep-submicron and nanometre-scale levels. It occurs due to tunnelling of electrons through the ultra-thin gate oxide layer, which leads to unintended I $I_{leakage}$ even when the transistor is in the off state. As the gate oxide gets thinner to make transistors work better, quantum mechanical tunnelling effects become stronger, causing more static power use and more heat. The effects of gate leakage include reduced battery lifetime in portable devices, degraded circuit reliability, and potential failure of high-speed integrated circuits (ICs). Furthermore, excessive gate leakage leads to signal integrity issues, impacting the overall performance and lifespan of electronic systems. FinFET-based transistor designs employ gate leakage mitigation to enhance energy efficiency and circuit stability. Addressing gate leakage is crucial in modern low-power and high-performance applications, ensuring reliable operation and prolonged device lifespan [41].

Junction Tunnelling Leakage: Junction tunnelling leakage is a significant concern as device dimensions shrink to deep-submicron and nanometre-scale levels. This type of leakage occurs due to the tunnelling of charge carriers across reverse-biased transistors. When transistor sizes get smaller and doping concentrations rise, the depletion width at the junctions gets minimal. This results in stronger quantum mechanical tunnelling effects and an increase in leakage current. The relationship between junction doping and reverse bias voltages is exponential [14].

Junction leakage minimally affects the overall leakage current. FinFET technology employs mitigation of junction tunnelling leakage to enhance energy efficiency and circuit stability. Designers employ various techniques to minimize leakage currents in FinFET circuits, such as optimizing transistor doping profiles, adjusting threshold voltage, implementing power gating, and scaling gate length.

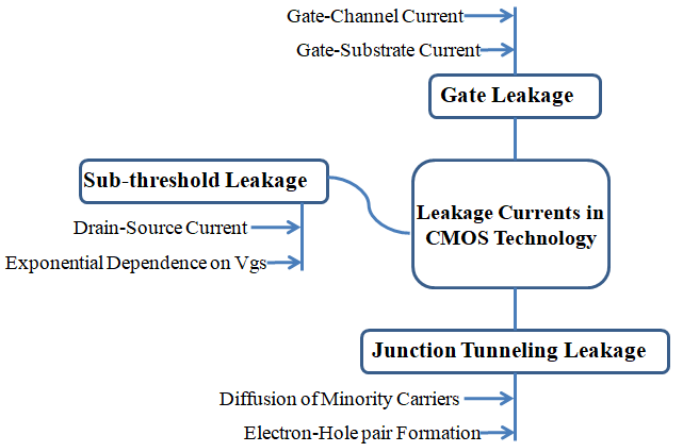

Fig 10: Leakage Currents understanding in CMOS technology.

V. Self-controllable Voltage Level Approach (SVL)

In semiconductor design and integrated circuit fabrication, the SVL method is used to make sure that

voltage levels in a circuit are always at the right level. We refer to this method as dynamic voltage and frequency scaling (DVFS). This procedure suggests a manner in which a system or component independently regulates its voltage level. This method may incorporate self-regulation mechanisms, potentially using internal sensors or feedback loops. This would enable the system to dynamically adjust its voltage level according to its operating conditions. This methodology serves as a power management strategy that is especially effective in situations characterised by fluctuations in supply voltage, temperature, process variations, or load conditions.

The SVL technique serves as an efficient methodology for enhancing the performance and power efficiency of ICs. This is particularly relevant in contemporary semiconductor designs, where energy efficiency is a paramount factor. The following outline summarises the features or characteristics of the SVL technique: The SVL method lets the system keep its self-controlling abilities, so it can check its own working conditions and change the voltage level as needed without any help from outside sources. The system may include feedback mechanisms designed to monitor parameters including workload, current, temperature and voltage. The measurements may provide guidance for making adjustments to the voltage level. The primary aim of the method is to improve energy efficiency by operating at the lowermost viable voltage level, ensuring that performance requirements are still met. The method aims to optimise execution by dynamically adjusting the voltage level to align with workload demands, ensuring adequate resources are available and reducing power consumption. This methodology may include mechanisms designed to enhance fault tolerance and system reliability, such as fallback strategies and error detection and correction mechanisms. The SVL method is classified into two main types: the upper and the lower SVL methods.

(i) Upper SVL circuit: Figure 11 (a) illustrates the USVL method. As the width of the transistor increases, the impedance of a MOS transistor also increases. The wide FinFET M1 in the circuit results in a significantly high resistance in the pathway between V_{DD} and VD. Consequently, the leakage in this SVL mode is minimal. Furthermore, the combination of transistor M2 and M3 facilitates the cell's standard operational state. In the active mode, FinFET M3 operates like a resistor to decrease current flow. Additionally, the aforementioned connection manner minimises leakage.

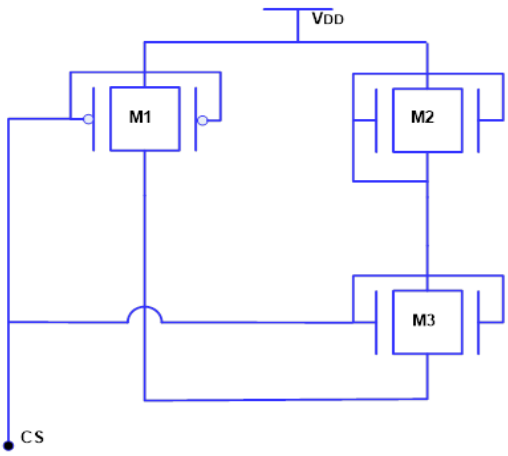

Fig 11(a): USVL circuit

(ii) Lower SVL circuit: Figure 11 (b) illustrates the LSVL method. The cell operates in the standard mode for FinFET M2 and FinFET M3, while transistor M1 operates in the SVL state. Transistor M2 minimizes leakage by behaves as a resistor.

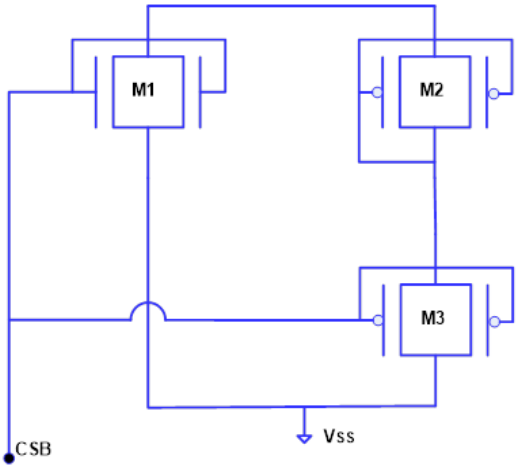

Fig 11(b): LSVL circuit

The operation of an SRAM utilizing FinFET technology is detailed in Table II.

Table II
SRAM Cell: SVL Operations

Mode	USVL Circuit	LSVL Circuit
Active	The PMOS switch is in the ON state.	The NMOS switch is in the ON state.
	The V_{DD} is now accessible.	The V_{SS} is now accessible.
Stand-by mode	The NMOS switch is in the ON state.	The PMOS switch is in the ON state.
	The V_{DD} (>V_D) is now accessible.	The V_{SS} (<V_S) is now accessible.

Advantages of SVL Technique over other Techniques

This technique provides several benefits compared to alternative methods for reducing leakage current, including:

i. Decrees Power Consumption: SVL permits the system to adjust its frequency and operating voltage in response to workload requirements. Reducing the frequency and voltage during low activity or idle states can lead to a substantial decrease in the system's power consumption. This results in enhanced energy efficiency and extended battery lifespan.

ii. Improved Thermal Management: DVFS works well to keep electronic systems from getting too hot by lowering the operating voltage and frequency when there isn't much going on. In high-execution computing applications, the significance of thermal management is paramount for ensuring system reliability and longevity. Effective management of thermal problems enables self-controllable voltage levels to prevent overheating and thermal throttling, which enhances system reliability and execution.

iii. No Need for Additional Power Gating – Some conventional methods, such as power gating, require extra transistors or sleep modes that can introduce wake-up delays. SVL mitigates leakage without requiring additional complex switching.

iv. Reduced Dependence on High-VTH Transistors – Many leakage reduction techniques rely on high-threshold

voltage (VTH) transistors, which may degrade performance. SVL achieves power reduction without heavily relying on high-VTH devices.

v. Dynamic Performance Optimisation: SVL enables the system to adjust its operating characteristics in real time, responding to varying workload demands and operating conditions. Enhancing the voltage and frequency when there is a lot of computing demand makes the system work better, making sure that it responds quickly and gets a lot of work done. By reducing the voltage and frequency during low-activity periods, the system achieves energy conservation while maintaining performance levels.

vi. Compatibility with Multiple Operating Modes: Active mode, standby mode, and sleep mode are only a few of the various operating modes that many contemporary electronic systems enable, each with varying performance and power needs. To optimise power consumption and performance across the whole system operation range, SVL can be combined with various operating modes.

vii. Lower Implementation Cost – Compared to multi-threshold CMOS or body biasing techniques, SVL offers a cost-effective alternative due to its simpler design and fewer fabrication modifications.

viii. Lower Design Complexity – Compared to techniques like adaptive body biasing or power gating, SVL offers a simpler design methodology, reducing circuit complexity and ease of integration.

VI. Design of a 7T SRAM cell using FinFET with the SVL Approach

To conserve power while maintaining high-speed performance, various strategies are employed. The SVL technique serves as a valuable method for enhancing high-speed performance. This method is capable of reducing the supply voltage to a load when in standby mode or permitting the use of maximum DC voltage to an active load. The design and analysis of a 7T SRAM cell using FinFET technology incorporates all three varieties of SVL circuits. The varieties include USVL, LSVL, and a hybrid of upper and lower SVL circuit designs. Table III provides the details pertaining to the FinFET dimensions [41].

Table III
FinFET Dimension Information

S. No.	Parameter	Value
1	Source diffusion periphery	521 nm
2	Source–drain metal width	60 nm
3	Source diffusion area	16.8 f
4	Channel Length	45 nm
5	Drain diffusion periphery	520 nm
6	Drain diffusion res square	1.1667
7	Gate spacing	160 nm
8	Channel Width	120 nm
9	Source diffusion res square	1.1667
10	Right source/drain length (SB)	140 nm
11	Drain diffusion area	16.8 f
12	Finger Width	120 nm
13	Left source/drain length (SA)	140 nm

The Design flow graph for the achieving optimal SRAM cell design using SVL technique is shown in Figure 12.

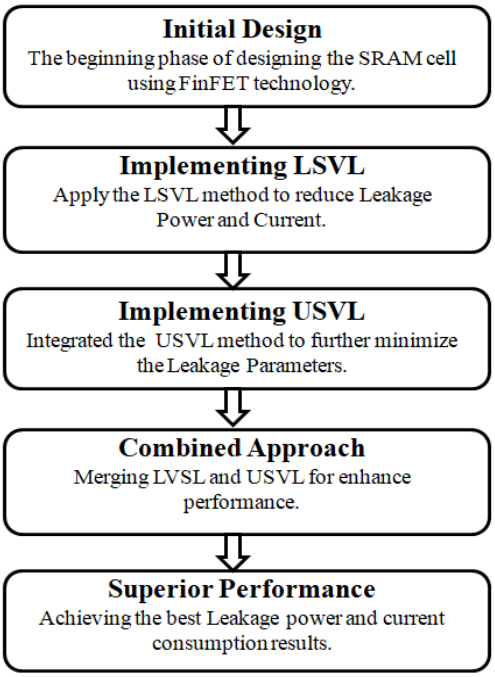

Fig 12: Design flow for achieving optimal SRAM design

A. 7T SRAM Cell Design using Upper SVL Approach

The Seven-Transistor SRAM design using the upper SVL approach is a valuable method for reducing leakage power while maintaining performance. In this design, the upper SVL circuit is integrated into the power supply path of the SRAM cell, dynamically controlling the supply voltage to minimise leakage current. Unlike conventional SRAM designs, which suffer from high leakage power in standby mode, the upper SVL technique helps in reducing static power dissipation without significantly impacting access speed. This approach selectively lowers the supply voltage during idle states, thereby achieving a balance between power savings and data retention. The implementation of the upper SVL method in the 7T SRAM design further enhances energy efficiency, making it highly beneficial for portable, battery-operated, and high-performance computing devices.

Figure 13 illustrates the SRAM cell using FinFET technology and the USVL technique. Two n-channel type FinFET transistors (which work as resistors) are operated in series with a single p-channel type FinFET transistor (which works as a switch) to make the USVL circuit. FinFET technology interfaces the USVL circuit between the power supply VDD and the 7T SRAM cell. As shown in Figure 13, the CS signal functions as a control signal for the USVL circuit. Upon request, the ON P-channel type FinFET transistor connects to V_{DD} and a 7T SRAM cell, utilising FinFET technology in active mode. Similarly, we connect the ON N-channel type FinFET transistor to VDD and a 7T SRAM cell that uses FinFET technology in standby mode. This procedure entails the application of the full supply voltage (V_{DD}) to the 7T SRAM cell using FinFET technology during active mode while reducing the voltage level (VD) during sleep mode (standby mode). To conserve energy and maintain optimal performance, various strategies are employed. The SVL technique serves as an effective method for enhancing high-speed performance. This method is capable of reducing the applied voltage to a load during standby state or enabling the application of peak DC voltage to an active load.

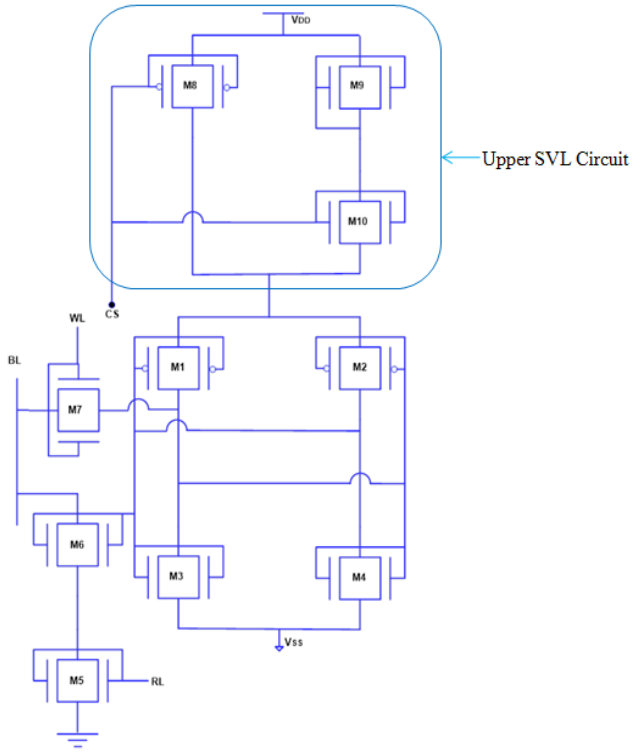

Fig 13: 7T FinFET based SRAM cell utilizing USVL Technique

The simulations show that when the gate voltage on transistor FinFET M6 is lowered, the leakage gate current that flows through the device also decreases. When the channel voltage of FinFET M3 goes down, the gate leakage current also goes down. This causes the gate channel voltage across transistor M4 to go down. The leakage gate current of FinFET M1 is consistent and shows no variation. The USVL circuit-based p-channel type FinFET M8 exhibits minimal leakage current characteristics. The leakage current is consistent across FinFET M1, while the USVL method decreases the sub-edge leakage current in transistors M2 and M3. The gate leakage currents in Access FinFETs M7 and M6 remain constant when utilising the USVL method. This method reduces gate leakage current, thereby minimising all subthreshold currents. In conclusion, the USVL technique works better at lowering the leakage gate current in access transistors, but it doesn't change two parts of the gate leakage current. Furthermore, it generates an additional sub-threshold leakage current through the access transistor while preserving one sub-threshold current component within it [42].

B. 7T SRAM Cell Design using Lower SVL Approach

The seven-transistor static random-access memory using the lower SVL approach is an efficient technique for reducing leakage power while maintaining reliable data retention. In this method, the lower SVL circuit is connected in the ground path of the SRAM design, dynamically controlling the voltage level to reduce sub-threshold leakage current. The 7T architecture provides enhanced read stability and better noise margin**,** making it more appropriate for low-power and energy-efficient uses. The integration of the Lower SVL technique in 7T SRAM design ensures improved power efficiency, making it highly beneficial for battery-powered, portable, and high-performance computing devices.

Figure 14 illustrates the SRAM cell that incorporates FinFET technology and utilises the USVL technique. There is one n-channel type FinFET transistor (which acts as a switch) connected in series with two p-channel type FinFET transistors (which act as resistors). FinFET technology interfaces the lower SVL circuit between a VSS and a 7T SRAM design. As shown in Figure 14, the CSB signal functions as a control signal for the lower SVL circuit. In active mode, a control signal provides a voltage of 0 volts, whereas in standby mode, the ground voltage is increased.

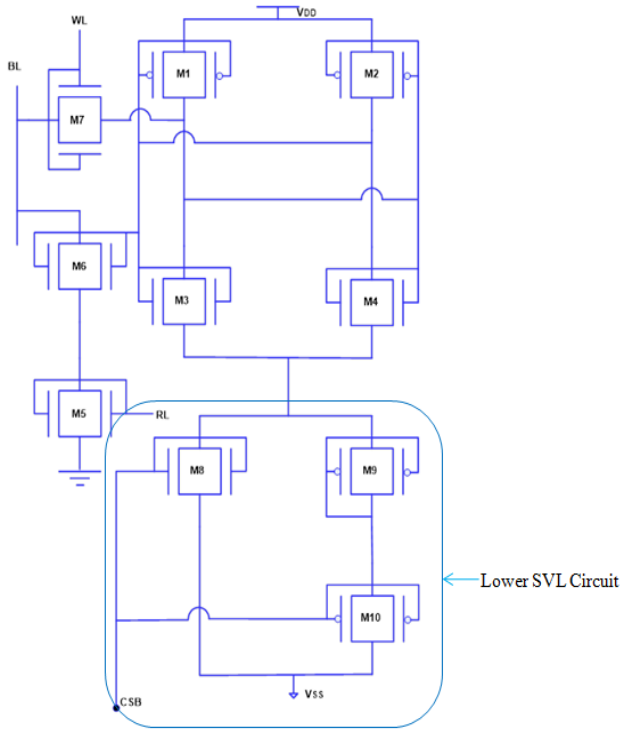

Fig 14: 7T FinFET based SRAM cell utilizing LSVL technique

The M8 transistor is used to provide VSS to the 7T SRAM cell in a lower SVL circuit. This shows the VSS received by M10 and M9 transistors to turn on the remaining 7T SRAM cell. In the lower SVL circuit (VSS=0 volts), it enables the FinFET transistors M10, which is controlled by the control signal (CSB). With the CSB switch in dynamic mode, the output is at ground level [0 V], and the output reflects a higher virtual ground when idle. The leakage flows in transistors M2, M3 and M7 are significantly minimised by applying the LSVL technique successfully. This measure suppresses gate leakage current and in turn reduces all sub-threshold currents. This approach mirrors the diode-footed store structure concept suggested in [43], aimed at mitigating sub-edge leakages and managing control signals within a 7T SRAM cell utilising FinFET technology.

C. 7T SRAM Cell Design using both (Lower + Upper) SVL Approach

The integration of USVL and LSVL approaches in a 7T FinFET-based SRAM cell necessitates the management of voltage levels within the cell. This approach is essential for maintaining reliable operation across diverse conditions and enhancing power efficiency. Regular monitoring starts changes to make sure voltage levels stay within certain

ranges, which stops both over-voltage and under-voltage situations from happening. The integrated method is designed to safeguard the SRAM cell against voltage fluctuations that may result in data loss, instability, or potential damage. Implementing proactive control of both upper and lower voltage limits improves longevity, data retention and reliability.

Figure 15 illustrates the circuit arrangement using a combined SVL approach. This approach involves connecting the lower SVL circuit between V_{SS} and the 7T SRAM cell, while the upper SVL circuit is linked between V_{DD} and the same 7T SRAM design, as illustrated in Figure 11. As illustrated in Figure 15, the CSB and CS signals function as control signals for the USVL and LSVL circuits, respectively.

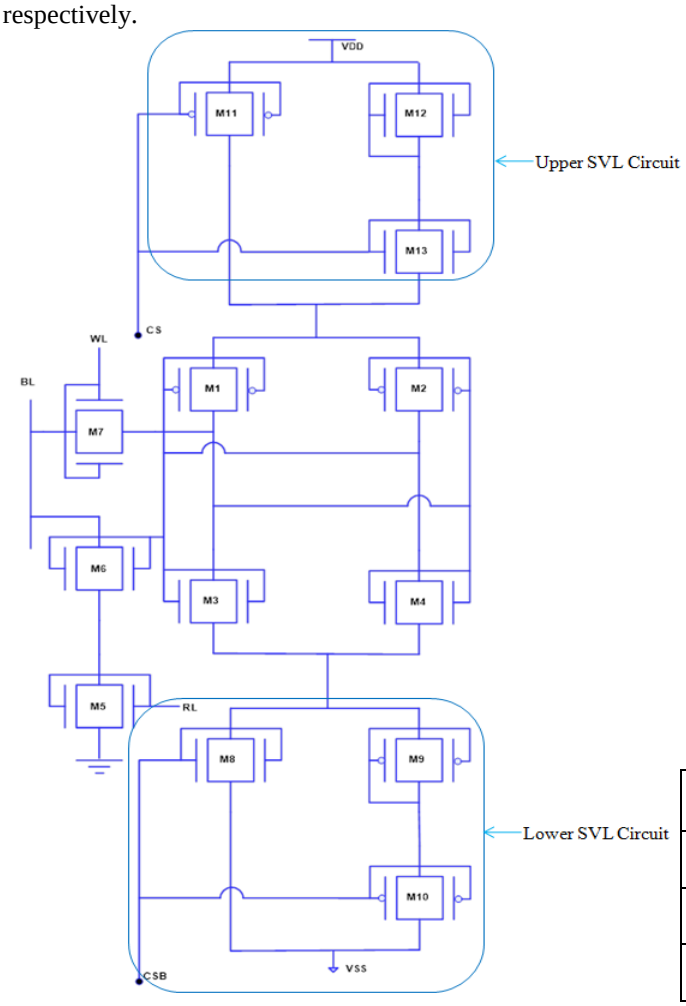

Fig 15: 7T FinFET based SRAM cell utilizing combined Techniques

As shown in Figure 15, a control signal connects the three transistors (M9, M10, and M8) between Vss and 7 T-SRAM cells. The system establishes a virtual ground and a ground potential in both active and idle modes, contingent upon the value of the control signal. As an outcome, we can minimise the leakage across the M3, M2, and M7 transistors. Consequently, reducing gate leakage can lead to a decrease in sub-threshold currents in this context. The 7T SRAM and V_{DD} configuration integrate three supplementary transistors. Transistor M5 is responsible for delivering V_{DD} to the 7T SRAM during dynamic operation, whereas transistor M8 is tasked with supplying V_{DD} during idle conditions. Utilising the triple transistors located at the upper section, leakage can be minimised through the reaming of transistors M1, M4, and M5. This approach results in a reduction of V_{DD} to 50% of its supply level, while the ground potential experiences a 25% increase.

The implementation of the mixing SVL technique results in an increase of Vss to 0.25 V while concurrently decreasing VDD to 0.35 V. The combined SVL technique works better than the individual (LSVL or USVL) SVL techniques because it cuts down on leakage power and current use by a large amount [41, 44].

VII. Result Analysis

The Cadence Virtuoso Tool facilitated the design of the suggested 7T SRAM cells using FinFET technology. The suggested SRAM cell demonstrates a decrease in leakage power and current. However, due to the limitations of FinFET's ability to achieve adequate leakage power and current reduction, the SVL approach is necessary to further minimise these parameters in the 7T SRAM cell. This design uses only 24.29 nW of power and has a minimum leakage current of 9.46 nA. This is possible by using both LSVL and USVL methods together. This proposed SRAM cell design decreases the leakage power by up to 10% and 31% as compared to SRAM cells designed using the USVL and LVSL techniques, respectively. The proposed 7T SRAM cell utilising FinFET technology demonstrates superior performance in leakage power and current consumption compared to the other 7T SRAM configurations presented in Table IV, particularly in the context of the collective approach of LSVL and USVL. Figure 16 is a comparison chart that shows the leakage currents and powers that come with different SVL methods. A more advanced version of a portable IoT system with a longer battery life has a low-leakage power memory design based on FinFET technology that utilises an integrated circuit, resulting in superior performance. Table V & VI compares the proposed 7T SRAM cell with previously published research articles.

Table IV
Analysis of Leakage Current and Power for the suggested SRAM cell

S. No.	Proposed 7T SRAM	Leakage	
		Power	Current
1	With Mixing (LSVL + USVL) Technique	24.28 nW	9.45 nA
2	With LSVL Technique	35.48 nW	28.22 nA
3	With USVL Technique	26.98 nW	10.6 nA

Table V
Analysis comparing the 7-Transistor SRAM cell with findings from other published research articles

S. No.	SRAM Cell Configuration	Leakage Power (nW)
1	Proposed with LSVL Technique	35.48
2	Proposed with USVL Technique	26.98
3	Proposed with Mixing (LSVL + USVL) Technique	24.28
4	Santosh [45]	35.22
5	Kushwaha [46]	26.63
6	Ensan [31]	69.1

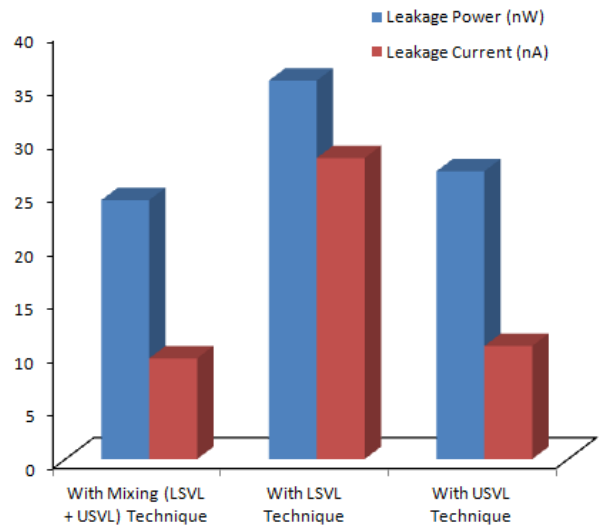

Fig 16: Comparison of Leakage Current and Power in the Suggested 7-Transistor SRAM Cell utilizing FinFET Technology.

Table VI
Analysis of Leakage Current for Suggested SRAM cell with other published research articles

S. No.	SRAM Cell Configuration	Leakage Current (nA)
1	Proposed with LSVL Technique	28.22
2	Proposed with USVL Technique	10.6
3	Proposed with Mixing (LSVL + USVL) Technique	9.45
4	Kariyappa [47]	64.25
5	Santosh [48]	50.26

Applications of suggested SRAM design for In-Memory Computing Applications

FinFET-based SRAM cells, with their superior electrostatic control, reduced leakage current and enhanced performance at nano-scale dimensions, offer significant advantages for in-memory computing applications. Such potential applications are:

i. FinFET SRAM can be used to build Compute-in-Memory (CIM) architectures where the weights of a neural network are stored in the SRAM cells, and matrix-vector multiplications, which are fundamental to neural network inference, are performed directly within the memory array.
ii. FinFET SRAM's stability and high speed make it suitable for implementing high-performance Content-Addressable Memories (CAMs). In-memory computing principles can be applied to perform the comparison operations directly within the memory cells, enhancing the search speed and energy efficiency compared to traditional CAM designs.
iii. Beyond arithmetic operations, FinFET SRAM can be designed to perform Boolean logic operations directly within the memory array. This capability can be leveraged in applications requiring fast logic processing on large datasets stored in memory. For instance, operations like AND, OR, NAND, NOR, and XOR can be implemented using modified SRAM cell structures and control schemes.
iv. Operations like filtering, convolution, and correlation, which are heavily used in image and video processing, can be accelerated using FinFET SRAM-based CIM. The parallel processing capabilities of in-memory computing can significantly speed up these tasks.
v. In-memory computing using FinFET SRAM can potentially improve the performance and energy efficiency of these algorithms by performing computations closer to the data.

VIII. Conclusion and Future Work

Enhanced driving capability enables faster operations to function at reduced voltage levels, resulting in lower energy consumption. This article presents various circuits proposed to reduce the leakage parameter in FinFET devices, complementing existing solutions. The study of leakage currents in 7T SRAM cells using FinFET technology while they are in standby mode shows that these currents make a big difference in the total amount of power that is lost through leakage. The study is mostly about how SVL circuits can be used to lower the supply voltage and raise the ground voltage so that 7T SRAM cells using FinFET technology have less leakage power and current. The application of the SVL technique demonstrated a reduction in leakage power and current, contributing to the minimisation of LSVL and USVL. Additionally, combined strategies were introduced that effectively decreased leakage in FinFET-based SRAM cells. This method is superior to either the USVL or LSVL method used alone because it cuts down on leakage power and current by a lot compared to the USVL and LSVL methods alone. This design uses only 24.29 nW of power and has a minimum leakage current of 9.46 nA. This is possible by using both LSVL and USVL techniques together. This proposed SRAM cell design reduces leakage power by up to 10% and 31% relative to SRAM cells designed using the USVL and LVSL techniques, respectively.

Future research may be explored as:

i. Integrating FinFET SRAM with non-volatile memory technologies (e.g., MRAM, STT-MRAM, ReRAM) on the same chip could create hybrid memory systems with the speed of SRAM and the non-volatility of other memories, opening up new possibilities for power-efficient and persistent memory solutions.
ii. Research into advanced FinFET designs, like gate-all-around (GAA) nano-wire/nano-sheet FETs, could result in better control of electrical signals, reduced energy loss, and enhanced performance for in-memory computing uses. These advancements could enable more energy-efficient and faster CIM designs based on SRAM.
iii. FinFET-based SRAM for in-memory computing has a promising future, with significant potential to revolutionize energy-efficient and high-performance computing. Continued research and innovation in cell design, hybrid memory systems, reliability enhancements, software co-design, and application-specific optimization will pave the way for the widespread adoption of this promising technology.

References

[1] Bowman, K. A., Duvall, S. G., & Meindl, J. D. (2002). Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for giga-scale integration. *IEEE Journal of Solid-State Circuits*, *37*(2), 183.
[2] Calhoun, B. H., & Chandrakasan, A. P. (2007). A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation. IEEE journal of solid-state circuits, 42(3), 680-688.

[3] Kim, T. H., Liu, J., Keane, J., & Kim, C. H. (2008). A 0.2 V, 480 kb subthreshold SRAM with 1 k cells per bitline for ultra-low-voltage computing. IEEE Journal of Solid-State Circuits, 43(2), 518-529.

[4] Ebrahimi, B., Afzali-Kusha, H., & Afzali-Kusha, A. (2012). Low power and robust 8T/10T subthreshold SRAM cells. In 2012 International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) (pp. 141-144). IEEE.

[5] Kiran, P. V., & Saxena, N. (2015). Design and analysis of different types SRAM cell topologies. In 2015 2nd International Conference on Electronics and Communication Systems (ICECS) (pp. 167-173). IEEE.

[6] Gupta S, Gupta K, Pandey N (2018). Pentavariate Vmin analysis of a subthreshold 10T SRAM bit cell with variation tolerant write and divided bit-line read. IEEE Trans Circuits Syst I Regul Pap 65(10):3326–3337

[7] Kumar, T. S., & Tripathi, S. L. (2019). Implementation of CMOS SRAM Cells in 7, 8, 10 and 12-transistor topologies and their performance comparison. International Journal of Engineering and Advanced Technology, 8(2S2), 227–229.

[8] Rathod, S. S., Saxena, A. K., & Dasgupta, S. (2010). A proposed DG-FinFET based SRAM cell design with RadHard capabilities. Microelectronics Reliability, 50(8), 1039–1190.

[9] Kushwaha, C. B., Vishvakarma, S. K., & Dwivedi, D. (2016). A 20nm robust single-ended boostless 7T FinFET sub-threshold SRAM cell under process–voltage–temperature variation. Microelectronics Journal, 51, 75–88.

[10] Sil, A., Bakkamanthala, S., karlapudi, S., & Bayoumi, M. (2012). Highly Stable, Dual-port, Sub- threshold 7T SRAM Cell for Ultra-low Power Application. In IEEE International NEWCAS Confer- ence (pp. 493–496).

[11] Ansari, M., Afzali-Kusha, H., Ebrahimi, B., Navabi, Z., Afzali-Kusha, A., & Pedram, M. (2015). A near-threshold 7T SRAM cell with high write and read margins and low write time for sub-20 nm FinFET technologies. Integration, 50, 91-106.

[12] Gavaskar, K., & Ragupathy, U. S. (2019). Low power self-controllable voltage level and low swing logic based 11T SRAM cell for high speed CMOS circuits. Analog Integrated Circuits and Signal Processing, 100(1), 61–77.

[13] Satish, M. N., Vasundara Patel K. S. (2019). Power Reduction in FinFET Half Adder using SVL Tech- nique in 32 nm Technology. In IEEE MEC International Conference on Big Data and Smart City (ICBDSC)

[14] Birla, S., Shukla, N. K., Pattanaik, M., & Singh, R. K. (2010). Device-and-circuit-design-challenges-for- low-leakage-SRAM for ultra-low power applications. Canadian Journal on Electrical & Electronics Engineering, 1(7), 156–167.

[15] Gupta, D. C., & Raman, A. (2012). Analysis of leakage current reduction techniques in SRAM cell in 90 nm CMOS technology. IJCA, 50(19), 18–22.

[16] Lavanya, S., & Lisbin, J. (2012). Self controllable voltage level (SVL) for low power consumption. In 2012 IEEE International Conference on Computational Intelligence and Computing Research (pp. 1-5). IEEE.

[17] Asli, R.N. and Taghipour, S., 2020. Reliable and high performance asymmetric FinFET SRAM cell using back-gate control. *Microelectronics Reliability*, *104*, p.113545.

[18] Sneha, G., Krishna, B. H., & Kumar, C. A. (2017). Design of 7T FinFET based SRAM cell design for nanometer regime. In 2017 International Conference on Inventive Systems and Control (ICISC), IEEE, 1–4.

[19] Yang, Y., Jeong, H., Song, S. C., Wang, J., Yeap, G., & Jung, S. O. (2016). Single bit-line 7T SRAM cell for near threshold voltage operation with enhanced performance and energy in 14 nm FinFET technology. IEEE Transactions on Circuits and Systems I: Regular Papers, 63(7), 1023–1032.

[20] Monica, M., &Chandra Mohan, P. (2017). A Novel 8T SRAM Cell using 16 nm FinFET Technology. SASTech-Technical Journal of RUAS, 16(1), 5–8.

[21] Farkhani, H., Peiravi, A., Kargaard, J. M., & Moradi, F. (2014). Comparative study of FinFETs versus 22nm bulk CMOS technologies: SRAM design perspective. In 2014 27th IEEE International System-on-Chip Conference (SOCC), IEEE, 449–454.

[22] Kim, Y. B., Kim, Y. B., & Lombardi, F. (2008). New SRAM cell design for low power and high reliability using 32nm independent gate FinFET technology. In 2008 IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems, IEEE, 25–28.

[23] Yang, Y., Park, J., Song, S. C., Wang, J., Yeap, G., & Jung, S. O. (2014). Single-ended 9T SRAM cell for near-threshold voltage operation with enhanced read performance in 22-nm FinFET technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 23(11), 2748–2752.

[24] Moradi, F., & Tohidi, M. (2015). Low-voltage 9T FinFET SRAM cell for low-power applications. In 2015 28th IEEE International System-on-Chip Conference (SOCC), IEEE, 149–153.

[25] Oh, T. W., Jeong, H., Kang, K., Park, J., Yank, Y., & Jung, S. O. (2016). Power-gated 9T SRAM cell for low-energy operation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 25(3), 1183–1187.

[26] Yadav, N., Dutt, S., Pattnaik, M., & Sharma, G. K. (2013). Double-gate FinFET process variation aware 10T SRAM cell topology design and analysis. In 2013 European Conference on Circuit Theory and Design (ECCTD), IEEE, 1–4.

[27] Sharma, M., Gill, S. S., Sharma, K., & Krishna, B. (2025). Design of High-Speed Low-power SRAM Cell using FinFET in the Stack Method for Medical Applications. *WSEAS Transactions on Biology and Biomedicine*, *22*, 26-36.

[28] Birla, S., Shukla, N. K., Singh, N., & Raja, R. K., 2020. Performance Analysis of 8T FinFET SRAM Bit-Cell for Low-power Applications. In 2020 5th International Conference on Computing, Communication and Security (ICCCS) (pp. 1-4). IEEE.

[29] Kaushal, S., & Rana, A. K. (2022). Negative capacitance junction-less FinFET for low power applications: an innovative approach. Silicon, 14(12), 6719-6728.

[30] Subannan Palanisamy, K., & Ramachandran, R. (2020). FinFET-based power-efficient, low leakage, and area-efficient DWT lifting architecture using power gating and reversible logic. International Journal of Circuit Theory and Applications, 48(8), 1304-1318.

[31] Sayyah Ensan, S., Moaiyeri, M. H., Ebrahimi, B., Hessabi, S., & Afzali-Kusha, A. (2019). A low-leakage and high-writable SRAM cell with back-gate biasing in FinFET technology. Journal of Computational Electronics, 18, 519-526.

[32] Maroof N, Kong B (2017) 10T SRAM using half-precharge and row-wise dynamically powered read port for low switching power and ultralow RBL leakage. IEEE Trans Very Large Scale Integr. VLSI Syst 25(4):1193–1203.

[33] Mushtaq U, Sharma VK (2020) Design and analysis of INDEP FinFET SRAM cell at 7-nm technology. Int J Numer Model El :1–14..

[34] Calhoun BH, Ryan JF, Khanna S, Putic M, Lach J (2010) Flexible circuits and architectures for ultralow power. Proc. IEEE, 98(2): 267–282.

[35] Chung Y, Kim H (2017) A differential subthreshold SRAMcell for ultra-low voltage embedded computing applications. Int J Appl Eng Res 12:7998–8003.

[36] Sinangil ME, Lin YT, Liao HJ, Chang J (2019) A 290-mV, 7-nm ultra-Low-voltage one-port SRAM compiler design using a 12T write contention and read upset free bit-cell. IEEE J Solid State Circuits 54(4):1152–1160.

[37] Prasad G, Kumari N, Mandi BP, Ali M (2020) Design and statistical analysis of low power and high speed 10T static random access memory cell. Int J Circ Theor Appl :1–10.

[38] Garg, D., Singh R., Sharma D. K., (2024), Analysis of FinFET based SRAM cells with improved performance parameters, IJEECS, 37(3), pp. 1464-1475.

[39] Kumar, V. and Tomar, V.K., (2020), February. A comparative performance analysis of 6T, 7T and 8T SRAM cells in 18nm FinFET technology. In 2020 International Conference on Power Electronics & IoT Applications in Renewable Energy and its Control (PARC) (pp. 329-333). IEEE.

[40] Amelifard, B., Fallah, F., & Pedram, M. (2006). Reducing the sub-threshold and gate-tunneling leakage of SRAM cells using dual-Vt and dual-Tox assignment. In Proceedings of the Design Automation & Test in Europe Conference (Vol. 1, pp. 1-6). IEEE.

[41] Kushwah, R. S., & Sikarwar, V. (2015). Analysis of leakage current and power reduction techniques in FinFET based SRAM cell. Radio electronics and Communications Systems, 58(7), 312-321.

[42] Akashe, S., & Sharma, S. (2013). Leakage current reduction techniques for 7T SRAM cell in 45 nm technology. Wireless personal communications, 71, 123-136.

[43] Birla, S. (2019). Ultra-low Power FinFET SRAM Cell with improved stability suitable for low power applications. International Journal of Electronics and Telecommunications, 65(4).

[44] Endo, K., Shin-Ichioinchi, Ishikawa, Y., Liu, Y., Matsukawa, T., Sakamoto, K., Masahara, M., Tsukada, J., Ishii, K., Yamauchi, H., & Suzuki, E., (2009) Independent-Double-Gate FinFET SRAM for leakage current reduction. IEEE Electron Device letters, 30(7), 757–759.

[45] Kumar, T. S., & Tripathi, S. L. (2021). Leakage reduction in 18 nm FinFET based 7T SRAM cell using self-controllable voltage level technique. Wireless Personal Communications, 116(3), 1837-1847.
[46] Kushwaha RS, Akashe S (2014) Analysis of leakage reduction technique on FinFET based 7T and 8T SRAM cells. Radio electron Commun Syst 57:383–393.
[47] Kumar, C.S.H. and Kariyappa, B.S.,(2022). Analysis of 7T SRAM Cell Based on MTCMOS, SVL and I-SVL Technique. *Indian Journal of Science and Technology*, *15*(23), pp.1143-1150.
[48] Kumar, T.S., Tripathi, S.L. and Sinha, S.K.,(2020),June. Comparative analysis of leakage power in 18nm 7T and 8T SRAM cell Implemented with SVL Technique. In *2020 International Conference on Intelligent Engineering and Management (ICIEM)* (pp. 121-124). IEEE.

Deepak Garg (M'12) was born in Meerut, India, received the B. Tech degree in Electronics and Communication Engineering from Uttar Pradesh Technical University, Lucknow, received the M. Tech degree in VLSI from Shobhit University, Meerut, India in 2007 and 2010.
He is currently pursuing Ph.D. degree from SRM Institute of Science and Technology, Delhi-NCR Campus, Ghaziabad, India. His research interests include Digital circuit design, VLSI.

Rupali Singh was born in Maharashtra, INDIA, received the B. Tech degree in Electronics and Communication Engineering from Nagpur University, received M.Tech. degree from Shobhit University, Meerut, and received PhD degree from SRMIST, Ghaziabad, India in 2001, 2009 and 2021.
She is currently working at the Department of Electronics and Communication Engineering, at SRM Institute of Science and Technology, Delhi-NCR Campus, Ghaziabad, India as an Associate Professor and Head. She published more than 25 academic papers. Her research area includes Low Power Circuits, Reversible Logic and QCA.

Pankaj Singh was born in Mathura, INDIA, received the B. Tech degree in Electronics and Communication Engineering from Nagpur University, received M.Tech. degree from Dr. B R Ambedkar University, Agra, and received PhD degree from NIMS University, Rajasthan, India in 1998, 2005 and 2016.
He is currently working at the Department of Electrical and Electronics Engineering, at IIMT University, Meerut, India as an Associate Professor. He published more than 30 academic papers. His research area includes Microwave, Low Power Circuits and Reversible Logic.