Research on the Control Mechanism of DC Capacitor Voltage of SSSC Based on Multi-pulse VSC

Guanjun Ding, Guangfu Tang, and Ming Ding

***Abstract*—The characteristics of Static Synchronous Series Compensator (SSSC) based on six-pulse Voltage Source Converter (VSC), which is inserted in series into a three phase inductive system, are analyzed and calculated in detail in its inductive and capacitive operation modes, including the AC, DC current and DC capacitor voltage in one period. And the expressions for them are derived in order to assess the compensator performance. The SSSC based on six-pulse VSC is specially studied because it gives an insight into the study of the more complex configurations. On the basis of calculations and simulations in PSCAD/EMTDC, the impact of current on DC capacitor charge and discharge is analyzed thoroughly. A methodology for the capacitor voltage control of SSSC is obtained. Meanwhile, a basis for choosing semiconductor devices of SSSC is presented in the paper.**

***Index Terms*—control mechanism, impact of current on the capacitor, multi-pulse VSC, Static Synchronous Series Compensator (SSSC), Voltage Source Converter (VSC).**

I. Introduction

Static Synchronous Series Compensator (SSSC) is a series type of Flexible AC Transmission System (FACTS) devices, which is based on self commutated converters formed by semiconductor switches with self turn-off capability. The main objective of the SSSC is the compensation of transmission lines. This device is inserted in series with the line to inject a voltage in quadrature with the line current in order to emulate a reactance. So it has a direct effect over the line current [1-2].

Voltage Source Converter (VSC) is the most crucial part of SSSC [3]. VSC has many types of topology configuration. The multi-pulse configuration is chosen in this paper due to its characteristics and applicability. Most of the existing VSC based FACTS devices rated above 80 MVAR use either 24 or 48-pulse converters [4], because they exhibit several advantages over other VSC configurations, e.g., better harmonic property, lower switching frequency, lower rated voltage level of DC capacitor, etc [5].

SSSC based on multi-pulse VSC has been researched in the past few years by some well-known scholars. For instance, Kalyan K. Sen researched on the SSSC based on 24-pulse VSC [6], and L. Sunil Kumar, Arindam Ghosh studied on the SSSC based on 48-pulse VSC [7]. But they didn't analyze the AC and DC current of VSC and the impact of current on DC capacitor charge and discharge. These aspects are important because such analyses lead to full understanding of the converter and its mechanism for controlling and implementing it. And this is exactly the aim of the paper.

II. Characteristics Of Sssc Based On Six-Pulse Vsc, Only Reactive Power Exchange

The basic topology of VSC is six-pulse configuration, when the gate pulse pattern of its devices is fundamental switching mode, the output load side voltage of phase A is shown as Fig. 1.

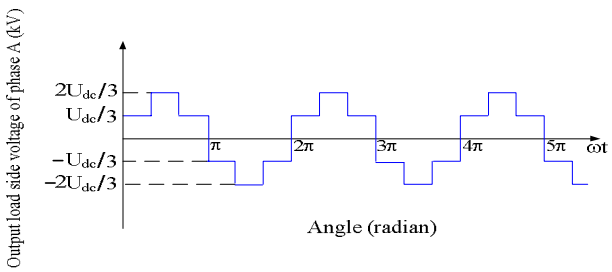

Fig. 1. Output load side voltage of phase A of six-pulse VSC.

The transmission line impedance has resistive and inductive components, is mostly inductive. And it is such inductive component that the SSSC attempts to modify by injecting a voltage with controllable magnitude. So in the following, a three phase inductive system with pure inductive line is used to perform the analyses, in which SSSC based on six-pulse VSC is inserted in series representing a sinusoidal voltage source, shown as Fig. 2. The analyses include the AC, DC current and DC capacitor voltage of the VSC, and the impact of current on DC capacitor charge and discharge. The SSSC based on six-pulse VSC is specially studied because it gives an insight into the study of the more complex configurations.

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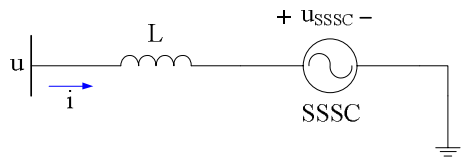

Fig. 2. SSSC embedded in an inductive circuit.

In Fig. 2, the AC system voltage is "$u = U_m \cdot sin(\omega t)$", the current i lags the voltage u by 90° due to the pure inductive line. "u_{SSSC}" denotes the injected voltage with controllable magnitude of SSSC. In real circuits it is a common practice to connect a star-star transformer with a turn ratio of 1:1 to the VSC in order to couple the VSC with an external circuit. The AC voltages are taken from the secondary side of the coupling transformer. Neglecting losses the current flowing in the secondary side equals the current in the primary side of each single phase transformer. Therefore the SSSC currents are the line currents. The vector diagram of voltages and current in inductive and capacitive operation modes of SSSC is shown in Fig. 3.

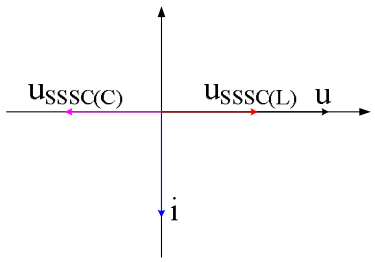

Fig. 3. Vector diagram of voltages and current.

In Fig. 3, $u_{SSSC(L)}$ denotes the injected voltage in inductive operation mode of SSSC; $u_{SSSC(C)}$ denotes the injected voltage in capacitor operation mode of SSSC.

Fig. 4 depicts the AC system voltage u and the injected voltage u_{SSSC} of phase A in one period.

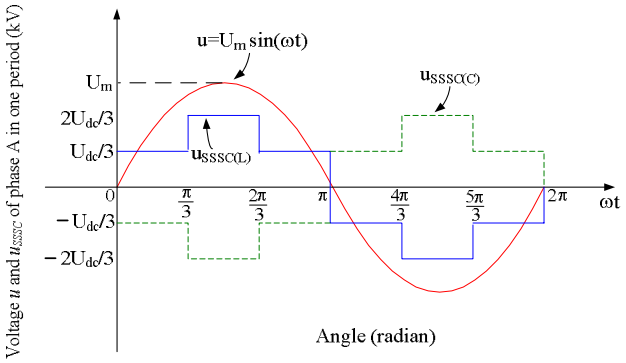

Fig. 4. AC system voltage u and injected voltage u_{SSSC} of phase A in one period.

A. Analysis of AC side Current

The expression that describes the circuit shown in Fig. 2 is as (1), i.e., the current flowing between SSSC and the AC system is determined by the voltage across the inductor L.

$$u_L(t) = L\frac{di}{dt} = u - u_{SSSC} \tag{1}$$

Taking into account the injected voltage u_{SSSC} over each 60° conduction interval (see Fig. 4), the equation that describes the AC side current $i_a(t)$ is derived. The specific analysis is as follows:

1) Interval: $0 \leqslant \omega t \leqslant \pi/3$

$$L\frac{di_a(t)}{dt} = U_m \cdot sin(\omega t) - (-1)^S \frac{U_{dc}}{3} \Rightarrow$$

$$i_a(t) = \int_0^t \frac{U_m}{L} sin(\omega t)dt - \int_0^t (-1)^S \frac{U_{dc}}{3L} dt + I_0 \Rightarrow$$

$$i_a(t) = \frac{U_m}{\omega L}[1 - cos(\omega t)] - (-1)^S \frac{U_{dc}}{3L} \cdot t + I_0 \tag{2}$$

where I_0 is the initial condition at t=0, i.e., $I_0 = i_a(0)$. S is a marked sign, if SSSC is in its inductive operation mode, the value of S is zero, i.e., S=0; if SSSC is in its capacitive operation mode, the value of S is one, i.e., S=1. In the following expressions, S has the same meaning as abovementioned.

2) Interval: $\pi/3 \leqslant \omega t \leqslant 2\pi/3$

$$L\frac{di_a(t)}{dt} = U_m \cdot sin(\omega t) - (-1)^S \frac{2U_{dc}}{3} \Rightarrow$$

$$i_a(t) = \int_{\frac{\pi}{3\omega}}^t \frac{U_m}{L} sin(\omega t)dt - \int_{\frac{\pi}{3\omega}}^t (-1)^S \frac{2U_{dc}}{3L} dt + I_1 \Rightarrow$$

$$i_a(t) = \frac{U_m}{\omega L}\left[\frac{1}{2} - cos(\omega t)\right] - (-1)^S \frac{2U_{dc}}{3L}\left(t - \frac{\pi}{3\omega}\right) + I_1 \tag{3}$$

where $I_1 = i_a\left(\frac{\pi}{3\omega}\right)$.

3) Interval: $2\pi/3 \leqslant \omega t \leqslant \pi$

$$L\frac{di_a(t)}{dt} = U_m\, sin(\omega t) - (-1)^S \frac{1}{3}U_{dc} \Rightarrow$$

$$i_a(t) = \int_{\frac{2\pi}{3\omega}}^t \frac{U_m}{L} sin(\omega t)dt - \int_{\frac{2\pi}{3\omega}}^t (-1)^S \frac{1}{3L}U_{dc}dt + I_2 \Rightarrow$$

$$i_a(t) = \frac{U_m}{\omega L}\left[-\frac{1}{2} - cos(\omega t)\right] - (-1)^S \frac{1}{3L}U_{dc} \cdot \left(t - \frac{2\pi}{3\omega}\right) + I_2 \tag{4}$$

where $I_2 = i_a\left(\frac{2\pi}{3\omega}\right)$.

It is known that in steady state the AC current waveform is symmetric, therefore,

$$i_a\left(\frac{\pi}{2\omega}\right) = 0 \tag{5}$$

taking into account the above property, I_0, I_1 and I_2 can be calculated as (6).

$$\begin{cases} I_1 = (-1)^S \dfrac{\pi}{9\omega L}U_{dc} - \dfrac{U_m}{2\omega L} \\ I_2 = (-1)^{S+1} \dfrac{\pi}{9\omega L}U_{dc} + \dfrac{U_m}{2\omega L} \\ I_0 = (-1)^S \dfrac{2\pi}{9\omega L}U_{dc} - \dfrac{U_m}{\omega L} \end{cases} \tag{6}$$

So $i_a(t)$ can be obtained shown as (7).

$$i_a(t)=\begin{cases}-\frac{U_m}{\omega L}cos(\omega t)-(-1)^S\cdot\left(\frac{t}{3L}-\frac{2\pi}{9\omega L}\right)\cdot U_{dc} & \left(0\le\omega t\le\frac{\pi}{3}\right)\\ -\frac{U_m}{\omega L}cos(\omega t)-(-1)^S\cdot\left(\frac{2t}{3L}-\frac{\pi}{3\omega L}\right)\cdot U_{dc} & \left(\frac{\pi}{3}\le\omega t\le\frac{2\pi}{3}\right)\\ -\frac{U_m}{\omega L}cos(\omega t)-(-1)^S\cdot\left(\frac{t}{3L}-\frac{\pi}{9\omega L}\right)\cdot U_{dc} & \left(\frac{2\pi}{3}\le\omega t\le\pi\right)\end{cases} \quad (7)$$

Over the interval $\pi \leqslant \omega t \leqslant 2\pi$, the waveform of AC side phase current $i_a(t)$ is the negative respect to that described in (7). The other two phase currents, $i_b(t)$ and $i_c(t)$ are identical except phase shifted by 120° and 240° from $i_a(t)$, respectively.

B. Analysis of DC Capacitor Current

Once the SSSC currents are known it is possible to derive the DC capacitor current i_{dc}. The DC capacitor current is constructed by adding segments of AC phase currents. The segments depend on which transistor-diode (*G–D*) pair is conducting. Analyzing the upper *G–D* pairs of the six-pulse VSC, it is observed that the pairs G_1-D_1, G_3-D_3 and G_5-D_5 participate in the DC capacitor current, thus,

$$i_{dc}=gs_1\cdot i_a+gs_3\cdot i_b+gs_5\cdot i_c \quad (8)$$

where gs_1, gs_3 and gs_5 are the gate signals of G_1, G_3 and G_5 respectively, and take values of 0 and 1 when they are *off* and *on* respectively.

When the gate signal is present in the transistor of a upper *G–D* pair, the transistor conducts if the current is negative and the diode conducts if the current is positive. Analyzing the gate pulse patterns of gs_1, gs_3 and gs_5, the following behavior of i_{dc} can be deducted for a cycle in the inductive mode of operation. For the capacitive operating mode, the intervals are the same except that are phase shifted by 180°.

1) Interval: $0\leqslant\omega t<\pi/3$

Signals gs_1 and gs_5 are activated, therefore i_{dc} is formed of i_a and i_c, i.e.,

$$i_{dc}(t)=i_a(t)+i_c(t) \quad (9)$$

where $i_c(t)=-\frac{U_m}{\omega L}cos\left(\omega t+\frac{2\pi}{3}\right)-\left(\frac{1}{3L}\cdot t+\frac{\pi}{9\omega L}\right)\cdot U_{dc}$.

2) Interval: $\pi/3\leqslant\omega t<2\pi/3$

Only gs_1 is present, consequently i_{dc} equals i_a, i.e.,

$$i_{dc}(t)=i_a(t) \quad (10)$$

3) Interval: $2\pi/3\leqslant\omega t\leqslant\pi$

Signals gs_1 and gs_3 are activated, thus i_{dc} is constructed of i_a and i_b, i.e.,

$$i_{dc}(t)=i_a(t)+i_b(t) \quad (11)$$

where $i_b(t)=-\frac{U_m}{\omega L}cos\left(\omega t-\frac{2\pi}{3}\right)-\left(\frac{1}{3L}\cdot t-\frac{4\pi}{9\omega L}\right)\cdot U_{dc}$.

Taken together abovementioned and in combination with (7), the expression for DC capacitor current $i_{dc}(t)$ is as follows.

$$i_{dc}(t)=\begin{cases}(-1)^S\frac{U_m}{\omega L}sin\left(\omega t-\frac{\pi}{6}\right)-\left(\frac{2t}{3L}-\frac{\pi}{9\omega L}\right)\cdot U_{dc} & \left(0\le\omega t<\frac{\pi}{3}\right)\\ (-1)^S\frac{U_m}{\omega L}sin\left(\omega t-\frac{\pi}{2}\right)-\left(\frac{2t}{3L}-\frac{\pi}{3\omega L}\right)\cdot U_{dc} & \left(\frac{\pi}{3}\le\omega t<\frac{2\pi}{3}\right)\\ (-1)^{S+1}\frac{U_m}{\omega L}sin\left(\omega t+\frac{\pi}{6}\right)-\left(\frac{2t}{3L}-\frac{5\pi}{9\omega L}\right)\cdot U_{dc} & \left(\frac{2\pi}{3}\le\omega t\le\pi\right)\end{cases} \quad (12)$$

These expressions are equivalent except phase shifted by 60° among them; therefore the capacitor current waveform over each of the remaining three conduction periods is identical to that described by (12), and yields, in a repetitive waveform, six times the corresponding AC system frequency. When the parameters used are $U_m=220\sqrt{2}$ V, L=6mH, f=50Hz and $U_{dc}=50$ V, the waveforms of $i_{dc}(t)$ in the inductive operation mode and capacitive operation mode of SSSC are shown as Fig. 5 and 6, respectively.

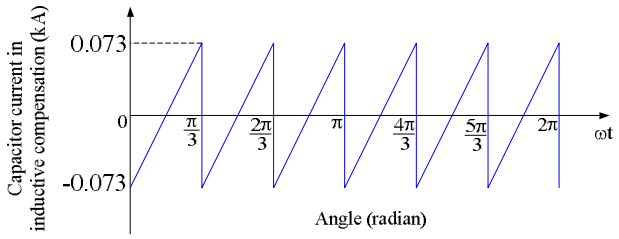

Fig. 5. DC capacitor current $i_{dc}(t)$ in inductive operation mode of SSSC.

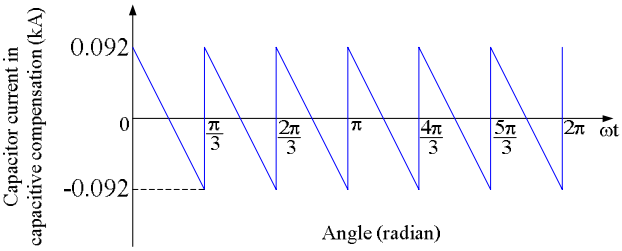

Fig. 6. DC capacitor current $i_{dc}(t)$ in capacitive operation mode of SSSC.

As seen in Fig. 5 and 6, the capacitor current results in a periodic waveform with a period of 60°.

C. Analysis of DC Capacitor Voltage

Assuming a lossless SSSC, the DC capacitor is initially charged and preserves its charge during the operation. The DC capacitor voltage is given by the following expression.

$$u_{dc}(t)=\frac{1}{C}\int i_{dc}(t)dt+U_0 \quad (13)$$

where U_0 is the initial capacitor voltage, i.e., $U_0=u_{dc}(0)$.

Assuming that the capacitor current remains significantly unchanged from that given by (12), the DC capacitor voltage can be estimated; under this condition a minimum DC ripple voltage is obtained [8]. The capacitor voltage over the first 60° period is given by:

$$u_{dc}(t)=\frac{1}{C}\int_0^t i_{dc}(t)dt+U_0 \quad (14)$$

where $t\in[0, T]$, and $T=\frac{\pi}{3\omega}$.

Substituting the corresponding equation in (12) into (14),

$u_{dc}(t)$ can be obtained and shown as (15).

$$u_{dc}(t)=(-1)^S\cdot\frac{U_m}{\omega^2 LC}\left[\frac{\sqrt{3}}{2}-\cos\left(\omega t-\frac{\pi}{6}\right)\right]-\frac{U_{dc}}{3LC}t^2+\frac{\pi}{9\omega LC}U_{dc}\cdot t+U_0 \quad (15)$$

At the same time the DC voltage level $U_{dc}=\frac{1}{T}\int_0^T u_{dc}(t)dt$, so the value of U_0 can be calculated and shown as (16).

$$U_0=(-1)^S\cdot 0.089\cdot\frac{U_m}{\omega^2 LC}-0.06097\frac{U_{dc}}{\omega^2 LC}+U_{dc} \quad (16)$$

So (15) can be transformed into (17), it's the expression for $u_{dc}(t)$.

$$u_{dc}(t)=(-1)^S\cdot\frac{U_m}{\omega^2 LC}\left[0.955-\cos\left(\omega t-\frac{\pi}{6}\right)\right]-\frac{U_{dc}}{3LC}t^2+\frac{\pi}{9\omega LC}U_{dc}\cdot t-0.06097\frac{U_{dc}}{\omega^2 LC}+U_{dc} \quad (17)$$

From the relationship between $u_{dc}(t)$ and $i_{dc}(t)$, i.e., (13) or (14), it is known that when $i_{dc}(t)$ has the value of zero, $u_{dc}(t)$ has extremum value U_{pk} of capacitor voltage shown as follows.

$$U_{pk}=u_{dc}\left(\frac{\pi}{6\omega}\right)=(-1)^{S+1}\cdot 0.045\frac{U_m}{\omega^2 LC}+0.0304\frac{U_{dc}}{\omega^2 LC}+U_{dc} \quad (18)$$

If SSSC is in its inductive operation mode, U_{pk} is the minimum value; if SSSC is in its capacitive operation mode, U_{pk} is the maximum value. So there are two quantities are worth attention, i.e., the initial capacitor voltage in inductive operation mode (denoted as U_{0L}) and U_{pk} in capacitive operation mode (denoted as U_{pkC}). Taking higher value between U_{0L} and U_{pkC}, and this higher value is denoted as U_{max}, i.e., $U_{max}=max(U_{0L},U_{pkC})$. Comparing corresponding expressions of U_{0L} in (16) and U_{pkC} in (18), the following can be got that if $U_{dc}\leqslant 0.482U_m$, $U_{max}=U_{0L}$; if $U_{dc}\geqslant 0.482U_m$, $U_{max}=U_{pkC}$. U_{max} is very important to semiconductor devices because the capacitor voltage is applied directly to the semiconductor devices, therefore those semiconductor devices must be able to support that voltage. And it is a basis for choosing semiconductor devices of SSSC.

The abovementioned parameters are still used, and C=500 μ F, then the waveforms of $u_{dc}(t)$ in the inductive operation mode and capacitive operation mode of SSSC are shown as Fig. 7 and 8, respectively.

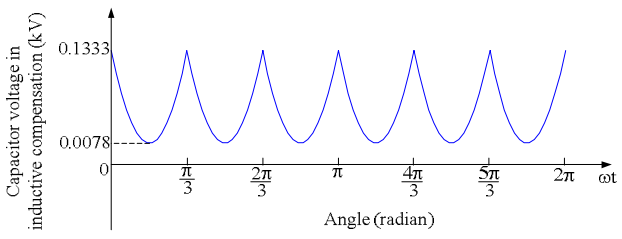

Fig. 7. DC capacitor voltage $u_{dc}(t)$ in inductive operation mode of SSSC.

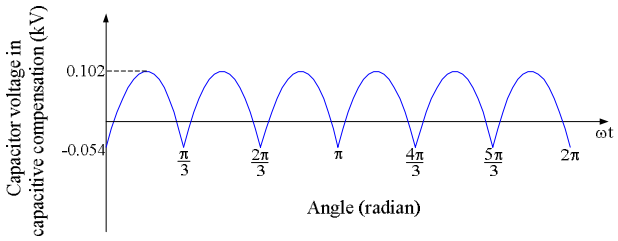

Fig. 8. DC capacitor voltage $u_{dc}(t)$ in capacitive operation mode of SSSC.

The DC capacitor current described as (12) and shown in Fig. 5 and 6 has an average value of zero. Thus, taking into account (13), the capacitor current does not have effect on the capacitor charge regardless the type of compensation the SSSC is providing. That is, when the compensator voltage is in quadrature with the line current only reactive power is exchanged between the compensator and the system. Otherwise, a different behavior is found. To show this, a phase shift in u is considered, i.e., $u=U_m\sin(\omega t-\theta)$. The specific analyses are as follows.

III. Characteristics Of Sssc Based On Six-Pulse Vsc, Both Real Power And Reactive Power Exchange

A phase shift θ is considered in u, i.e., $u=U_m\sin(\omega t-\theta)$. The vector diagram of voltages and current in inductive and capacitive operation modes of SSSC in this case is shown in Fig. 9. Fig. 10 depicts the AC system voltage u and the injected voltage u_{SSSC} of phase A in one period in this case.

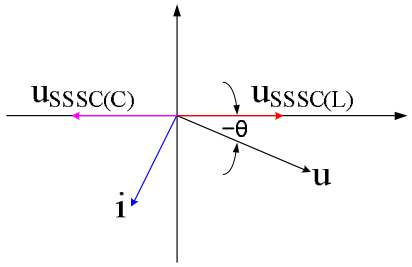

Fig. 9. Vector diagram of voltages and current with θ >0.

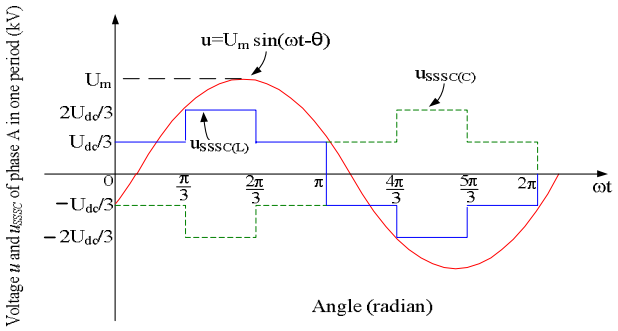

Fig. 10. AC system voltage u with phase shift θ >0 and injected voltage u_{SSSC} of phase A in one period.

A. Analysis of AC side Current

To obtain the AC side current equations, a similar procedure to that presented in section Ⅱ.A is carried out. But

in this case in steady state the AC current waveform has the following property.

$$i_a(0) = -i_a\left(\frac{\pi}{\omega}\right) \tag{19}$$

So I_0, I_1 and I_2 can be calculated in this case. By means of calculations, the expression for $i_a(t)$ is described as (20) in this case.

$$i_a(t) = \begin{cases} -\frac{U_m}{\omega L}\cos(\omega t-\theta)-(-1)^S\left(\frac{t}{3L}-\frac{2\pi}{9\omega L}\right)U_{dc} & \left(0 \le \omega t \le \frac{\pi}{3}\right) \\ -\frac{U_m}{\omega L}\cos(\omega t-\theta)-(-1)^S\left(\frac{2t}{3L}-\frac{\pi}{3\omega L}\right)U_{dc} & \left(\frac{\pi}{3} \le \omega t \le \frac{2\pi}{3}\right) \\ -\frac{U_m}{\omega L}\cos(\omega t-\theta)-(-1)^S\left(\frac{t}{3L}-\frac{\pi}{9\omega L}\right)U_{dc} & \left(\frac{2\pi}{3} \le \omega t \le \pi\right) \end{cases} \tag{20}$$

B. Analysis of DC Capacitor Current

A similar procedure to that presented in section Ⅱ.B is carried out. The expression for $i_{dc}(t)$ is described as (21).

$$i_{dc}(t) = \begin{cases} (-1)^S\frac{U_m}{\omega L}\sin\left(\omega t-\theta-\frac{\pi}{6}\right)-\left(\frac{2t}{3L}-\frac{\pi}{9\omega L}\right)U_{dc} & \left(0 \le \omega t < \frac{\pi}{3}\right) \\ (-1)^S\frac{U_m}{\omega L}\sin\left(\omega t-\theta-\frac{\pi}{2}\right)-\left(\frac{2t}{3L}-\frac{\pi}{3\omega L}\right)U_{dc} & \left(\frac{\pi}{3} \le \omega t < \frac{2\pi}{3}\right) \\ (-1)^{S+1}\frac{U_m}{\omega L}\sin\left(\omega t-\theta+\frac{\pi}{6}\right)-\left(\frac{2t}{3L}-\frac{5\pi}{9\omega L}\right)U_{dc} & \left(\frac{2\pi}{3} \le \omega t \le \pi\right) \end{cases} \tag{21}$$

The abovementioned parameters are still used, the waveforms of $i_{dc}(t)$ in the inductive and capacitive operation mode of SSSC with $\theta = 5°$, $\theta = -1°$ and $\theta = -5°$ are shown as Fig. 11-14, respectively.

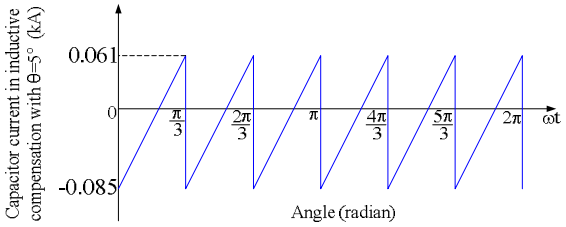

Fig. 11. DC capacitor current (inductive compensation with $\theta = 5°$).

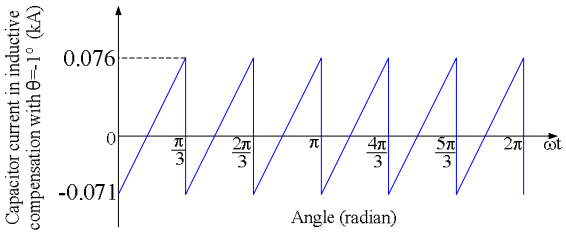

Fig. 12. DC capacitor current (inductive compensation with $\theta = -1°$).

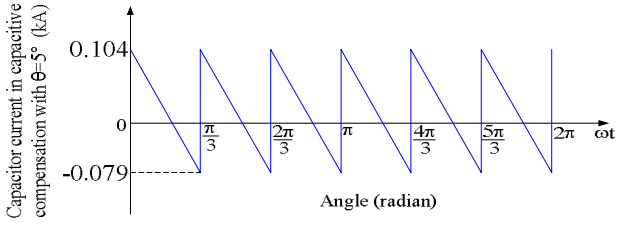

Fig. 13. DC capacitor current (capacitive compensation with $\theta = 5°$).

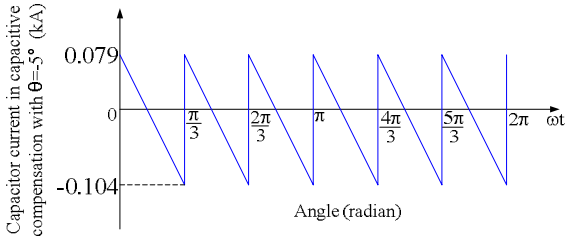

Fig. 14. DC capacitor current (capacitive compensation with $\theta = -5°$).

C. Analysis of DC Capacitor Voltage

The waveforms of $u_{dc}(t)$ in the inductive and capacitive operation mode of SSSC with $\theta = -1°$ and $\theta = 5°$ are shown as Fig. 15 and 16, respectively.

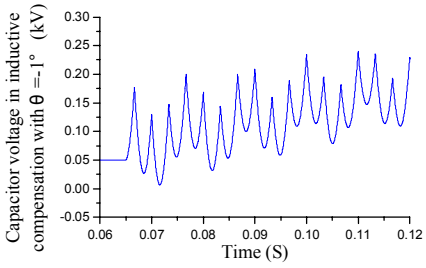

Fig. 15. DC capacitor voltage (inductive compensation with $\theta = -1°$).

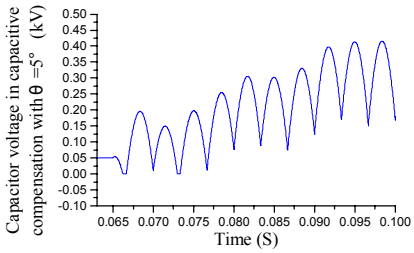

Fig. 16. DC capacitor voltage (capacitive compensation with $\theta = 5°$).

IV. Conclusion

The theoretical calculations and simulation results lead to the following three conclusions:

1) When the injected voltage of the SSSC is in quadrature with the line current, the capacitor current has an average value of zero. So the capacitor current doesn't have effect on the capacitor charge regardless the type of compensation the SSSC is providing. Only reactive power is exchanged between the SSSC and the system. If the injected voltage leads the line current by 90°, it acts as a reactor, and it only absorbs reactive power. If the injected voltage lags the line current by 90°, it acts as a capacitor. Thus, it only provides reactive power.
2) When the injected voltage is out of quadrature with the line current, if the voltage leads the current by an angle between 0° and 90°, the capacitor current has a positive average value, thus the capacitor will be charged. At this time, the SSSC acts as an inductive reactance absorbing reactive power and active power. If the voltage leads the current by an angle greater than 90°, the capacitor current has a negative average value that discharges the capacitor, so the SSSC

absorbs reactive power while provides active power.

3) When the injected voltage is out of quadrature with the line current, if the voltage lags the current by an angle between 0° and 90°, the capacitor current has a positive average value, thus the capacitor will be charged. At this time, the SSSC acts as a capacitor reactance providing reactive power while absorbing active power. If the voltage lags the current by an angle greater than 90°, the capacitor current has a negative average value that discharges the capacitor, so the SSSC not only provides reactive power, but provides active power.

The degree of compensation of SSSC is proportional to the magnitude of the injected voltage, and, withal, the injected voltage is proportional to the DC capacitor voltage. With the above conclusions, a procedure to charge or discharge the capacitor can be easily applied. Therefore, the degree of compensation can be adjusted by charging or discharging the capacitor to the desired level easily. In addition, in practical circuits, VSC configurations are not losses, so the SSSC angle has to be varied a few degrees to be out of quadrature with the line current, enabling the flow of positive average capacitor current to compensate for the losses maintaining the desired capacitor voltage level.

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