Research and Analysis on the Reconfigurable System

LIU Guangzhong, XU Xiao

***Abstract*——After the appearance of Field Programmable Gate Array (FPGA), several systems have been built using FPGAs，thus called Reconfigurable System. The essence of Reconfigurable System is dynamically changing the circuit at runtime with the reconfigurable characteristic of Programmable Logic Devices to give the system advantages of both hardware and software. The thesis here starting from the basic technology of the Reconfigurable System——FPGA , makes comparative analysis of the reconfigurable and traditional systems, and introduces the application of the Reconfigurable System in the life.**

***Key words*——FPGA, Parallel Computing, Reconfigurable System**

Ⅰ. INTRODUCTION

With the continuous progress of the micro-electronics and the computer technologies, the hardware system has been softwared, particularly after the emergence of the large-scale high performance programmable devices, represented by FPGA (Field Programmable Gate Array). In the current world, particularly in the western developed countries, many high performance systems adopt the FPGA reconfigurable technologies for the construction, which conduct partial or whole reconfiguration on the programmable chips and dynamically change the functions of the system. While under the prerequisite to increase small quantity of hardware resources, the advantages of both hardware and software are combined into one and present super high computing capacities. The reconfigurable system designed on the basis of this technology has broad prospect for application in spaceflight, military and civil areas.

This thesis explores the reconfigurable system based on the reconfiguration technologies on the analysis of the programmable logic device FPGA's framework, principle structure, and compares which with the traditional computer systems.

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Ⅱ. FPGA

A .Concept of FPG

FPGA is to directly convert the hardware description into hardware realization [1] .The FPGA is flexibly used and the same piece of FPGA could generate different circuit functions through different programmable data. Users could place the FPGA's programmable data into Flash chips and load to FPGA through electrifying for initiation; users could also work out the online program and realize the online system reconfiguration; this feature could construct a CPU customized by different computing tasks, which is the popular area for research nowadays.

B. Framework of FPGA

Structurally FPGA could be divided into three main parts: Logic Block, Routing Channel and I/O Pad. I/O Pad consists of the ring surrounding the outer layer of the device; each I/O Pad provides the respective input, output or the bi-directional universal I/O pin connected at the external part of the FPGA packaging. The inside ring of the I/O Pad is allotted with square array logic block whereas the connection between the logic blocks and between the logic block and the I/O Pad could all pass the

programmable internal channel. Please see Figure 1 for details.

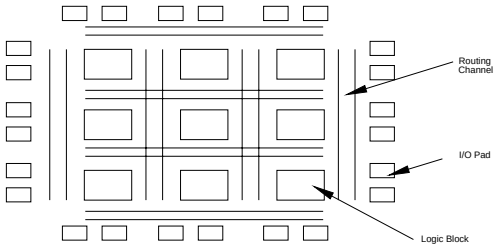

Figure 1 Typical FPGA framework

C. Advantages of FPGA

(1) Strong parallel capacity and quick computing speed. Though the computing speed of a single FPGA device is not very quick and the time frequency is lower than the CPU. Namely the time for a single FPGA to have an addition is about ten times that of the Pentium. However, this weakness could be compensated by the strong parallel capacity of FPGA.

(2) Low price and low power consumption. The computing capacity of the Virtex-4 chip of XILINX Company could reach 20- 120 GFLOPS, far beyond the 8 GFLOPS of Pentium 4 whereas the cost of each GFLOPS ranges only from 15 USD to 99 USD. From the power consumption, for each GFLOPS, the Virtex-4 only consumes 0.05--0.32 w whereas the Pentium consumes 16.5w and the earth simulator consumes 320 w.

D. Principle and structure of FPGA

(1) The principle and structure of Look-Up-Table

The Look-Up-Table is for short LUT and actually it's a RAM. Currently the FPGA mainly use the LUT with four routes of LUT, therefore, each LUT could be looked as a 16x1 RAM with 4 address lines. When the user describes a logic circuit with the principle scheme or HDL (Hardware Description Language), FPGA software will automatically compute all the possible results of the logic circuits and write the results into the RAM in advance. Therefore, every input of a signal for logic calculation equals to the input of an address to look up the table, find the corresponding content of the address and then output it.

(2) FPGA structure based on LUT

The internal structure of Xilinx Spartan-II (FPGA of the Spartan-II Serial introduced by Xilinx Company) and the Slices structure are shown in Figure 2 and Figure 3.

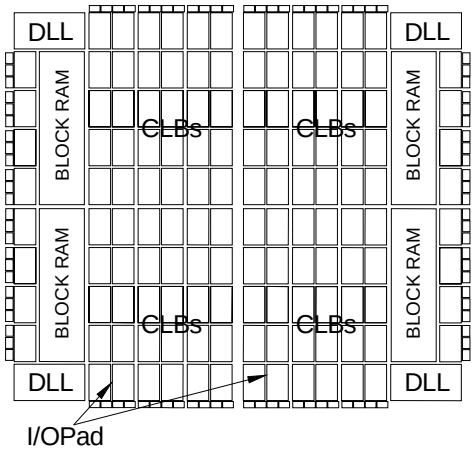

Figure 2 Internal structure of Xilinx Spartan-II

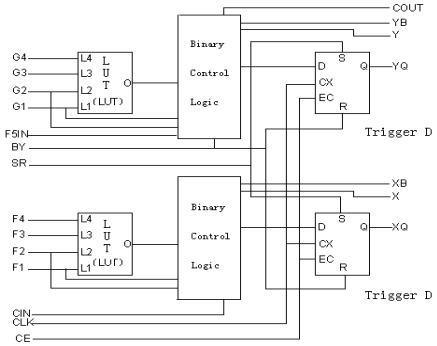

Figure 3 Slices structure of Xilinx Spartan-II

Spartan-II mainly includes CLBs (Configurable Logic Block), I/O Pad, RAM Pad and the programmable wire (not indicated).In Spartan-II, a CLB includes two Slices and each Slice includes two LUTs, two triggers and the relevant logics. Slices could be considered as the most basic structure of Spartan-II to realize the logics.

(3) FPGA logic realization principle of LUT structure

For instance, let's see the circuit in Figure 4:

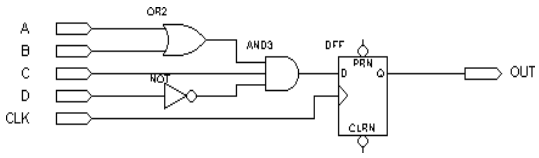

Figure 4 Circuit

A, B, C and D enter the programmable wire through the pins of the FPGA chips and are connected into LUT as address wires. LUT has all the possible logic results written inside and through the address search, the corresponding data is found before output to realize the combined logic. In this circuit, the D trigger is realized by directly using the D trigger behind the LUT. The clock signal CLK enters the exclusive clock channel inside the chip after inputting from I/O pins and is directly connected to the trigger's clock end. The output of the trigger is connected with the I/O pin and

output the result to the pin of the chip. Therefore PLD completes the functions of the circuit indicated in the Figure 4.

III. RECONFIGURABLE SYSTEM ANALYSIS

A .Proposal of the reconfigurable questions

For a long time, people have been using methods of software or hardware to realize the computing work in the electronic system. In actual application, people could choose a most suitable and eclectic plan between the software and hardware methods according to the own requirements.

In the reconfigurable system, the hardware information (configuration information of the programmable devices) could also be dynamically debugged or modified like software program. Thus it maintains the performance of the hardware computing and the flexibility of the software.

B. Analysis of the reconfigurable computing

(1) Meaning of the reconfigurable computing

Reconfigurable computing, RC, for short, is to utilize the FPGA to logically realize the computing tasks. The concept of the reconfigurable computing has already been raised in the 1960s.Currently, the RC has been greatly improved with the main targets to adapt to the requirements of computing tasks through programmable hardware and reach the best performance; while the changes in the hardware structure could adapt to the changes of the computing tasks [2].

(2) Advantages of the reconfigurable computing

The variable features of the reconfigurable computing technology system excellently adapts to the diversified requirements in practical application. Specifically speaking, the advantages are mainly embodied in three aspects:

1) Designers could realize more functions with simpler hardware.

2) Reduce the cost of the system.

3) Shorten the product period.

C. Comparison and analysis between the reconfigurable system and traditional computer system

(1) Basic composition of the system

1) Traditional computer system

The traditional computer system is composed by hardware and software. According to the Von Neumann principle, the hardware structure is composed by five basic parts: respectively being ALU, CU, Memory, Input Device and Output Device [3].

2) Reconfigurable system

The reconfigurable system constructed by reconfigurable computing technologies is usually composed by three parts: Host, RPU(Reconfigurable Processing Unit) and Memory. Please see Figure 5 for details.

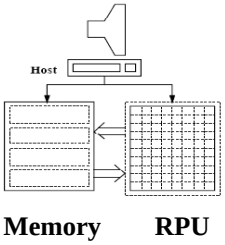

Figure 5 Composition of reconfigurable system

The host is to provide the user interface and I/O services. The compiler and other tools are also located in the host.

RPU is an array composed by one or several FPGA chips. Many FPGA chips provide the configurable I/O pins at the periphery of the chips and input the data at the top of the array and output the data at the bottom. This process is named as the standard configuration process.

Lastly, the most important part is the Memory. As the RPU is pipelining and the Memory has a very high requirement on the bandwidth.

(2) Working principle of the system

1) Traditional computer system

Almost all the working principles of the traditional computer follow the Von Neumann principle and the basic working process is to memorize the order, take the order, analyze the order, perform the order, take the next order and repeat the process again [4].

2) Reconfigurable system

In reconfigurable system, the hardware information (configuration information of the programmable device) could also be dynamically debugged or modified like software program.

Next we will explain the basic working principle of the reconfigurable system with simple example and compare which with the software and hardware realization.

For instance, a certain task is divided into three sub-tasks: A, B and C. Please see Figure 6 for the task flow. We must first complete A and then perform B and C.B and C have no direction connection and thus could be conducted independently.

If it's realized by means of software, the three tasks are performed in serial. If not considering the low performing

speed of the software, the non-parallel treatment will cost many extra times.

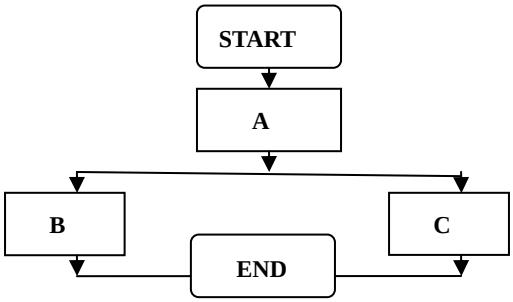

Figure 6 Task flow diagram

The system architecture and the content in the Memory realized by software are shown in Figure 7 and 8.

If it's realized by means of hardware, the B and C tasks could be performed in parallel; in addition to the inherent performance advantages of the hardware, the speed will be much faster than the software. However, the inherent hardware is difficult to be upgraded, not as flexible as the software. The system architecture realized by hardware is shown in Figure 9.

If it could be realized by reconfigurable system, the system architecture is shown in Figure 10.FPGA has two modes of configuration: Configuration 1 completes the task A, please see Figure 11.After task A, the Configurable Circuits, CC reads the Configuration 2 and completes the task B and C in parallel, please see Figure 12.Therefore, the reconfigurable system has both the speed and the parallelism of the hardware means and the flexibility of the software means (by modifying the configuration could complete the system upgrade)[5].

D. Application of the reconfigurable system

From the very beginning when the reconfigurable system is raised, it has won the extensive attention due to its excellence in different fields.

(1) Application in aviation field

Australian scientific satellite FedSat (blast off in December, 2002) takes the leading role to apply the reconfigurable computing technology into aviation area. Thanks to the adoption of the reconfigurable computing technologies, the satellite could change the internal electric lines without returning the ground whereas saving large quantities of time and cost for research[6].Another unique application is the tolerance system, which is used in the spatial technology[7].

(2) Application in military field

The application of the reconfigurable computing technologies in military field is much earlier. US have initiated the application research of the reconfigurable computing in BMD since the early 1950s until now. The Pave Pillar plan of the US air force contributes fairly good reconfiguration capacity to the aviation electronic comprehensive system has applied which successfully to the F-22 military airplanes.

(3) Application in civil field

Firstly, the reconfigurable technologies satisfy the requirements of the auto electronic products on the reliabilities. Secondly, it could satisfy different functional requirements by means of the dynamic modification of the device configurations[8].

Ⅳ. Conclusion

The development of the high-performance computer system is advancing quickly. Nowadays the number of the GFLOPS of FPGA is three times to ten times that of the Pentium chips and some image treatment arithmetic speed is 70 times that of the Pentium and the code attack speed is even 1000 times faster. The reconfigurable technologies based on FPGA are rising quickly and the reconfigurable system will be the latest tendency of the high performance computer system development.

References

[1] Growth Tendency of FPGA. Wireless Technology, Vol.401

[2] Li Renfa, Zhou Zude, Chen Youping. Hardware Structure of Reconfigurable Computing. Computer Research and Development, 2003.

[3] Xu Hongjie. Computer System Guideline. Tianjin: Nankai University Publishing House, 2003

[4] S.A.Guccione, M.J.Gonzalez.A Data-parallel Programming Model for Reconfigurable Architectures.IEEE Workshop on FCCM, 1993.

[5] Reconfigurable computing technologies are evolving into civil arena: .http://www.gd-emb.org/detail/id-31268.html.

[6] Yang You'an, Cui Kemei, Li Zhanchun. Computer Application Foundation. Beijing: Posts and Telecom Press, 2003

[7] J.D.Lohn, G.L.Haith, S.P.Colombano, and D.Stassinopoulos.Towards evolving circuits for autonomous space applications. IEEE Aerospace Conference Proceedings,Vol.5, 2000.

[8] Wang Tao, Wang Feng. Exploration on the Application of Reconfigurable Computing Technologies in Auto Electronic Arena. Electronic Engineering Special.

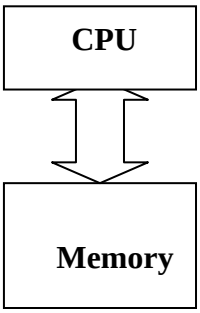

Figure 7 System architecture of the software realization

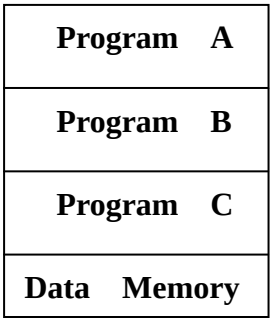

Figure 8 Memory of the software realization

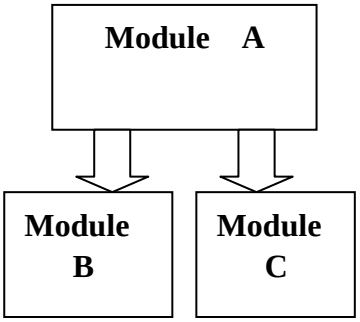

Figure 9 System architecture of the hardware realization

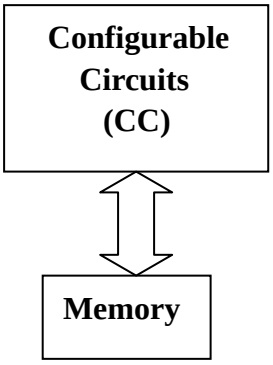

Figure 10 System architecture of reconfigurable realization

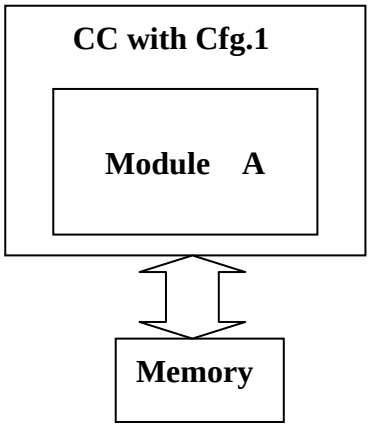

Figure 11 Configuration 1

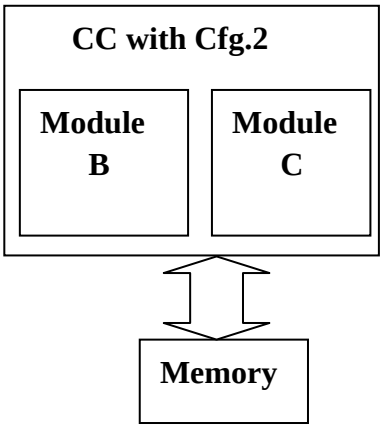

Figure 12 Configuration 2

Table 1 Comparison of the three realization methods of the arithmetic

Arithmetic realization	Hardware	Software	Reconfigurable system
Speed	Fast	Slow	Relatively fast
Parallelism	Realize the parallelism at any meanings	Only realize the order parallelism	Could realize most of the parallelism means
Resources consumption	Change with the applied environment	No change	No change
Development difficulties	Difficult	Easy	Under development
One-off investment cost	Big	Small	Small
To be upgraded	No	Yes	Yes