Digital Ultra Low Voltage High Speed Logic

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Abstract

In this paper we present a differential ultra low voltage gate, which makes use of a keeper function to obtain higher stability and minimizing the concurn of the leakage on the semi floating-gates. Keywords: Ultra low voltage, floating-gate, differential, keeper.

1 Introduction and background

Low power is becoming more and more crucial and in many aspects becoming the number 1 priority when designing new applications. Ultra low voltage CMOS is an approach for producing very low-power CMOS circuits by reducing the supply voltage to several hundred millivolts [1, 2]. To maintain good performance at low supply voltages, the threshold voltages of MOS transistors must also be reduced [3–5]. Unfortunately, this requires a change in the CMOS fabrication process. Because variations in $V_{\rm th}$, when operating in a low-$V_{\rm dd}$ and low-$V_{\rm th}$ environment, cause significant variations in performance, the ultra low power approach lies on the biasing of transistor bodies to adjust thresholds [3]. The primary drawbacks to ultra low power CMOS are that it requires (i) *a change in the fabrication process*, (ii) *additional circuitry to adjust body potential*, and (iii) *additional routing of separate well-voltage ($V_{\rm p\text{-}well}$ and $V_{\rm n\text{-}well}$) references.*

The outline of this paper is as follows: in section 2 key aspects of the ultra low voltage (ULV) gate is presented. Section 3 elaborates on the leakage problem of the ULV gates and presents a solution with a keeper functionality. In section 4 a differential ULV gate including the keeper function is presented. Finally, the paper concludes by emphasising the key aspects of this paper. The simulation results demontrated throughout this paper were obtained by simulations produced in a STM 90nm process environment provided by Cadence.

2 Ultra Low Voltage Floating-Gate Inverter

The ultra low voltage (ULV) gate, illustrated in Fig. 1 were first introduced in [6] and demonstrated with measurements for supply voltage of 0.4V. Moreover, its potential has been simulated to be more than ten times the operating frequency than compared footed domino logic gates resulting in a improved EDP of 20 times better than standard inverter. Further comparisons to CMOS has been elaborated in [7], which also strengthen the ULV gates potential. Furthermore, this gate has been used in the field of power analysis and it has been found to be able to camouflage its instantaneous current dissipation due to the clock drivers [8]. Extracting the joint advantages of this particular ULV gate, we find the combination of high speed and low voltage giving quite good EDP numbers than other known similar logic, such as CMOS and footed domino logic. Although, the ULV inverter is presented here, there are published work on other logical gates, such as NAND and NOR [7].

In general all floating-gates suffer from leakage, some to more extent than other. It is a well-known phenomenon in the field of floating-gate that a frequent recharging strategy include elements which would increase the leakage. The presented ULV gates is classified as semi-floating-gate (SFG) because of the direct connected recharge transistor. The leakage through the drain contact of the recharge transistor will set restrictions for the operating frequency both in terms of high cut-off and low cut-off. The leakage of the semi floating-gate would also affect the inverters ability to reach the rails. Simulation results demonstrating the leakage as a function of the supply-voltage is given in Fig. 2 and a cor-

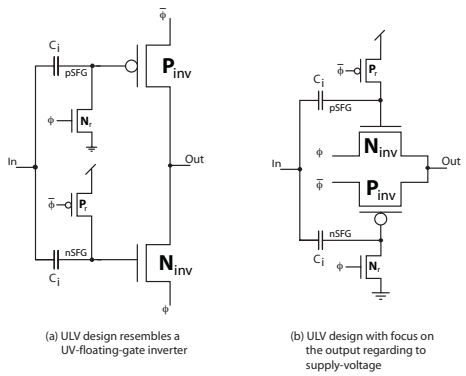

Figure 1: *The figure illustrates the ultra low voltage gate. Both designs are logically and electrically equivalent. In (a) the design clearly shows the inverter and the biasing/recharging of the floating-gate, while (b) is designed to emphasise that the output is not directly connected to the supply voltage.*

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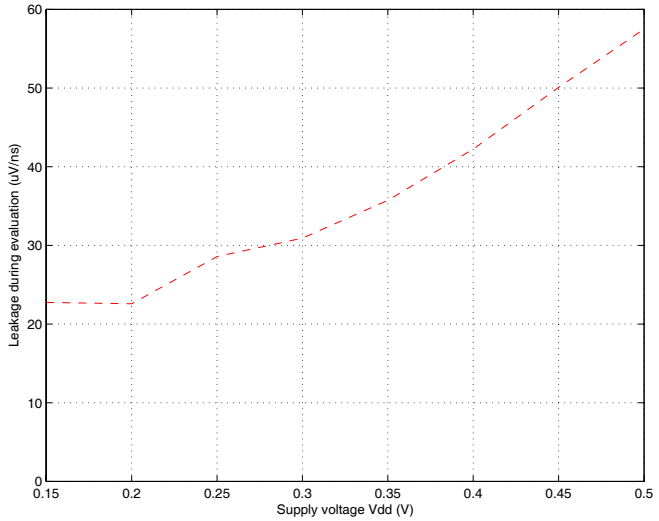

Figure 2: *Simulation results show the leakage of the ULV gate during an evaluation period as a function of low supply-voltages. The leakage is given by $\mu V/ns$.*

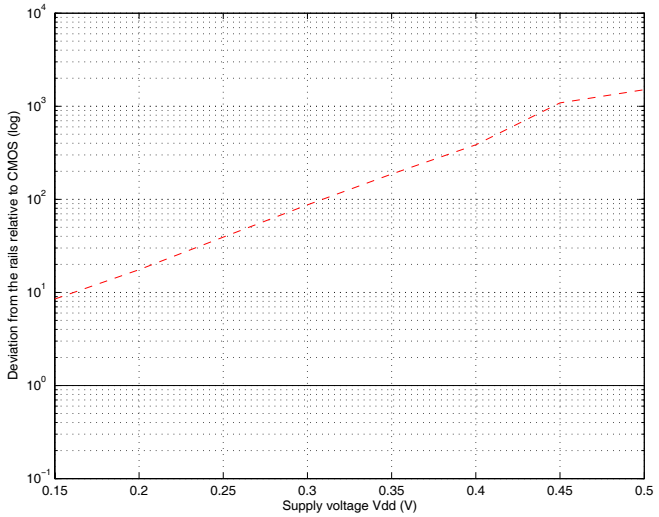

Figure 3: *Simulation results demonstrating the amount of deviation relative to CMOS under given supply-voltages. This behaviour is expected due to the leakage through the diffusion contact of the recharge transistor.*

responding deviation from the rails in Fig. 3. With these two simulation result the lowest operating frequency can be calculated by the formula:

$$f_{low} = \frac{leakage}{NM - deviation} \quad (1)$$

where *deviation* represents the amount of voltage deviation from the rails, *NM* represents the noise margin (typically 25% of V_{dd}) and *leakage* is the amount given in μV/ns.

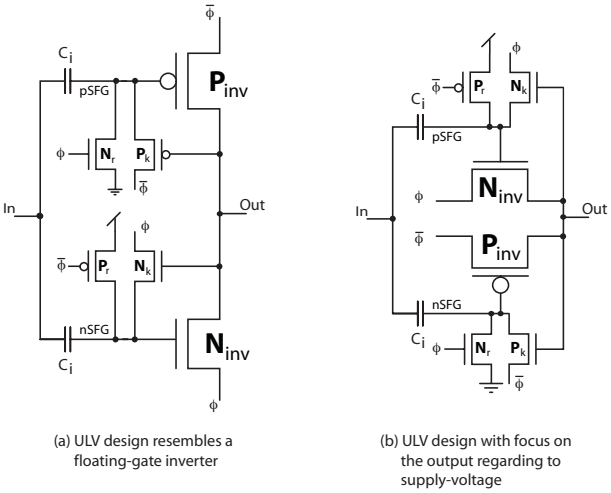

Figure 4: *The ultra low voltage gate is modified by including a transistor which acts as an keeper. The keeper transistors are label N_k and P_k and would contribute to hold the semi-floating-gates potential, thus eliminating the leakage.*

3 Keeper function

In order to face the problem with stability, that is to be able to reach the rails, a design solution is given in Fig. 4. The inspiration may be claimed from the keeper function in domino logic. The additional transistors, labelled N_k and P_k, will at given time keep the charge on the semi floating-gate to a fixed potential. The behaviour during evaluation for a falling transition is given below:

PRE The semi floating-gates, nSFG and pSFG, are set to V_{dd} and Gnd, respectively. The recharge clock, ϕ, is turning off. The input signal, In, is at $V_{dd}/2$ and Out is $V_{dd}/2$.

DUR In starts on a falling transition. nSFG and pSFG see this change with an attenuation factor of C_i/C_{tot}, where C_{tot} is the total capacitance seen from the semi floating-gate. The output drivers, P_{inv} and N_{inv}, starts pulling the output node up. While evaluating, the semi floating-gates are leaking, for nSFG the leakage is from (V_{dd} - ΔV) to Gnd, while for pMOS it is (Gnd - ΔV) to Gnd. The voltage change ΔV is as result of the transition at the input.

POST When In has reached its rail (Gnd), the output drivers are still evaluating the change and try to pull up the output to the rail (V_{dd}). It is here the keeper steps in and holds the nSFG to Gnd and makes sure that the output is as close to the rail as possible and hold the value until next recharge period. Note that the N_k is active and not P_k, due to the falling transition.

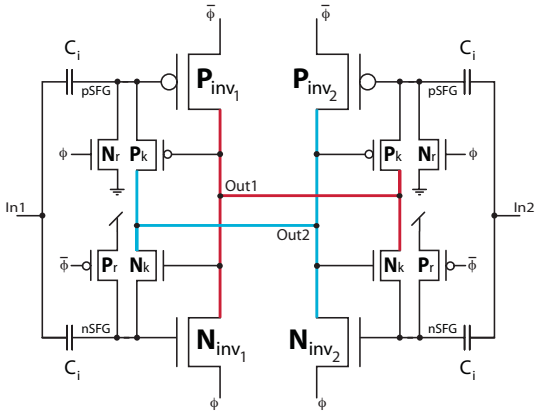

Figure 5: *The ultra low voltage differential semi floating-gate inverter including a keeper function is illustrated. Transistor sizes are kept minimum and matched, the input capacitances are scaled relative to obtain the same voltage attenuation for both nSFG and pSFG.*

Simulation results also verify the theoretical approach and further states the improved stability and lower the leakage due to the included keeper function. Nevertheless, experience with semi floating-gates show that designs with a logical depth of 2 or more, some problems concerning signal delay and clock synchronisation occurs. In that particular case it can actually in worst-case scenario lead to a lock down for the gate. The worst-case in a design, with a logical depth of 2 or more, is where one of the gates output, due to some unexpected reason, is shifted away from $V_{\rm dd}/2$. Even a small voltage change from $V_{\rm dd}/2$ at the output would lead to a lock down to either rails. The lock-down can be avoided if the keeper transistors are not connected to the same reference as the recharge. One very interesting gate to examine in more details are a differential design of the ULV gate with keeper. A differential ULV gate has not, to our knowledge, been published.

4 Differential ULV gate with keeper

In a differential ULV gate, the keeper really gets to be used for more than its potential. The benefit of having the keeper is gained both through keeping a fixed potential for the semi floating-gate and to actually turn "more" off those transistors which should be off. The main benefit for having a differential design is that the opposite output signal is accessible and thus can be connected to the keeper transistors instead of a reference which could lead to a lock down. In Fig. 5 a differential design of the ULV gate including keeper function is illustrated. From the simulation results presented in Fig. 6 the keepers contribution in holding the nSFG down to Gnd is clearly visual. This differential design, called ULV diff, would consume approximately the same amount of dynamic power as the ULV, but have the same static dissipation as CMOS. Furthermore, motivation for differential design can also be found in the context of power analysis, were one of the main countermeasure is to use differential design.

In the following the ULV diff and the ULV are compared to standard CMOS. The simulation conditions has been the same for each logic style, though minimum matched output transistors. The recharge and keeper transistors are kept minimum and the input capacitances are 0.7fF and 1fF for nSFG and pSFG, respectively. Figure 7 and Fig. 8 reinforce the real benefit of the stability and the leakage properties of the ULV diff related to ULV. In Fig. 9 and Fig. 10 the current dissipations are shown. We like to stress that the dissipation behaviour of the ULV diff is gaining the best from both logic styles, ULV and CMOS. The improvement and as a figure of merit is the EDP for the ULV diff and ULV relative to CMOS given in Fig. 11. In order to include the stability factor and to have a more fair comparison, the deviation factor relative to CMOS is multiplied to the EDP. Fig. 12 shows the real improvement in ULV diff compared to ULV. The interesting point to extract from all these data is that the optimal point is to have $V_{\rm dd} = 0.35$ V and that gives a improvement of approximately 5 times better for ULV diff than CMOS and approximately 100 times better for ULV diff than ULV.

5 Conclusion and discussion

In this paper we have introduced a new logic style which is to improve the ULV gates possibility to pull to the rail and to neglect the leakage on semi floating-gates. The presented design, differential ULV gate, make use of a

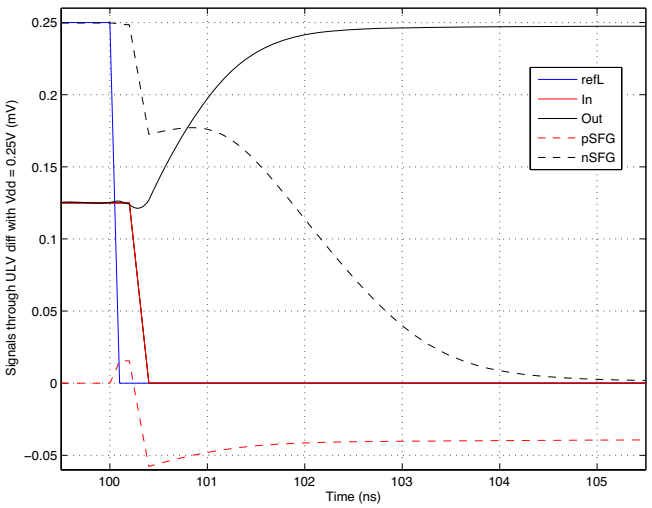

Figure 6: *Simulation results showing all signals in the differential ULV gate during evaluation. As seen from the results the keeper functions steps in at approximately 101 ns and pulling the nSFG down to Gnd.*

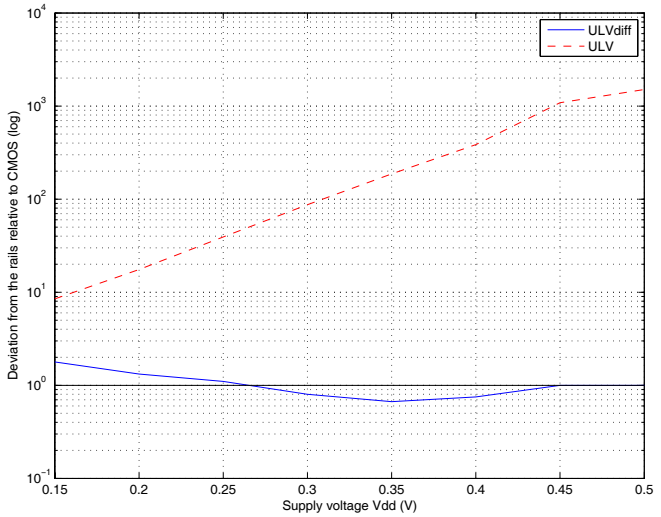

Figure 7: *Simulation results showing the deviation for the ULV diff and the ULV relative to CMOS.*

keeper function and the EDP*stability is found to be approximately 5 times better than CMOS and approximately 100 times better than ULV.

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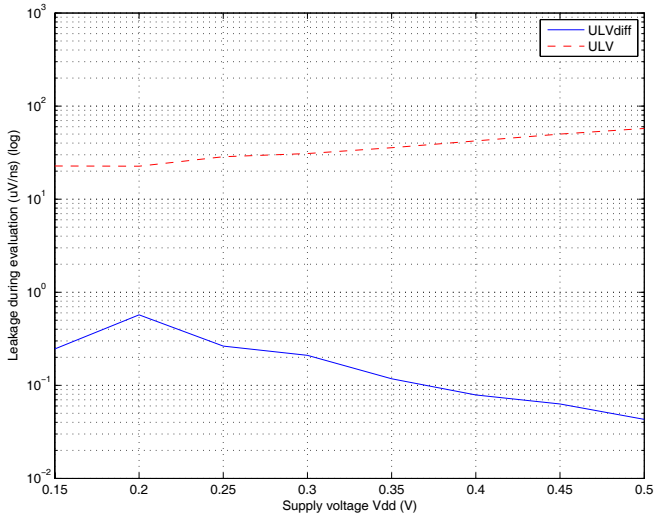

Figure 8: *The leakage of the semi floating-gate affecting the output during the evaluation period.*

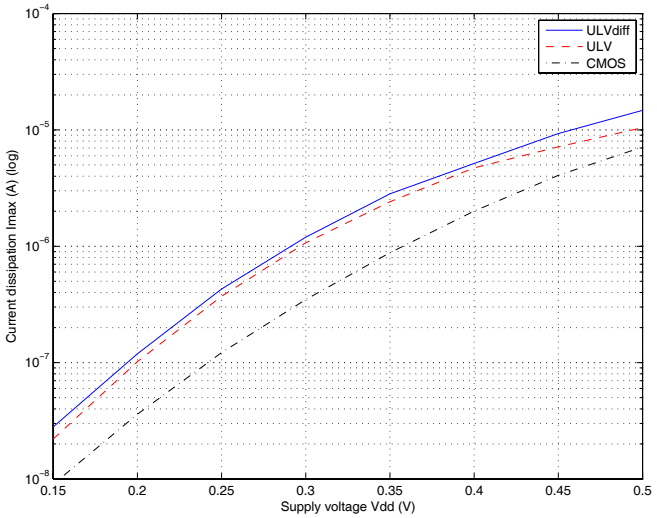

Figure 9: *The maximum current dissipation (dynamic dissipation) for all three styles.*

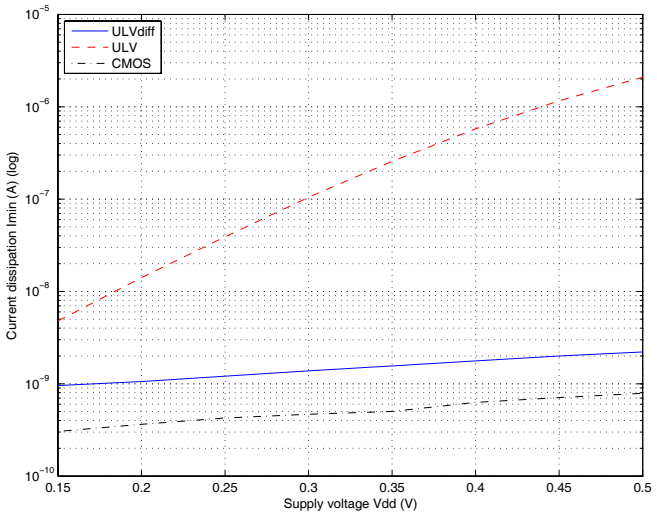

Figure 10: *The minimum current dissipation (static dissipation) for all three logic styles.*

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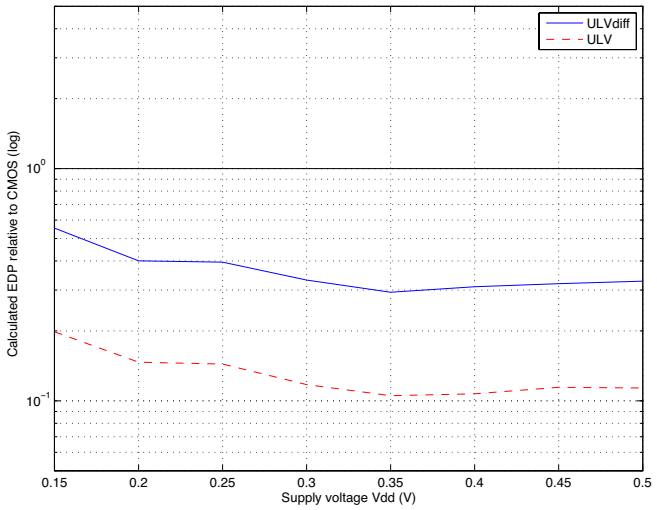

Figure 11: *Simulation results for the EDP for the ULV diff and the ULV relative to CMOS.*

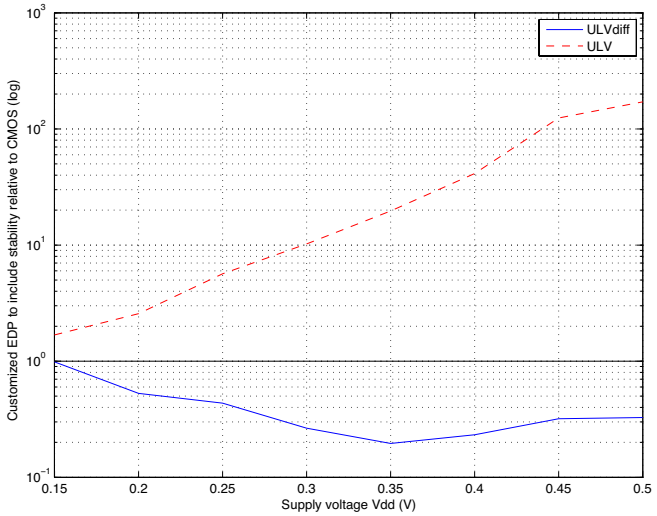

Figure 12: *Simulation results for the EDP*stability for ULV diff and ULV relative to CMOS. The results show a optimum point at* $V_{\mathrm{dd}} = 350\ mV$.