Differential Voltage-to-Frequency Converter for Telemetry

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***Abstract*— A simple circuit technique to realize differential voltage-to-frequency converter suitable for telemetry is presented. The realization method employs second-generation current conveyors in connection with Set-Reset latch to generate the oscillating output signal whose frequency is proportional to the difference between two input voltages. The converter gain can be easily adjusted through the variation of a single resistor. Experimental results are used to confirm the operational characteristics of the proposed converter.**

***Index Terms*—voltage-to-frequency converter, voltage-controlled oscillator, telemetry, CCII-based circuit.**

I. Introduction

A voltage-to-frequency converter (VFC), or voltage-controlled oscillator (VCO), is very useful in measurement and signal conditioning systems. Its applications can be found in data conversion circuit [1] and sensor-based data acquisition systems [2]-[3]. A linearity of its voltage-frequency relation then becomes one of the most important problems to be considered [4]. In the past, one approach to realize the differential VFC, defined as δVFC, whose output frequency is proportional to the difference between two input voltages has been reported in [5]. This circuit was implemented in bipolar technology with low supply voltage. Its operating frequency can be adjusted via an external capacitor. The major advantages of this approach are that a frequency offset can be controlled and a low temperature coefficient of frequency can be obtained. However, this technique requires perfectly matched bipolar transistors and has the complex structure. For the ease of hardware implementation and low cost in design, the simple δVFC using commercially available devices is introduced in this paper. The proposed δVFC is based on second-generation current conveyors (CCIIs) and Set-Reset (S-R) latch similar as the concept in [6]. However, the circuit design is developed to convert the difference between two measured voltages from sensors into the pulse train for telemetry applications. The proposed δVFC can be connected with sensors providing differential voltage output such as strain gauge bridges, an effect of stress can be determined by the frequency measurement [7]. Experimental results showing the performances of the proposed δVFC are also included.

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II. Proposed Circuit Configuration

A. Second-generation Current Conveyor

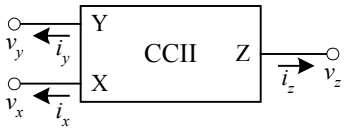


Fig. 1 Circuit symbol of the CCII.

The CCII, whose circuit symbol is shown in Fig. 1, is a universal active element with port relations described by the following matrix equation

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{1}$$

From (1), the current at port Y is zero. The voltage at port Y is accurately transferred to port X. The current supplied to port X is conveyed to port Z, where it is supplied either positive polarity (in positive CCII or CCII⊕) or negative polarity (in negative CCII or CCIIΘ).

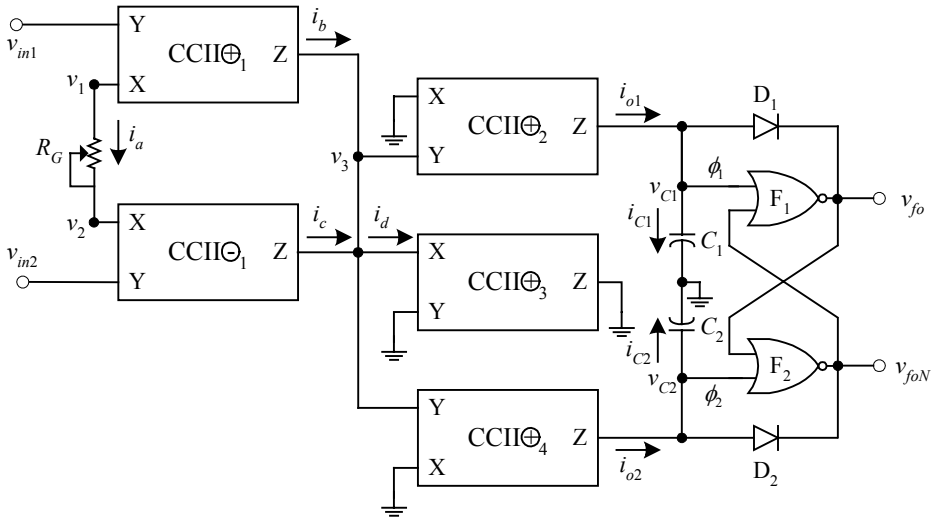
B. Proposed δVFC

The circuit diagram of the proposed δVFC is shown in Fig. 2(a). The CCII⊕$_1$-CCIIΘ$_1$ and the variable resistor R_G form as an instrumentation amplifier with high common-mode rejection ratio (CMRR) [8] to provide the current i_d proportional to the difference between two input voltages v_{in1} and v_{in2}. The CCII⊕$_2$-CCII⊕$_4$ are employed to generate the currents i_{o1} and i_{o2}. The NOR gates F_1-F_2 function as the S-R latch, which has two inputs, the reset (ϕ_1) and set (ϕ_2) signals, and two outputs, labeled v_{fo} and v_{foN}, where v_{foN} is normally the complement of v_{fo}. The diodes D_1 and D_2 are connected to control the capacitors C_1 and C_2, respectively, to be charged or discharged. Based on the operations of the CCII⊕$_1$ and CCIIΘ$_1$, the current i_a flowing through the variable resistor R_G and the currents i_b and i_c can be stated as

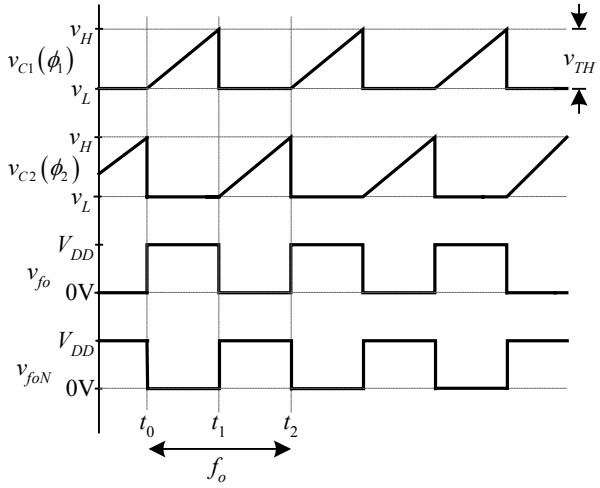
$$i_a = \frac{v_1 - v_2}{R_G} = \frac{v_{in1} - v_{in2}}{R_G} \tag{2}$$

$$i_b = i_a \tag{3}$$

$$i_c = i_a \tag{4}$$



(a) Circuit diagram



(b) Periodic voltage signals

Fig. 2 Proposed δVFC.

Considering at node v_3, the current i_d can be given by

$$i_d = i_b + i_c \tag{5}$$

Substituting (3) and (4) into (5) gives

$$i_d = 2i_a \tag{6}$$

By the actions of the CCII⊕$_2$-CCII⊕$_4$, two currents i_{o1} and i_{o2} can be expressed as

$$i_{o1} = i_{o2} = i_d \tag{7}$$

Solving for the currents i_{o1} and i_{o2} by using (2), (6), and (7), it thus results in

$$i_{o1} = i_{o2} = \frac{2(v_{in1} - v_{in2})}{R_G} \tag{8}$$

The sequential operation of the proposed δVFC to generate tunable periodic voltage signals as illustrated in Fig. 2(b) can be explained as follows.

For the first instance at $t = t_0$, it is assumed that the states of the S-R latch outputs v_{fo} and v_{foN} are set to high and low, respectively. The diode D_2 is turn on, the capacitor C_2 will be discharged. When the voltage v_{C2} is approximately equal to the lower threshold voltage v_L, the signal ϕ_2 becomes low state. Simultaneously, the capacitor C_1 is left in the charge state by reversing D_1. When the C_1 charge reaches the voltage v_{C1} to the upper threshold voltage v_H at $t = t_1$, the signal ϕ_1 is then set to high. The change of v_{C1} can be stated as

$$\Delta v_{C1} = \frac{i_{o1}(t_1 - t_0)}{C_1} = \frac{i_{o1}\Delta t_{10}}{C_1} = v_H - v_L = v_{TH} \tag{9}$$

where v_L and v_H are defined as the maximum voltage and the minimum voltage guaranteed to be recognized as the low state and the high state, respectively.

Next, the S-R latch will force the output signals v_{fo} and v_{foN} to be low and high, respectively. The capacitor C_1 is discharged in the on state by D_1. When the voltage v_{C1} is nearly close to the lower threshold voltage v_L, the signal ϕ_1 is set to low. Otherwise, the capacitor C_2 is charged in the off state by D_2. When the voltage v_{C2} increases to the upper

threshold voltage v_H at $t = t_2$, the signal ϕ_2 will be set to high state. The change of v_{C2} can be written as

$$\Delta v_{C2} = \frac{i_{o2}(t_2 - t_1)}{C_2} = \frac{i_{o2}\Delta t_{21}}{C_2} = v_H - v_L = v_{TH} \tag{10}$$

The latch output signals v_{fo} and v_{foN} then are forced again to high and low, respectively. From above discussion, the periodic signals can be generated. The output frequency f_o, or rate of repetition, of the proposed δVFC can be calculated by using (9) and (10) as

$$f_o = \frac{1}{\Delta t_{10} + \Delta t_{21}} = \frac{i_{o1} i_{o2}}{(i_{o1} C_2 + i_{o2} C_1) v_{TH}} \tag{11}$$

By substituting (8) into (11) and setting $C_1 = C_2$, the output frequency f_o can now be rewritten as

$$f_o = \frac{(v_{in1} - v_{in2})}{R_G C_1 v_{TH}} \tag{12}$$

From (12), it is evident that the proposed δVFC as shown in Fig. 2(a) provides the output frequency directly proportional to the difference of two input voltages. Moreover, the output frequency can be easily adjusted through the variation of the variable resistor R_G.

III. Performance Analysis

In practical realization, the equivalent input resistance at port X of the CCII, R_x, is the major factor that contributes to the inaccuracy of the proposed δVFC. The relations between the difference of two input voltages (v_{in1}–v_{in2}) and the output currents i_{o1} and i_{o2} can be accurately stated as

$$i_{o1} = i_{o2} = \frac{2(v_{in1} - v_{in2})}{R_G}(1 - \varepsilon_{Rx}) \tag{13}$$

where ε_{Rx} is the error due to the resistance R_x, which can be given by

$$\varepsilon_{Rx} = \frac{2R_x}{R_G + 2R_x} \tag{14}$$

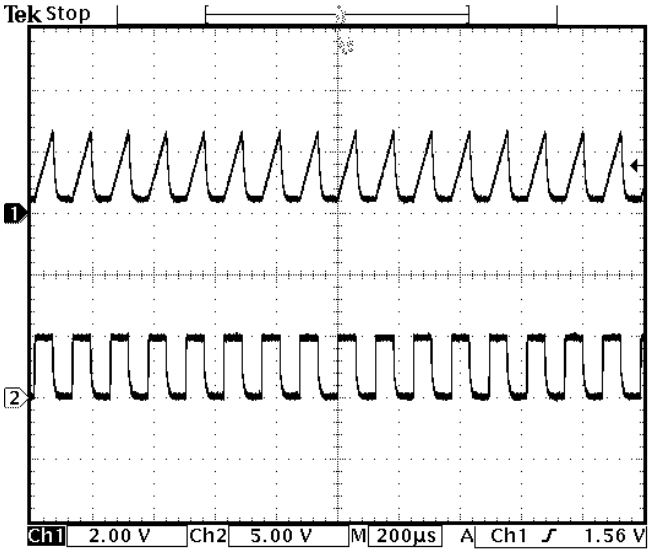
Consequently, the output frequency f_o including the error ε_{Rx} then is

$$f_o = \frac{(v_{in1} - v_{in2})(1 - \varepsilon_{Rx})}{R_G C_1 v_{TH}} \tag{15}$$

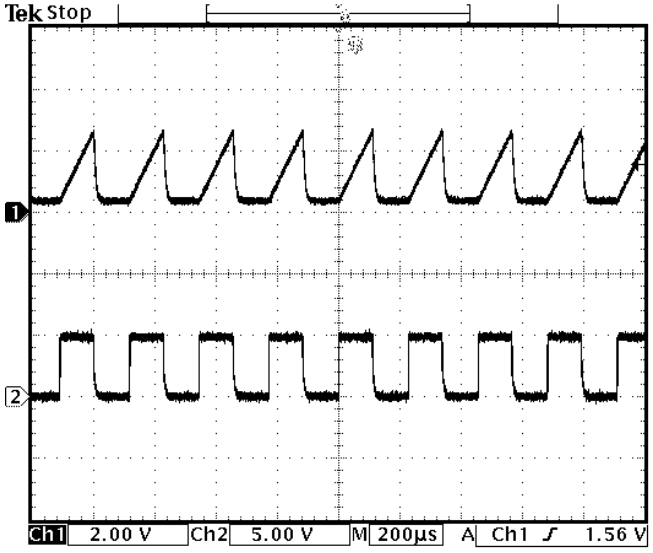
For example, if R_G = 2kΩ, and in the Analog Device IC AD844 configured as the CCII⊕, the resistance R_x ranges from 50Ω to 65Ω, then the error ε_{Rx} will be in the range of 4.76%-6.1%.

IV. Experimental Results

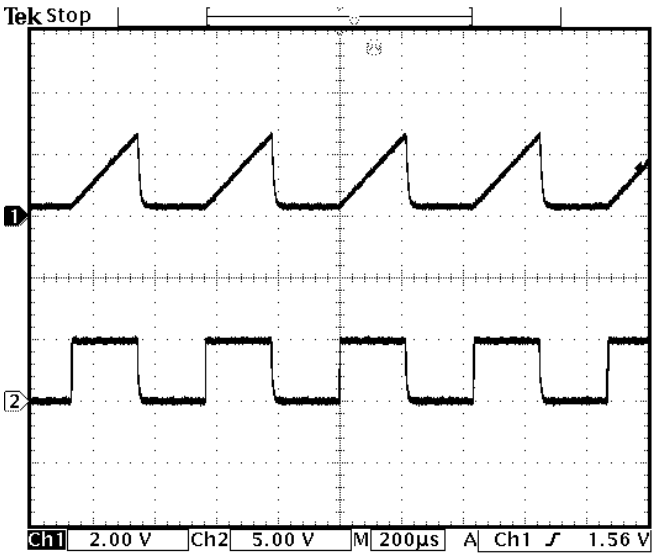
To verify the performances of the proposed δVFC, the



(a)



(b)



(c)

Fig. 3 Measured results of the proposed δVFC for v_{in1}–v_{in2} = 100mV and the resistor R_G: (a) 0.5kΩ; (b) 1kΩ; (c) 2kΩ. (upper trace: Reset signal ϕ_1, lower trace: Output v_{fo}.)

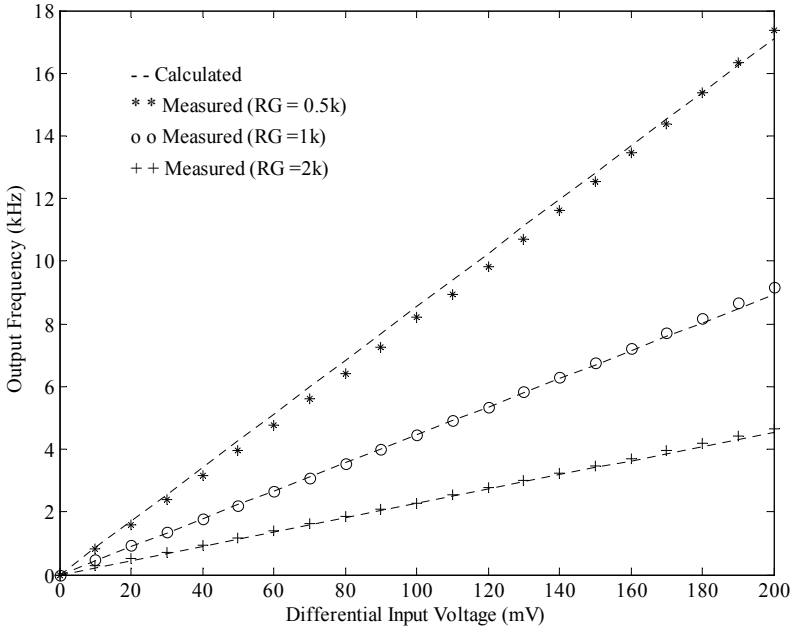


Fig. 4 Plots of the measured output frequency f_o against the differential input voltage (v_{in1}–v_{in2}).

circuit in Fig. 2(a) was experimentally implemented using commercial available IC AD844 and 4001BC as CCIIs and NOR gates, respectively. The supply voltages of the AD884 and 4001BC were set to +5/–5V and +5V/0V, respectively. The 5% tolerance capacitors C_1 and C_2 were set to 10nF.

Figs. 3(a)-3(c) show the measured results of the proposed δVFC for three differential values of the resistor R_G i.e. 0.5kΩ, 1kΩ, and 2kΩ, respectively, where the differential input voltage (v_{in1}–v_{in2}) = 100mV was applied. In Fig. 3(a), the voltage v_{TH} = 2.34V and the output frequency f_o = 8.217kHz are observed. In Fig. 3(b), the voltage v_{TH} and output frequency f_o as measured are about 2.24V and 4.452kHz, respectively. In Fig. 3(c), the voltage v_{TH} = 2.20V and the output frequency f_o = 2.287kHz can be measured. Whereas the calculated frequency values using (12) are about 8.547kHz, 4.464kHz, and 2.273kHz for R_G = 0.5kΩ, 1kΩ, and 2kΩ, respectively. It is obvious that the measured output frequencies agree with the calculated values.

Fig. 4 displays plots of the measured output frequency f_o against the differential input voltage (v_{in1}–v_{in2}) for three differential values of the resistor R_G. The differential input voltage was varied in the range of 0-200mV. It is apparent that the output frequency f_o can be linearly increased by increasing differential input voltage (v_{in1}–v_{in2}). Close agreement between the calculated values and the measured values have been demonstrated by the plots.

V. Conclusion

The circuit technique using commercially available devices has been described to realize the δVFC. Since the proposed method employs the concept of CCII-based instrumentation amplifier with good CMRR performance to support the differential input voltage. Then the proposed δVFC has sufficient characteristics for sending measured signals from sensors providing differential voltage output in the transmitter part of telemetry. In addition, the proposed δVFC offers the following advantages.

- simple configuration.
- ease of hardware implementation by using available ICs.
- ease of gain adjustment via the single resistor.
- linear voltage-frequency relation.

Experimental results demonstrate that proposed δVFC functions correctly.

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