A Low Power Small Area Multi-bit Quantizer with A Capacitor String in Sigma-Delta Modulator

Xuxia Wang, Jian Xu, and Xiaobo Wu†

***Abstract*—An ultra-low power area-efficient fully differential multi-bit quantizer used in Sigma-Delta modulator (SDM) is presented. The quantizer is named as capacitor-string area-efficient (CSAE) quantizer since instead of the typical resistor string, it employs a capacitor string to avoid static power consumption. Furthermore, a novel circuit configuration with saving half number of comparators is applied to it to save area for cutting cost of chip. The novel multi-bit quantizer is designed in a standard 0.35μm CMOS process. Simulation results show that a 17-level CSAE quantizer clocked at 32 kHz achieves a power consumption of 0.225μW when the power supply voltage is 1.8V. Its area is 0.145mm^2. Compared with traditional design, the proposed CSAE quantizer saves 81% power and 37% area and thus is suitable for ultra-low power applications.**

***Index Terms*-ultra-low power, area-efficient, SDM, CSAE multi-bit quantizer**

I. Introduction

Analog-to-Digital (AD) and Digital-to-Analog (DA) converters provide the interface between analog and digital circuits. Among prevalent AD converter (ADC) architectures, Multi-bit Sigma-Delta ADCs are more widely used in portable electronic products due to the features like low power, high SN-DR and high resolution. As one of its key modules, the multi-bit quantizer encodes a range of analog values into a set of discrete levels, and its characteristics directly influence the performance of the ADC.

In recent years, most contemporary ADCs use a uniform quantizer. It is the most traditional architecture comprising of a resistor string, comparator bank and encoding logic [1]. To get further improvement in resolution, a semi-uniform quantizer [1], which is constructed in the same way as a uniform quantizer, is applied in modulators by using varying quantization steps depending on the input signal. However, as the rapid development of portable equipments powered by batteries, the ADC with low power and area efficient features is demanded by market and attracts a lot of attentions. Therefore, this paper focuses on the reduction of the power consumption and area of multi-bit quantizer.

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As an important part of modulator, both uniform and semi-uniform quantizers have their own limitations. The resistor string consumes most power of quantizer in low frequency applications. Assuming the total dissipation of the modulator is less than 10uW, to avoid that the quantizer consumes most power, the resistance of quantizer should be as much as million Ohms. However, it will results in unacceptable area increasing while static power is still nonnegligible.

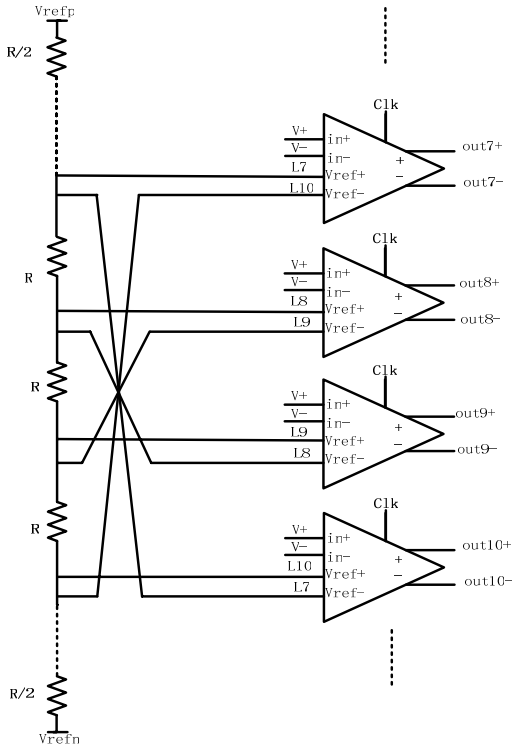

Fig.1 Traditional Quantizer

In this paper, an ultra-power and area efficient multi-bit quantizer with a capacitor string and half number of comparators (CSAE quantizer) for Sigma-Delta modulator is proposed. Section II describes the traditional quantizer architecture. An improved traditional quantizer with half number of comparators and CSAE multi-bit quantizer are introduced in Section III and Section IV, respectively. And in Section V, the simulation results and comparison with traditional ones are presented. Finally, the conclusion is given in Section VI.

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II. Traditional Quantizer

Most of the reported commercial Sigma-Delta modulators use single-bit internal quantizers due to the non-linearity of feedback DAC. But for a given oversampling ratio, the performance of the modulator using single-bit quantizer is limited. Therefore, employing a multi-bit quantizer instead of a single-bit quantizer is a choice to increase the resolution of a Sigma-Delta modulator for a given order. And the most popular structure of multi-bit quantizer adopted by designers is shown in Fig.1. It is realized by a resistor string, comparator bank and encoding logic.

There are two ways to achieve multi-bit quantizers: uniform quantization steps and non-uniform quantization steps. The quantization step of the non-uniform quantizer is increasing as the input signal values increase so that smaller input values affect a smaller error and larger input values affect a larger quantization error. Because the non-uniform quantizer requires a precision component matching and it is hard to achieve VLSI fabrication, a uniform quantizer is adopted in this design.

A uniform quantizer quantizes the input signal to a finite set of output values, and it needs two operations: sampling the analog signal and quantizing its amplitude [3]. The principle of quantization is shown in Fig.2. When the YFS is the maximum output value, separation between the output levels is

$$\Delta = \frac{Y_{FS}}{2^n - 1} \tag{1}$$

And the separation between the input levels is

$$V_{LSB} = \frac{X_{FS}}{2^n} \tag{2}$$

The magnitude of V_{LSB} is known as least-significant-bit (LSB) of the quantizer.

In order to simplify the circuit and reduce the power, dynamic comparator without pre-amplifier is chosen. The dynamic comparator shown in Fig.3 consists of two cross coupled differential pairs with inverter latch at the top [2]. Comparison is made once every clock period based on the inverter currents that are related to the inputs. However, there is a big problem here. The comparator works wrong because of the V-reference glitch. For the V-reference signal connects to the differential pair of comparator directly, the clock feed-through current is caused. To analysis the circuit clearly, the equivalent circuit is illustrated in the Fig.4. The parasitic capacitor between the Φ switch and the input differential pair is regarded as capacitor C1 while the parasitic capacitor between the gate of NMOS and ground is regarded as capacitor C2. Transfer function of the equivalent circuit is recognized in Eq.3

$$H(s) = \frac{sRC_1}{1 + sR(C_1 + C_2)} \tag{3}$$

At the same time, we know $V_0(1+e^{-sT_0/2})^{-1}s^{-1}$ is the S transforms of *clk(t)*.

$$clk(t) = \begin{cases} 0, \ for \ \ t<0 \ \ and \ \ kT_0 + \frac{T_0}{2} < t < (k+1)T_0 \\ V_0, \ for \ \ kT_0 < t < kT_0 + \frac{T_0}{2} \end{cases} \tag{4}$$

It is easy to obtain Vref(s) which is the S transforms of Vref(t). Vref(s) equals to clk(s)H(s) shown in Eq.5.

$$V_{ref}(s) = H(s) \times clk(s) = \frac{V_0 RC_1}{[1 + sR(C_1 + C_2)](1 - e^{-sT_0/2})} \tag{5}$$

The formula $1 - e^{-sT_0/2}$ can be ignored because the glitch is caused when the clock signal goes high. So the above equation is simplified as showed in Eq.6.

$$V_{ref}(s) \approx \frac{V_0 RC_1}{1 + sR(C_1 + C_2)} \tag{6}$$

$$V_{ref}(t) \approx V_0 RC_1 e^{-R(C_1+C_2)t} \tag{7}$$

As shown in Eq.7 that the value of its inverse transform *Vref(t)* is related to the elements C1, C2, R and V0. When the values of element R and C1 grows, the value of *Vref(t)* increases. Simultaneously, the value of *Vref(t)* also can be reduced by increasing the value of C2. By paralleling a small capacitor with the differential pair, the high frequency response can be eliminated. Hence, the glitch caused by the clock feed-through is reduced effectively. The improved comparator with small capacitor connecting to the Vref interface is shown in Fig.3.

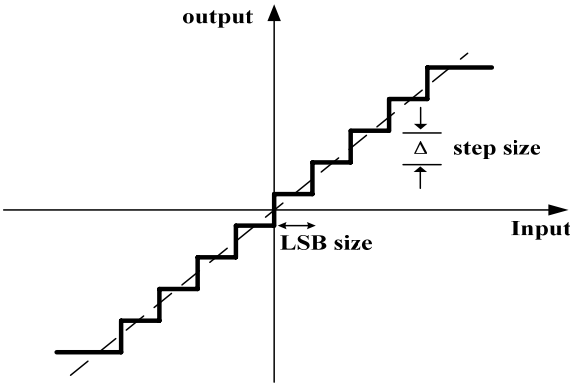

Fig.2 The principle of quantization

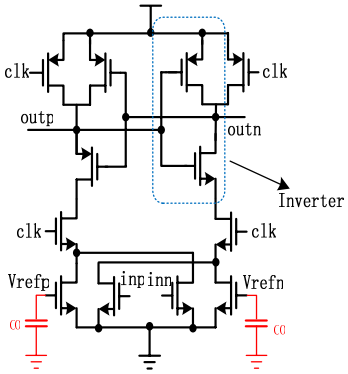

Fig.3 Dynamic comparator

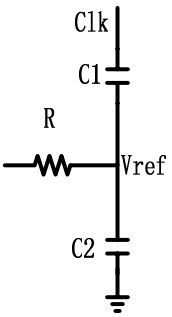

Fig.4 Equivalent circuit of the feed-through circuit

III. Improved Quantizer with Half Number of Comparators

As introduction mentions, the aim of this work is to reduce the power and the area of the chip. Therefore, to find a new architecture is important. An improved quantizer with half number of comparators is proposed in this section.

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It is known that the dynamic comparator shown in Fig.3 is only comparing differential Vin(inp - inn) with differential Vref(Vrefp – Vrefn) in effect [3]. First, considering the top comparator and the bottom comparator shown in Fig.1, if the voltages Vin(Vin^+ - Vin^-) is greater than Vref(Vref1 – Vref16), the output signal O1+ of the top comparator is high. In fact as long as the voltages Vin is positive, the output signal O16+ always goes to ground. Only when the voltages Vin equals to Vref(Vref1 – Vref16), O16+ begins to change to be high. Second, the value of the differential input Vin of the bottom comparator, at what the output O16+ changes, is just the inverse value of that of the top comparator. Hence, given that the differential input of the bottom comparator is (Vin^- - Vin^+) other than (Vin^+ - Vin^-), the outputs of the top and the bottom comparators is exactly the opposite. The above principle applies to the other 14 comparators either. From what has been discussed above, it can be seen clearly that if the input signal Vin is controlled before connecting to the comparators, about half number of comparators can be avoided to achieve the function.

After a detailed analysis of the traditional multi-bit quantizer, one comparator is adopted to generate the controlling signals. The controlling circuit is illustrated in Fig.5 which consists of a comparator, a delay module and the signal path. Before connecting to the comparators, the input signals are controlled by the Φ_a and Φ_b signals through from the delay module. As a result, the greater signal will be selected to go through the positive signal path connecting to comparator's inp input and the smaller signal is chosen to go through the negative signal path. By the above method, the input signal is quantized to only 8 states instead of 16 states as before. Coding logic will code this states into a temperature code.

By the above analysis, the quantization is the same as the traditional quantizer, also, the idea of cutting down about half number of comparators is to be effectively verified.

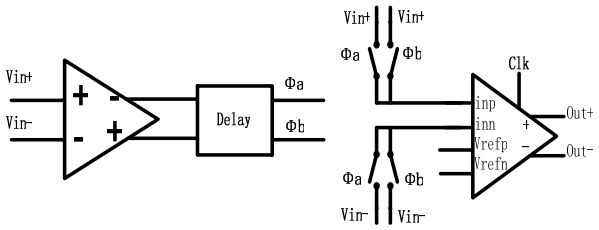

Fig.5 The controlling circuit of quantizer

IV. QUANTIZER WITH A CAPACITOR STRING

Although the above method has cut down about half number comparators, the main drawback has not been overcome. The power consumption is not reduced obviously. As we know, capacitor in circuit almost consumes transient power without static power. Therefore, Quantizer with a string of capacitors and half number of comaprators (CSAE quantizer) is proposed in this section. Specific analysis is as follows.

A. Structure selection

The voltage distribution circuit is shown in Fig.6. Φ and reset are two non-overlap clocks. V_{ref} is the expected reference voltage. C_0 is the parasitical capacitor of the comparator. 5 switches are alternative to control distributing the voltage, so there are total 31 different structures to generate the reference voltage. Among those structures, only 12 can be adopted to realize the function in effect. For example, the reference voltage can't be generated exactly when there is only Φ5 switch, neither is necessary to use all the 5 switches. If there are no charge injection and no leakage currents, the following equations are given in [4]:

$$V_{ideal} = \frac{V_{top}C_1 + V_{cmo}C_2}{C_1 + C_2} \tag{8}$$

$$V_{ref} = \frac{C_2}{C_1 + C_2 + C_0}V_{cmo} + \frac{C_1}{C_1 + C_2 + C_0}V_{top} \tag{9}$$

In the above equations, V_{ideal} means the expected voltage while V_{ref} is the actual voltage influenced by the parasitical capacitor C0. It is seen that the value of C0 should be as small as possible for better accuracy. Or, increasing the capacitance of C1 and C2 also does better to the accuracy. As shown in Fig.6, the Φ5 switch can be ignored, because its parasitical capacitor will be added to C0 when the Φ5 switch is on. Scanning the reference voltage Vref of all the 12 structures, three typical modes are posted in Fig.7 (a) (b) and (c), respectively. The following equations are present to illustrate the principles of the distribution. Q_x and V_x are the charge and voltage at node A with reset switches on while Q_x' and V_y are those when the reference voltage is generated.

$$Q_x = V_x C_0 \tag{10}$$

$$Q_x^{'} = -(V_{top} - V_y)C_1 - (V_{cmo} - V_y)C_2 + V_y C_0 \tag{11}$$

In the Fig.7 c, there is no charge flowing from the capacitor C0 during phase reset. So the charge flows can be determined as follows:

$$Q_x = Q_x^{'} \tag{12}$$

$$V_y = \frac{V_{top}C_1 + V_c C_2 + V_x C_0}{C_1 + C_2 + C_0} \tag{13}$$

$$\begin{aligned} V_y - V_{ideal} &= \frac{(V_x - \frac{V_{top}C_1 + V_c C_2}{C_1 + C_2})C_0}{C_1 + C_2 + C_0} \\ &= \frac{(V_x - V_{ideal})C_0}{C_1 + C_2 + C_0} \end{aligned} \tag{14}$$

Therefore, we can definitely get a conclusion from Eq.14 that the closer the V_y achieves to V_{ideal}, the smaller the error between V_x and V_{ideal}. However, seen from the circuits shown in Fig.11 (a) and (b), the above equations, especially Eq.14, are not suitable, because the node A is connected to the sources every time when the reset switches are on. As a result, the circuit shown in Fig.12 (c) is the optimal selection for the design.

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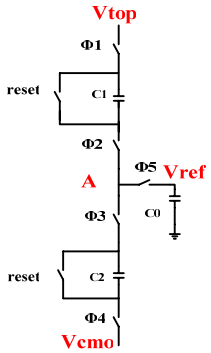


Fig.6 The ideal voltage distribution circuit

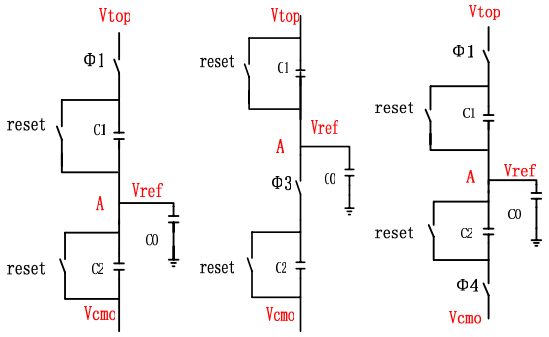


Fig.7 Three modes of reference voltage distribution

B. The actual circuit

As we know, all the switches adopted are ideal in the part of structure selection, actually, there is charge injection and leakage currents as well as parasitical capacitors existed in real circuit. In order to pull less parasitical capacitors in, Pmos switch and Nmos switch are used in the design. The real circuits of voltage distribution are shown in Fig.8.

Considering the influence of the parasitical capacitor, the circuit shown in Fig.8 (a) is analyzed in detail next. In this case, Eq.10~Eq.14 should be rewritten as following:

$$Q_x = V_x(C_0+2C_{p1}+2C_{p2}) - 2V_{dd}C_{p2} \tag{15}$$

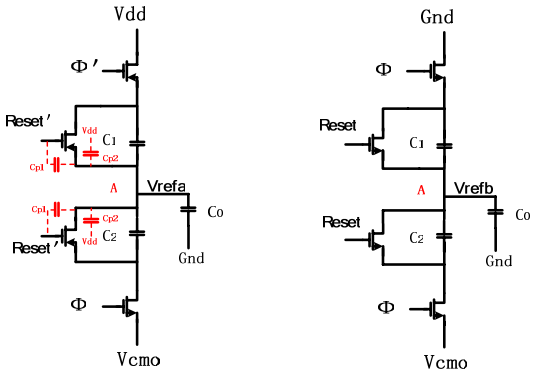
$$Q_x^{'} = -(V_{dd}-V_y)(C_1+2C_{p1}+2C_{p2}) - (V_{cmo}-V_y)C_2 + V_yC_0 \tag{16}$$

$$Q_x = Q_x^{'} \tag{17}$$

$$V_y = \frac{V_{dd}(C_1+2C_{p1}) + V_{cmo}C_2 + V_x(C_0+2C_{p1}+2C_{p2})}{C_1+C_2+C_0+2C_{p1}+2C_{p2}} \tag{18}$$

$$V_y - V_{ideal} = \frac{(V_x-V_{ideal})(C_0+2C_{p1}+2C_{p2}) + 2V_{dd}C_{p1}}{C_1+C_2+C_0+2C_{p1}+2C_{p2}} \tag{19}$$

A conclusion can be definitely got from Eq.19 that the value of V_y is closely related to the value of V_x. As we known, all the switches can still be regarded as resistors even when the reset switches are on, as a result, the source voltage is distributed again to get V_x at node A. Also, charge at node A is redistributed because of the parasitic capacitor of the reset switches. Giving attention to Eq.19 again, the error of (V_y-V_{ideal}) depends on two parts which are the formulas of (V_x-V_{ideal}) and V_{dd}. If (V_x-V_{ideal}) predominates in equation, the error is negative, and so on. The above principle supplies to the circuit shown in Fig.8(b) too.



(a) The first 8 Vref circuit (b) The next 8 Vref circuit

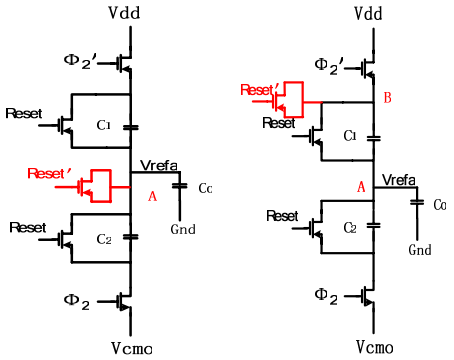
Fig.8 The actual voltage distribution circuit of CSAE multi-bit quantizer

C. Improvement of CSAE multi-bit quantizer

The above circuit should be improved because of the big error shown in Fig.14. The biggest error reaches to 2mV. Eq.16 is rewritten as following:

$$Q_x^{'} = V_y(C_1+C_2+C_0+2C_{p1}+2C_{p2}) - V_{dd}(C_1+2C_{p1}+2C_{p2}) - V_{cmo}C_2 \tag{20}$$

As shown in Fig.8(a), a dummy is added at node A to eliminate the charge injection. So the value of $Q_x^{'}$ and V_y decreases. At the same time, adding a dummy at node B will increase the value of V_y. As a result, by adding dummies in the circuit, the error of Vref can be improved obviously.



(a) (b)

Fig.9 Adding dummies in the circuit

V. Simulation Results

The proposed CSAE quantizer was designed and simulated with a 0.35-μm TSMC CMOS standard process. In Fig.10, the green curve describes the error between the actual reference and the ideal in real circuit with large capacitors whose area are about 15*15 μm^2, and another curve shows the error by using 10*10μm^2 capacitors. It is obviously seen that the error are reduced almost a half by doubling the capacitor. The error of the improved circuit is shown in Fig.11. This picture proves that it is useful to reduce the error by adding several dummies. Fig.12 shows the output spectrum of the 4th-order modulator with CSAE multi-bit quantizer. And Table I gives a comparison among all those quantizers about power consumption and area.

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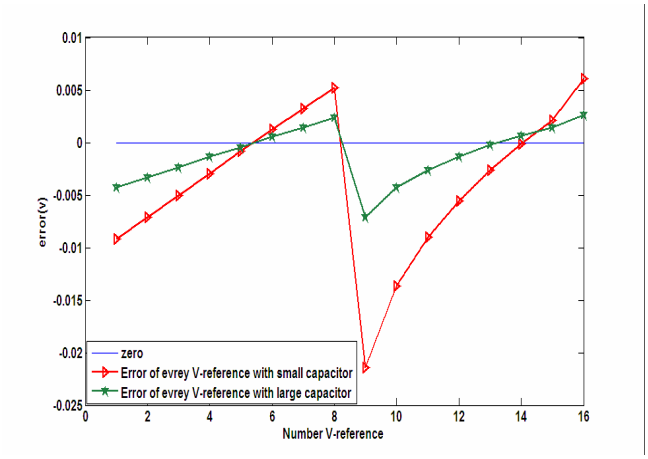

Fig.10 The error of the reference voltage with small and large capacitor

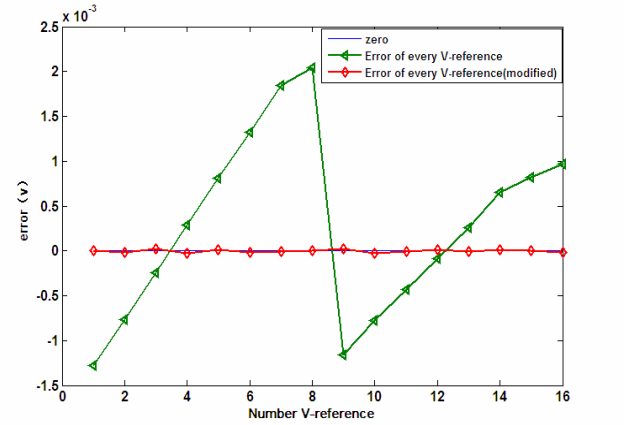

Fig.11 The error curves of the improved circuit

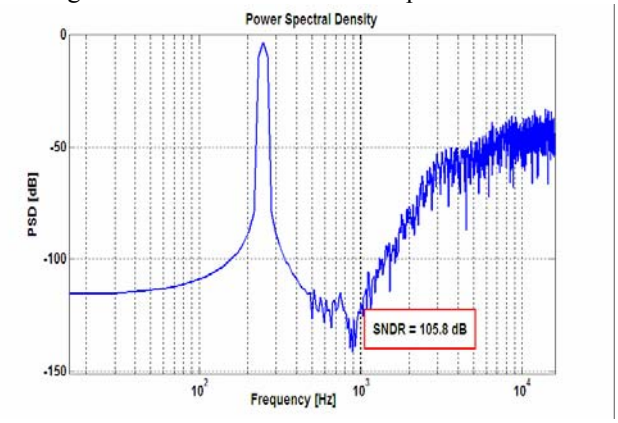

Fig.12 Output spectrum of the Sigma-Delta modulator

Table I A comparison among quantizers about area and power consumption

Quantizer technique	Area(mm^2)	Power consumption (μw)
Traditional Quantzier (3.2M resistor)	0.229	1.192
Traditional Quantzier with half comparators (3.2M resistor)	0.189	1.145
CHAE multi-bit Quantizer ($10*10\mu m^2$)	0.145	0.225

VI. Conclusion

In this paper, an ultra-low power area-efficient fully differential multi-bit quantizer was introduced. The comparison among different quantizers confirms that as to reduction of the power consumption and chip area, the CSAE multi-bit quantizer is the most efficient one. The total power consumption of CSAE quantizer is mininmized to 0.225μw. For a $16*16*10*10\mu m^2$ capacitor string, the total area is about $0.145mm^2$, which is much smaller than traditional quantizer. That means the quantizer could be used to ultra-low power applications.

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References

[1] Roshan Weerasekera, Design of a Semi-Uniform Quantizer for a Second order ∑—Δ Modulator,2001
[2] L. Sumanen, M. Waltari, K. Halonen, "A Mismatch Insensitive CMOS Dynamic Comparator for Pipeline A/D Converters," IEEE ICECS, vol. 1, pp. 32-35, Dec. 2000.
[3] R. Schreier, and G. C. Temes, Understanding Delta-Sigma Data Converters, IEEE Press, 2005.
[4] Michael D.Seeman, Analytical and Practical Analysis of Switche-Capacitor DC-DC Converts,

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