Design of a Charge-Pump PLL for LVDS SerDes

Jianbin Pan, Yuanfu Zhao

***Abstract*—A charge-pump PLL for low-voltage differential signaling (LVDS) serializer/deserializer (SerDes) is presented. A proposed charge pump can greatly reduced non-ideal effects, and a novel four-stage differential VCO using self-biasing improves overall jitter performance of system. The circuit is designed, simulated and laid out in 0.35um mixed-signal CMOS technology. Simulation results show the PLL has high performance. In the condition of 120MHz input (840MHz output), power consumption is less than 10.5mW and root-mean-square (RMS) jitter is 4.196ps.**

***Index Terms*—Charge-Pump, PLL, LVDS, SerDes**

I. INTRODUCTION

As process technologies continue to scale down, the on-chip data rate moves faster than the off-chip data rate. The interface between chips will become a significant bottleneck in high-speed data communications. LVDS, low-voltage differential signaling, is used to deliver higher transmission speed and higher bandwidth at lower power consumption when compared to conventional technologies [1,2]. SerDes is a high-speed serial data link to serialize the parallel data and transfer it at a much faster rate and a lower cost. Fig. 1 shows one of the LVDS SerDes architectures. The serializer converts 21 bits of CMOS/TTL data into three LVDS data streams. The deserializer converts the three LVDS data streams back into 21 bits of CMOS/TTL data. A phase-locked clock is transmitted in parallel with the data streams [3]. For example, at a transmit clock frequency of 75MHz, 21bit of TTL data are transmitted at a rate of 525Mbps per LVDS channel. The total data throughput is 1.575Gbit/s. The main disadvantage in SerDes is timing jitter, the deviation of the actual signal transition from the excepted transition in time. The SerDes jitter may affect the BER, which is the ratio of the number of bit errors to the total number of bits transmitted. The BER of SerDes can be improved by reducing the jitter in the clock generated by the Phase-lock Loop (PLL) [4].

Among different PLL topologies, charge pump PLL is widely used because of the phase-lock advantage [5, 6, 7]. As shown in Fig. 2, a charge pump (CP) circuit converts the phase frequency detector (PFD) outputs, UP and DN signals, which is in response to the phase difference between the reference signal and the feedback signal, to an analog signal supplied to the loop filter, in order to adjust the frequency of the VCO output.

In this work, a 0.35um charge-pump PLL applied for a LVDS SerDes, which data throughout is 1.785Gbit/sec is given. To meet the demand of the clock of the serializer or deserializer, the rate of the VCO output is as 7 times as the rate of the input clock. The input clock frequency of the PLL is 20 to 120MHz and the output frequency of the PLL ranges from 140MHz to 840MHz. In order to reduce jitter, a new charge pump is proposed. A differential VCO structure used reduces the effects of common-mode noise, the magnitude of currents spikes injected to power supply and substrate, and ultimately the jitter generation. The design of the proposed charge-pump PLL circuit is described in section Ⅱ. In section Ⅲ, simulation results will be given. Finally, the conclusion is drawn in section Ⅳ.

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II. DESIGN OF THE PROPOSED PLL CIRCUIT

A. Charge Pump Circuit

In conventional CMOS charge pump circuits, there are some non-ideal effects such as the clock feedthrough, current mismatch and charge sharing which result in a jitter in phase-locked loop circuits. The schematic of the proposed charge pump is shown in Fig. 3, in which, the current mirrors for generating I_{UP} and I_{DN} are actually implemented using wide-swing cascode current mirrors (M5 ~ M14) due to high output resistance and better current matching.

Compared with traditional charge pump circuit, in this design, Charging path (discharging path) consists of transistors M1 and M2 (M3 and M4), and switches

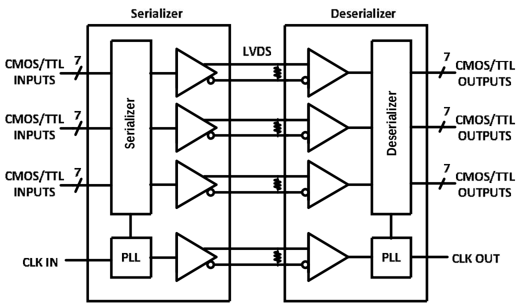

Figure 1. The architecture of LVDS SerDes

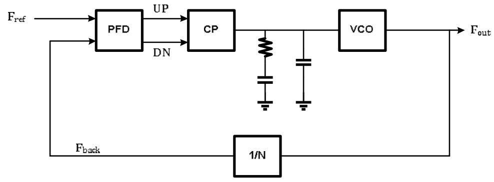

Figure 2. The block of charge-pump PLL

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(transistors M2/M3) are put far away from the output transistors M6/M7. The UP and DN signals provided by PFD are not directly connected to the switches to eliminate the mismatch through inverter and transmission gate. When UP and DN are all valid, the current I_{UP} flows into transistors M1 and M2, while very little or no current flows into output transistor M6. Meantime, the current I_{DN} flows from transistors M3 and M4, while no current flows into transistor M7. So there is no current to capacitor C_L and M6/M7 are almost turned off. When transistor M2 is off and transistor M3 is on, the current I_{UP} flows into M6 and no current flows into M7, so the capacitor C_L in the loop filter are being charged and the voltage of output node is pulled up. Similar principle applies to the discharging cycle. An amplitude contraction circuit (LS) is added as described in Fig. 3 in order to speed up the charge pump circuit. The detail circuit LS is showed in Fig. 4. The transistors Ma~Md are always on. When IN is equal to Gnd, M2 is off and M1 is on. Then the OUT node voltage depends on the radio of the resistance Mc/Ma/M1 and resistance Mb/Md. When IN is equal to Vdd, M1 is off and M2 is on. So the OUT node voltage depends on the ratio of the resistance Mc/Ma and resistance Mb/Md/M2. If we carefully choose the (W/L) ratio of Ma~Md, the swing of the input signal at the gate of switch M2~M3 can be compressed to any level as you want.

In this design, non-ideal effects can be greatly reduced. Firstly, as transistors M6/M7 and M1/M4 are connected to a fixed bias voltage, feedthrough of the input pulses can be avoided by blocking input pulses from reaching the output terminal during the transition of UP/DN signals. Secondly, the charge sharing effect is reduced in this configuration. As switches are on, the voltage at node A is pulled down to a voltage less than Vdd, while the voltage at node B is pulled up to a voltage more than Gnd. we can choose the (W/L) radio of M1~M4 to make the voltage at node A/B equal . Also transistor M6 and M7 are not completely off (in deep linear region), the output node is not floating. When the switches turn off, the current flows into M5~M8 and the level of voltage change at node A (B) is minimized, less than the difference between Vdd and Vctrl (the difference between Vctrl and Gnd). So the charge redistribution effect is suppressed. Thirdly, when the amplitude contraction circuit (LS) is used, the charge quantity of switching decreases and the circuit speed can be improved. Furthermore, the low-swing input signals can make switches work between cut-off region and saturation region to reduce the effect of charge injection [8].

B. Voltage-Controlled Oscillator

Ring oscillators are among the popular structures for VCOs due to their wide tuning range and relatively good phase noise performance. In this work a four-stage differential ring oscillator [9] is used, as shown in Fig. 5. In order to achieve the wide linear range and low jitter operation, we choose the symmetric load delay cell and a replica-feedback bias circuit to implement the VCO.

Generally, the loading in the delay cell adopting a single MOS device hardly keep linear I-V characteristic curve when the amplitude of the delay cell output swings. The non-linear resistor characteristic of the loading has poor static supply noise rejection. For this reason, we choose the symmetric load to decrease the frequency jitter because of its linear I-V characteristic curve and high static supply noise rejection. Fig. 6. shows that the delay cell circuit consists of a self-biased NMOS current source controlled by Vbp and the symmetric load controlled by Vbn, which consists of a diode-connected PMOS device in shunt with an equally sized biased PMOS device. The bias generator produces the bias voltage Vbn and Vbp from Vctrl to provide the correct swing for the symmetric load and automatically adjust the bias current that is independent of supply voltage. It consists of start-up circuit (not shown), differential amplifier and half-buffer replica as shown in Fig. 6. The amplifier adjusts Vbn so that the voltage at the output of the half-buffer replica, is equal to Vctrl, the lower voltage swing limit. Due to the output swing of the delay cell following the Vctrl to vary, we need differential-to-single end circuit to amplify the output swing and adjust the duty cycle of the delay cell.

The simulated tuning curve of the VCO (using Cadence Spectre circuit simulator) is shown in Fig. 7. As seen from the figure, for the desired tuning range (from 70MHz to 840MHz), the VCO control voltage changes from 0.8V to 2.35V.

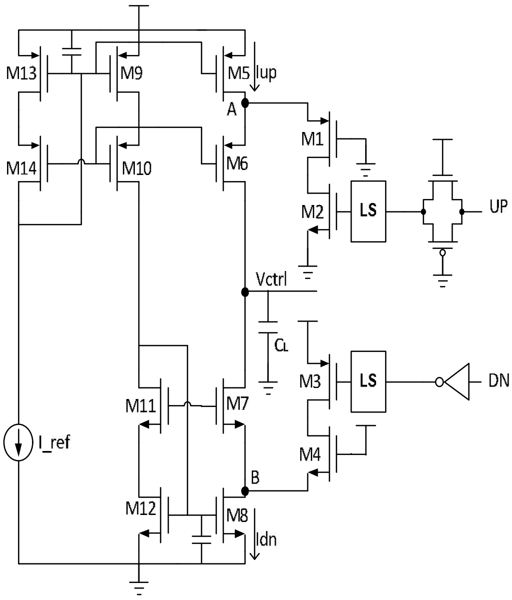

Figure 3. The schematic of proposed charge pump

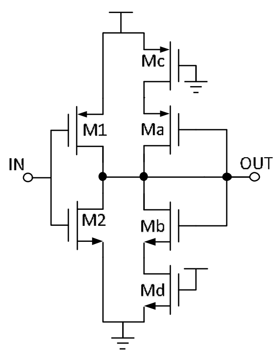

Figure 4. The schematic of the LS circuit

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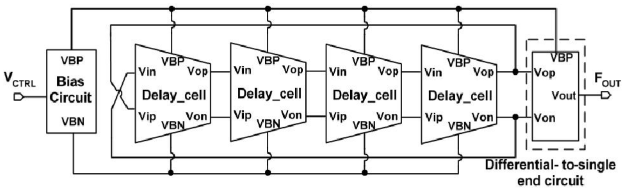

Figure 5. The full VCO circuit

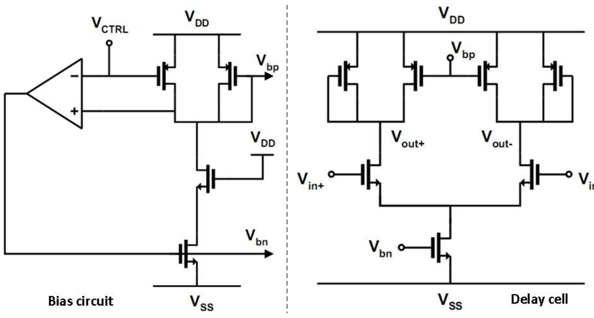

Figure 6. the schematic of Bias circuit and Delay cell

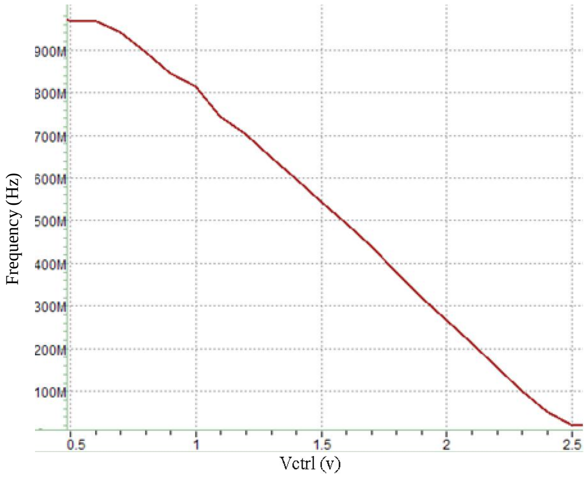

Figure 7. The Tuning curve of the VCO

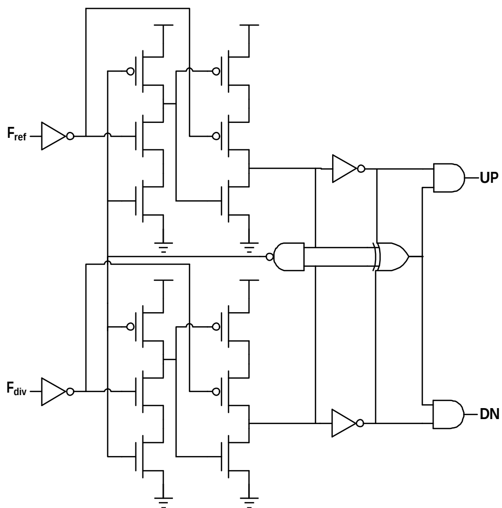

Figure 8. Circuit schematic of the PFD

C. Other Circuits

A common drawback for some PFDs is a dead zone. The dead zone generates phase jitter since the control system does not change the control voltage when the phase error is within the dead zone [10]. A dynamic phase frequency detector with less dead zone is proposed in [11,12] , as show in Fig. 8. Due to 7-times clock is needed in the serial-to-parallel or parallel-to-serial circuit, a frequency divider is used here and N=7. The schematic of the divider is shown in Fig. 9. The true single-phase-clock (TSPC) circuits [13], which can operate at high frequency, are used to build the required D filp-flops.

III. Simulation

The whole charge-pump PLL is designed and simulated in SMIC 0.35um 3.3V mix-signal CMOS technology using Cadence Spectre circuit simulator and Hspice. Furthermore, the complete PLL has laid out using Cadence Virtuoso. In this section, the post simulation results are also reported.

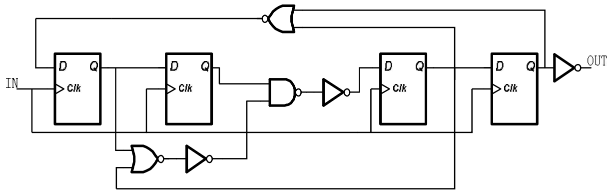

Figure 9. The schematic of divider (N=7)

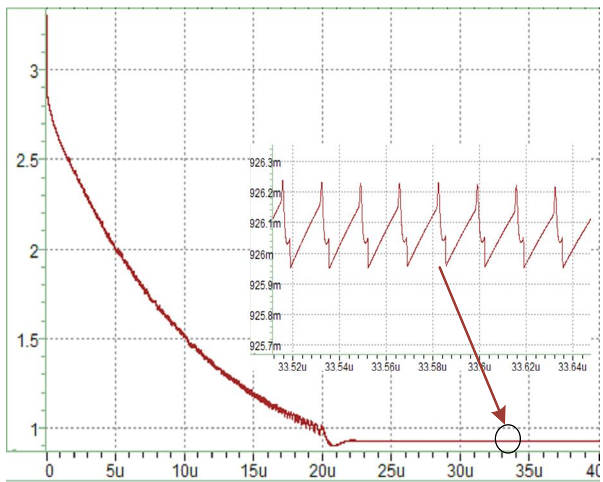

Figure. 10 The curves of control voltage (F_{input}=120MHz)

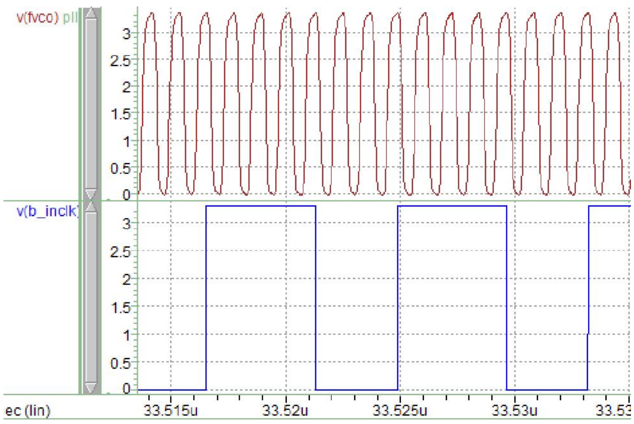

Figure.11 The waveforms of input and output (F_{input}=120MHz)

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Fig. 10. shows the transient behavior of the PLL when frequency of its input signal is 120MHz. As we can see from the Fig. 11, the output frequency is 7 times as input frequency whose duty cycle is 4:3. We sampled 12500 cycles and measured the jitter of the PLL output. The result, as given in Fig. 12, shows that the RMS jitter is 4.196ps and the Peak to Peak jitter is 23.772ps. The same simulations were done with the input clock ranged from 20MHz to 100MHz and the jitter characteristics measured is drawn in Fig. 13. The layout of the PLL shows in Fig. 14.

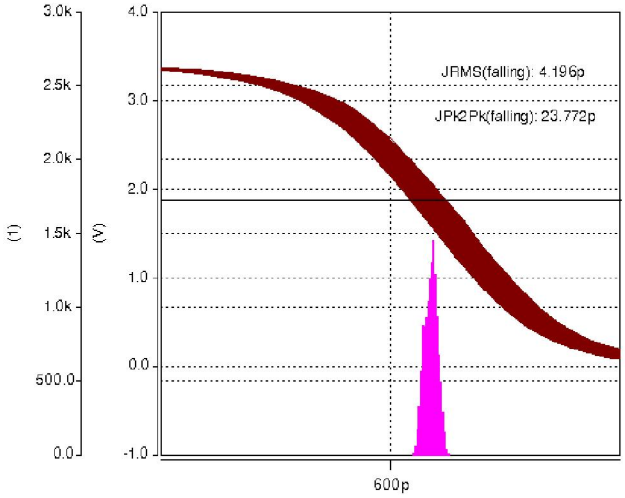

Figure 12. PLL output jitter characteristics (F_{input}=120MHz)

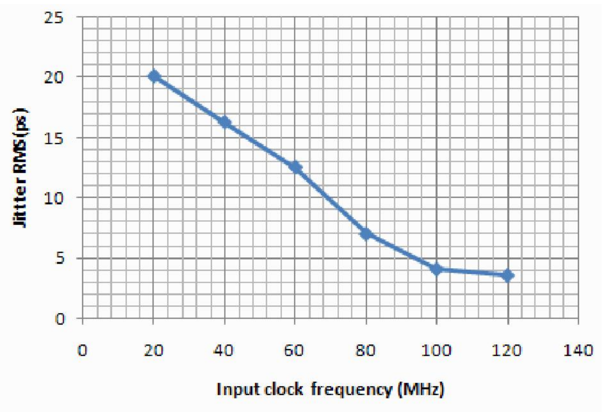

Figure 13. RMS Jitter vs. input frequency

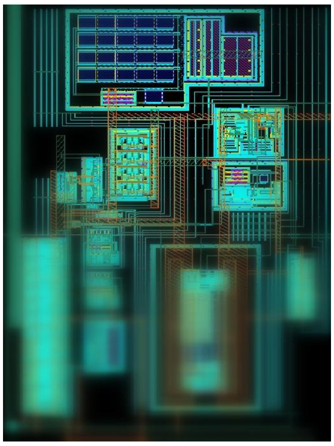

Figure 14. the layout of the PLL

IV. Conclusion

A 0.35um low-jitter charge-pump PLL applied in SerDes is realized, and it is also can be implemented in 0.18um. In design, a proposed charge pump is used to reduce non-effects which cause output phase noise. And a self-bias differential ring oscillator is used to achieve low jitter operation. The results show that the PLL has better jitter characteristics. And total power consumption @120MHz is 10.362mW.

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