A New Modeling Method for DC-DC Converter Based on Verilog-A

Boyu Hu and Lenian He

***Abstract*—A new modeling method for DC-DC converter based on Cadence platform and Verilog-A is proposed in this paper. It provides a continuous-time model for system design, in which the transistor-level power stage, the compensation network and the error amplifier could be put together in, therefore provides accurate prediction of system loop transfer function frequency response. In addition, the properly adjusted transistor-level key building blocks in the proposed continuous-time model can be directly used in the later all transistor-level system, which leads to a seamless design flow within the Cadence design platform.**

***Index Terms*—Modeling Method, DC-DC Converter, Verilog-A**

I. INTRODUCTION

The DC-DC converter, which is typically a mixed signal system, has its power stage as a nonlinear time-invariant part. The power stage regulates the output voltage and current through the modulation of the switch on time of the power MOSFETS once a period, so as lead to the sampling effect. How to represent this discrete behavior of the DC-DC converter into a continuous-time model, so as to be able to analysis the closed whole system loop and design the controller of the converter is a necessary in the system level design. This model should not only to be a linear continuous time model for design, but also includes as many real transistor-level circuits ,such as power stage, error amplifier and the related compensation network as possible to precisely represent the actual electrical characteristics of the converter. Nowadays, the theoretical deduction of the DC-DC continuous-time model is basically consummated [1]-[6], but it seems no much sense on the actual transistor-level circuits design instruction, especially for the chip design. The main problems represents as: 1) the theory deduction assumes that the system works in a proper quiescent operation point, then find out the relationship between the small signal parameters. However, to properly represent this predetermined quiescent operation point together with the ac small signal information based on it in one circuit topology requires as many transistor level circuits remaining in the continuous-time model for actual design as possible, which is still a problem; 2) the traditional system design and the bottom transistor-level design are based on different tool platform, therefore lead to the discontinuity in the design flow. How to include the system level design and the bottom circuit design in one union platform still remains as a problem.

The traditional modeling of DC-DC converters by previous papers are mainly based on three method and tools: 1) to use state-space-averaging and get the analytical mathematical expressions [7]. 2) to use Matlab / Simulink to construct the system as transfer function blocks [8]. 3) to use Pspice to construct the model [5]-[6].The problems of each of these methods are as follows: In method 1, the analytic expressions are unreachable or too complex to get a direct physical insight for system design when dealing with complex circuit topologies. In method 2, the problems are: firstly, the transfer functions only cares about the ac small signal characteristics, so that we can get no information about the actual large signal electrical characteristics about the blocks, (for instance, the feedback voltage, the output voltage of the error amplifier, etc. which is important in block specification define). Secondly, the transfer function blocks and its realization transistor level circuits sometimes cannot match, (for instance, the zeroes and poles in the compensation network) which leads to a redesign for the system in the later part of the design process. Method 3 is a promising method for the later circuits design. However, models in [5]-[6] give out no information about the out voltage loop of the system and how to present the proper quiescent operation point in the model, so it needs further improvement

This paper proposes a new modeling and simulation method for DC-DC converters in Cadence Spectre platform using boost converter peak current mode (PCM) as an example. This method provides a continuous-time model in which the transistor-level power stage, the compensation network, and the error amplifier can be all put in. These key blocks can be carefully designed and adjusted in the proposed model and directly used in the later all transistor-level system design so as to form a seamless design flow within the Cadence design platform.

II. CONTINUOUS-TIME MODEL USING VERILOG-A

Combining the advantages of different peak current mode models proposed in [1]-[6], we can realize a continuous-time boost PCM model in Cadence Spectre platform as shown in

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Fig.1.The compensation network, including the error amplifier and the power stage but excepting for the power MOSFETS, are realized as transistor-level circuit blocks, while the linearization part and signal adding part are written in Verilog-A. The expression of small signal duty ratio in [4]-[6] is:

$$\hat{d}=H_e F_m(\hat{i}_c-\hat{i}_L-F_g\hat{v}_g-F_v\hat{v}) \tag{1}$$

In(1) , F_m models the PWM modulator gain, $\hat{i}_c$, $\hat{i}_L$, $\hat{v}_g$, $\hat{v}$ are the small signal expressions of control current, inductor current, input voltage and output voltage. F_v and F_g model the effect which input voltage and output voltage have on small signal duty ratio [4]. H_e models the high frequency sampling effect [6]:

$$H_e=1/(1+\frac{s}{\omega_p}) \quad \omega_p=\frac{2\pi f_s}{4}\pi(\frac{2}{1+\alpha}-1) \tag{2}$$

however, (1) should be changed to a more proper voltage domain form as:

$$\hat{d}=H_e\frac{scale}{R_i}F_m(\hat{v}_c-\frac{\hat{i}_L R_i}{scale}-\frac{R_i}{scale}F_g\hat{v}_g-\frac{R_i}{scale}F_v\hat{v}) \tag{3}$$

for the reason that the actual control signal given by the outer voltage loop is $\hat{v}_c$ instead of $\hat{i}_c$. R_i is the I-V conversion ratio, *scale* is the ratio between the boost inductor current i_L and the sensed current i_{sense} used for control loop as:

$$i_{sense}=i_L/scale \tag{4}$$

$\frac{scale}{R_i}F_m$, $\frac{R_i}{scale}F_g$, $\frac{R_i}{scale}F_v$ and H_e in (3) are all implemented in the proposed model as their Laplace transfer function blocks; R_E in series with inductor in Fig.1 models the total effect of power MOSFETS' conduction resistors and inductor series resistor for consideration of inductor current ripple, which can be expressed as:

$$R_E=[DR_{NMOS}+(1-D)R_{PMOS}+R_{inductor}](1+\frac{\Delta i^2_L}{3I^2_L}) \tag{5}$$

$$\Delta i_L=\frac{V_g-V}{2L}DT_s \tag{6}$$

where R_{NMOS} and R_{PMOS} are the real testing value of power MOSFETS conduction resistors at converter switching frequency; D is the Duty ratio of the PWM modulator

Each of the four adders in Fig.1 is realized as a three input one output VCVS, giving out the sum of all input voltages as output voltage; the inductor current sensor is implemented as a CCCS together with a series resistor in the detected branch.

The packaged power stage linearization part models duty ratio controlled power MOSFETS' effect on the power stage, the detail of which is shown in Fig. 2. This block is composed of two parts. One is the small signal $\hat{d}(t)$ controlled VCVS $V\hat{d}(t)$ and VCCS $I_L\hat{d}(t)$, V and I_L are the output voltage's and inductor current's dc value at the predetermined quiescent operational point. The other part is the quiescent operational point D controlled transformer. Depicting all these relations in Verilog-A, we can get a two port network with an additional control port $\hat{d}(t)$ as shown in Fig.2.

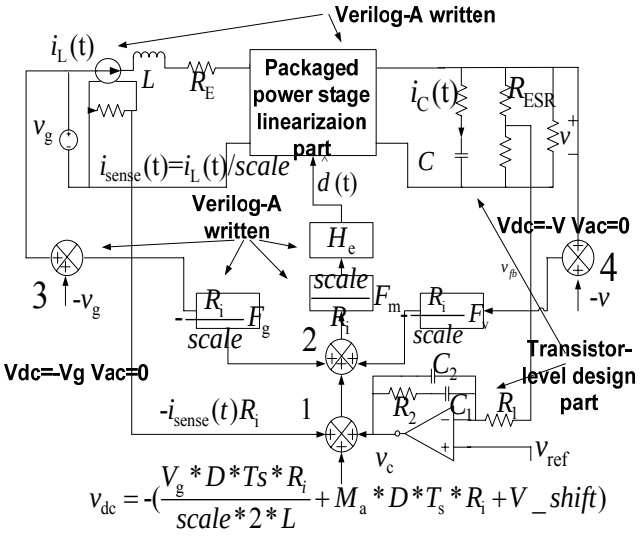

Fig. 1. Continuous-time model based on Verilog-A

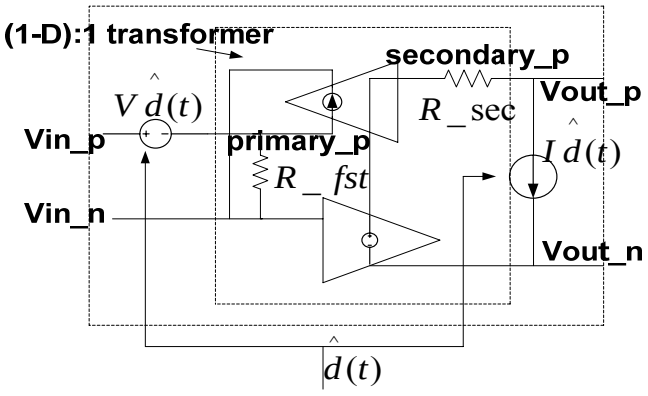

Fig. 2. Insight of packaged power stage linearization part

For proper usage of the proposed model, all the parameters needed for building the Verilog-A written blocks, such as V_g, V, C, L, f_{switch}, R_L, M_a, should be set to meet the specific design requirements. Duty ration D is remained as a DC sweep variable in Spectre to find out the predetermined quiescent operational point.

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The basic idea of the proposed model is that in a predetermine system working condition, for instance V_g=1.8V, V=3.3V, I_{out}=150mA, setting the model parameters as mentioned above to proper values, then using DC sweep fuction in Spectre to sweep the variable D from 0 to 1. When a variable D value making $\hat{d}(t)=0$ is found, it is the proper duty ratio for this predetermined system working condition, making the whole system is at the quiescent operational point. The detailed usage steps of the model are discussed as follows.

As been shown in Fig 3, when the system works at a certain quiescent operational point, the control voltage v_c generated by the error amplifier, the sensed inductor current and the compensation current has a relationship as:

$$v_c = i_L \frac{R_i}{scale} + \frac{v_g DT_s R_i}{scale 2L} + M_a \frac{R_i}{scale} DT_s + V\_shift \tag{7}$$

where M_a is the slope of the compensation current, V_{shift} is the level shift of the compensation current converted voltage at the beginning of every switching period.

In dc condition, as been shown in Fig.1, injecting a dc bias voltage to the No.1 adder as:

$$v_{o1} = v_c - i_L \frac{R_i}{scale} - \frac{v_{in} DT_s R_i}{scale 2L} - M_a \frac{R_i}{scale} DT_s - V\_shift \tag{8}$$

Injecting the No.3 and No.4 adder with dc voltage $-Vg$, and $-V$ separately, the dc output of $-F_v$ and $-F_g$ blocks become zero. So we can get that $\hat{d}(t)=v_{o1}$ in dc condition.

As shown in Fig.4, firstly do DC sweep to the sweep variable D in Spectre from 0 to 1, when a certain D value makes that $\hat{d}(t)=v_{o1}=0$, it means at this time the small signal $\hat{d}(t)$ has no influence on the power stage and the whole input/output relation is regulated by the large signal D. Output of the error amplifier v_c also suits the proper relationship with sensed inductor and compensation current in predetermined working condition. All these prove that the system has been in the predetermined quiescent operational point through the closed feedback.

One question comes out which is how to present the small signal duty ratio (2) in this model, since the dc and ac signals share the same signal path as seen in Fig 1. Actually, in ac analysis, all the dc bias voltages injected into the adders on the signal path to build the quiescent operational point equal zero, which means the (2) for small signal duty ratio still holds perfectly in this model.

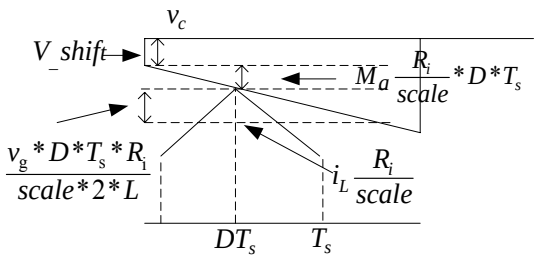

Fig. 3. The relationship between control voltage, inductor current and compensation current in steady state

With the proper set quiescent operational point, we can inject ac signals into various parts of the system and get the frequency response of the system loop. Moreover , as the voltage and current of the transistor-level power stage and compensation network has been set just the same as real working status, these carefully design blocks within this continuous-time model can be used directly in the all transistor-level system design later using Cadence Spectre.

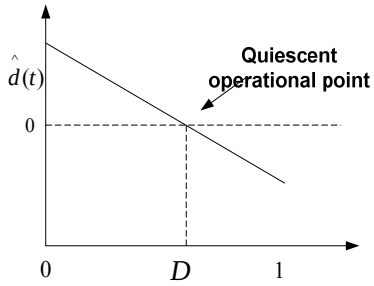

Fig. 4. Getting quiescent operational point through dc sweep

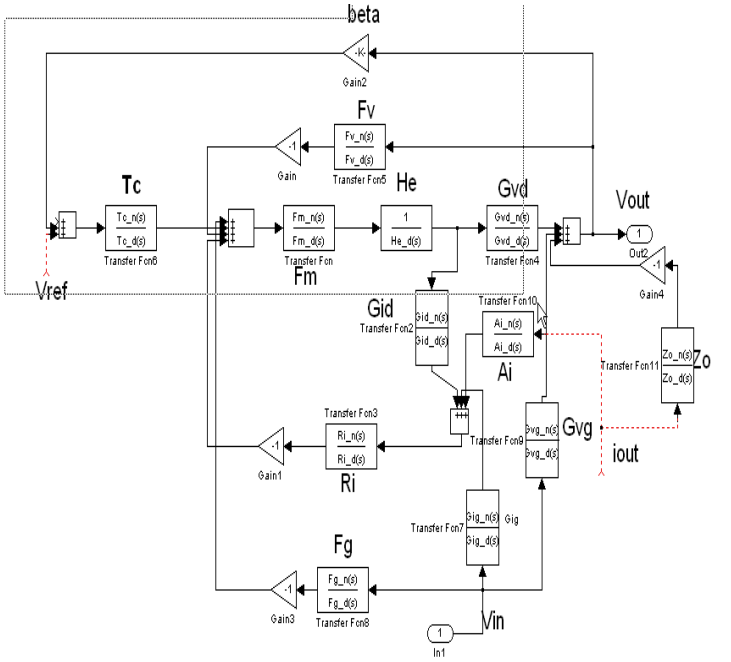

Fig. 5. Matlab/Simulink model for comparision

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III. SIMULATION RESULTS AND DISCUSSION

For compare purpose, one additional model is constructed using Matlab/Simulink in the form of all transfer function blocks as shown in Fig.5. The power stage in Simulink model is represented as transfer functions G_{vd}, G_{vg}, G_{id}, G_{ig} to model the effects of input voltage v_g and small signal duty ratio $\hat{d}(t)$ have on the inductor current i_L and output voltage *v*. A_i *and* Z_o are used to model the effect output current i_o has on i_L and *v*. All these power stage transfer functions used in the simulink model are carefully deduced in [1]-[3]. The type II compensation network:

$$T_c(s) = \frac{\omega_{c1}}{s}\frac{1+s/\omega_{cz1}}{1+s/\omega_{cp1}} \tag{9}$$

where $\omega_{c1}=1/((R_1(C_1+C_2)))$, $\omega_{cz1}=1/(R_2C_2)$, $\omega_{cp1}=(C_1+C_2)/(R_2C_1C_2)$ is just the same as that used in [8] and in Fig.1. All the other blocks and all system related parameters are set the same as the Verilog-A model.

As partly shown in Fig.6, the simulation results of frequency response of G_{vd}, G_{vg}, G_{id}, G_{ig}, A_i, Z_o , the closed current loop transfer function:

$$T_{icl}(s) = \frac{d(s)}{v_c(s)}\Big|_{v_g=i_o=0} \tag{10}$$

and the control voltage to output transfer function:

$$T_a(s) = \frac{v(s)}{v_c(s)}\Big|_{v_g=i_o=0} \tag{11}$$

are exactly the same with the two models ,which proves the functional correctness of the proposed Verilog-A model. However, since the type II *Tc* part in Verilog-A model is a transistor-level cascaded OTA together with real resistors and capacitors, whhile in Simulink model it is just an ideal transfer function (9) considering no effect of the finite gain and the movable inner zero-poles of the error amplifier due to the different outer RC network as load impedance. With the same type II parameters in (9), the frequency response magnitude and phase of *Tc* in these two models present different behavior as shown in Fig.7, especially in low frequency range. This omit of non-ideal factors of *Tc* affects the simulink model's accuracy in predicting the loop transfer function frequency response where *Tc* is included, such as the closed-loop audio-susceptibility transfer function G_{vg_closed} and the closed-loop output impedance Z_{o_closed} , which are the key specifications of a DC-DC converter., the compared simulation result of which are shown in Fig.8,

As been discussed in this section, the proposed Verilog-A model provides not only a seamless design platform within Cadence Spectre, but also a more accurate closed-loop frequency response prediction due to its inclusion of the transistor-level power stage and compensation network, which leads itself a more proper choice for all-transistor level chip design usage.

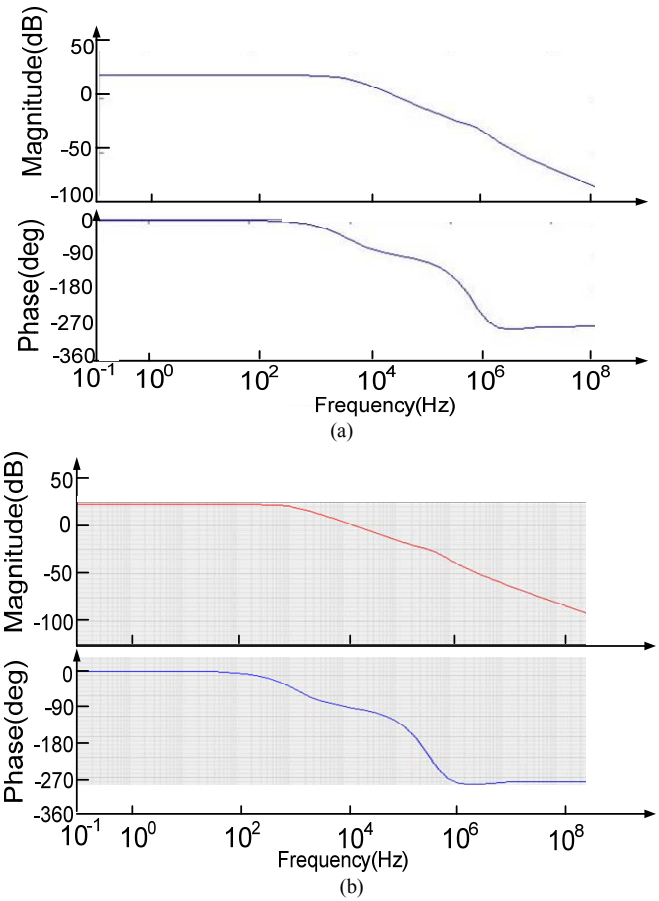
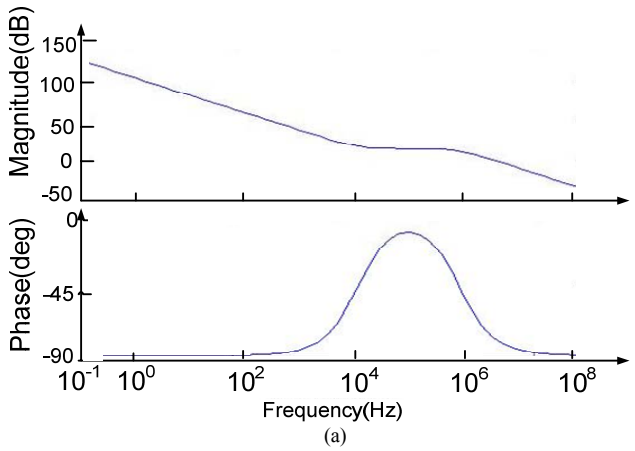


Fig. 6. Simulated frequency response of T_a in (a) Simulink model and (b)Verilog-A model



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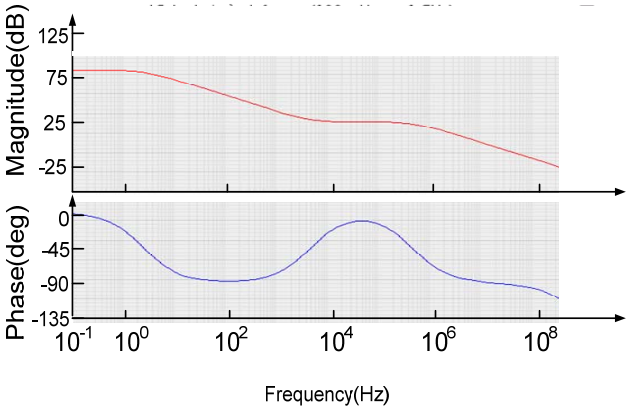
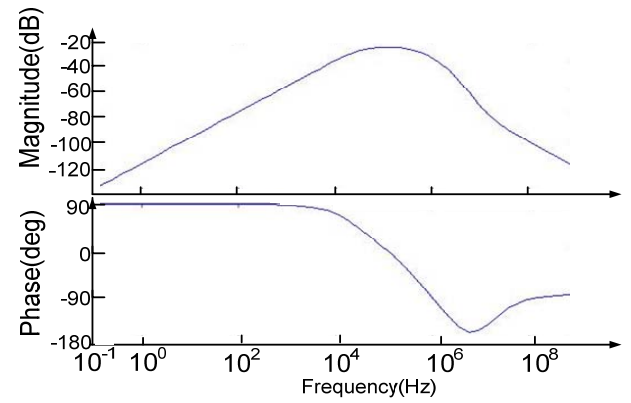
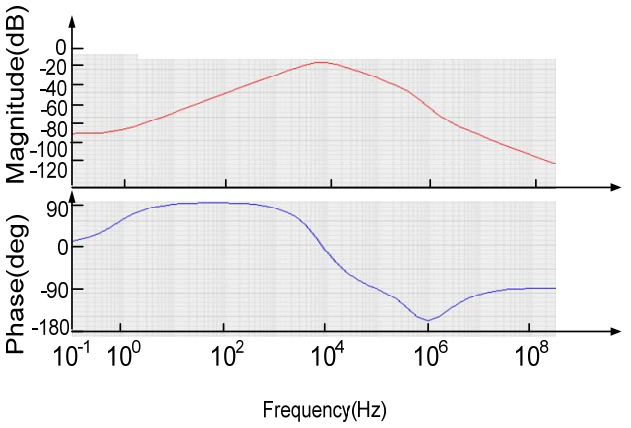


(b)

Fig. 7. Simulated frequency response of T_c in (a) Simulink model and (b)Verilog-A model



(a)



(b)

Fig. 8. Simulated frequency response of audio-susceptibility G_{vg_closed} in (a)Simulink model and (b) Verilog-A model

IV. CONCLUSIONS

This paper proposes a new continuous-time model for DC-DC converter based on Cadence platform and Verilog-A. This new model reserves the transistor-level power stage and compensation network within it, therefore provides a more accurate prediction of system loop transfer function. In addition, the properly designed key building blocks using the continuous-time model could be directly used in the later all transistor-level system. As this model and the transistor-level circuits design are based on the same Cadence platform, it also provides a seamless top-down design flow.

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