On-Chip Soft-start Cell for DC-DC Converter

Lu Jing, Wu Xiaobo, Shen Xuzhen, Qin Lin

***Abstract*—A novel COMS compatible digital soft-start cell for DC-DC converters is proposed in this paper. Besides suppressing the initial overshoot voltage and the inrush current, this cell also succeeds in smoothly converting the period of start-up to normal operation. Moreover, the proposed on-chip scheme cuts down a required I/O pin for traditional soft-start, which means a higher integration for DC-DC controllers and an economic real estate for PCBs. In this paper, a 2ms proposed soft-start is implemented in a Buck system with input voltage of 12V, output voltage of 5V, output capacitor of 47uF and load current of 1A. Cadence SpectreS simulation results show that both the soft-start part and the digital control part function well accord with the design purports. Owing to the excellent property of digital circuits, this soft-start cell is widely available to DC-DC converter.**

***Index Terms*—DC-DC converter, soft-start, on-chip.**

I. Introduction

Recently, the growing market of portable electronic devices brings greater demands for power management integrated circuit (PMIC). Among different PMIC, DC-DC converter is important in regulating the power supply, due to its high efficiency, capacity of outputting current and small static current [1]. However, an inrush current and overshoot voltage appears in the startup period of the DC-DC converter, which may causes damage to the whole system and the load. Thus, a so called soft-start function is adopted during the startup stage of the DC-DC converter, which smoothly conducts the output voltage and current in the inductor to the steady state.

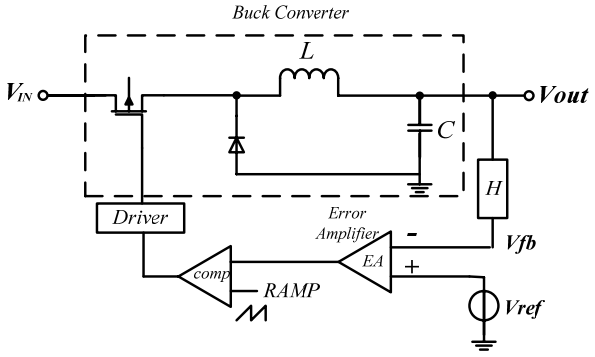

Fig. 1 Buck system.

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In a typical DC-DC converter, as in Fig.1 a Buck system, a negative feedback is applied to build a system that automatically adjusts the duty cycle to obtain a given output voltage maintaining steady under all conditions [2]. Usually the output voltage is measured with a factor of H. The sensed output signal V_{fb} is compared with a reference voltage V_{ref}. The negative feedback loop makes the sensed voltage accurately follows V_{ref}, so that a constant V_{out} achieved. Accordingly, V_{ref} can be replaced by a ramp signal during soft-start, holding the output voltage to climb bit by bit. As the duty cycle is limited, an inrush current can also be suppressed.

The conventional soft-start circuit is shown in Fig.2. During soft-start stage, a ramp voltage V_{SS} is generated from a capacitor charged by a current bias. The smaller one VSS is added to the feedback loop, compared with V_{ref} by a comparator, until it reaches V_{ref}. The drawback of this method is that the soft-start capacitor CSS is usually too large to be integrated on chip, which means additional pin and PCB area. Furthermore, voltage spike may still occur at the end of the soft-start, because two control signals V_{ref} and V_{SS} are put through at the same time by comparator, and compared to feedback voltage V_{fb} [3].

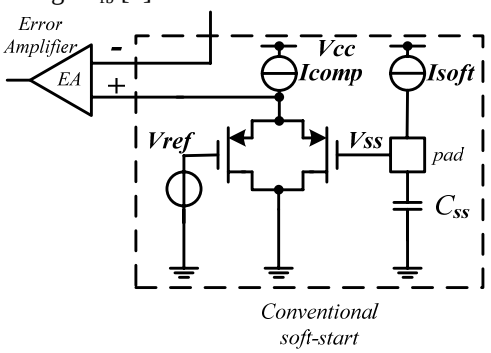

Fig.2 Conventional soft-start.

The proposed soft-start technique can overcome all the disadvantages of the conventional soft-start mentioned before, and accomplish the soft-start job perfectly. Besides, a whole power up sequence and control strategy is presented in this paper, which will be elaborated in the following parts. The proposed structure is employed in Buck system with input voltage of 12V, output voltage of 5V, output capacitor of 47uF and load current of 1A. The system operates at a frequency of 500k Hz and a 2ms soft-start is designed. The function is validated by simulation under BCD150 process in Cadence SpectrS.

The paper is organized as follows. First, the overall design of the proposed novel soft-start structure is presented in section II. Next, based on the novel functions of proposed soft-start, circuits' implementations are described in section III. Simulation results are exhibited in section V. Finally, the conclusion section IV.

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II. Implementations of Proposed Softstart

First, a whole power up process is shown in Fig.3. After the system is enabled by signal *ENA*, a simple bias is initiated. The LDO (Low dropout regulator) works by this rough bias. When the LDO is stable, it outputs power supply to a precision bandgap. *BG_ready* signal will go high when the precision bandgap stably works. The bias of LDO will change from a simple one to a precision one, leading to a more precision LDO output. When the power up process is over, an *LDO_ready* signal is sent all over the chip, and the rest of the chip will work then. This whole process will guarantee a safe power environment to sensitive analog modules. This *LDO_ready* signal will also tells the state control module to change the stage form *SD* (shut down) mode to *SS* (soft start) mode. When the soft-start is accomplished, an *SS_ok* signal will switch the stage to *NM* (Nmoral operation) mode. Furthermore, the entire protection signal can be incorporated in the state module to boot different operation stage.

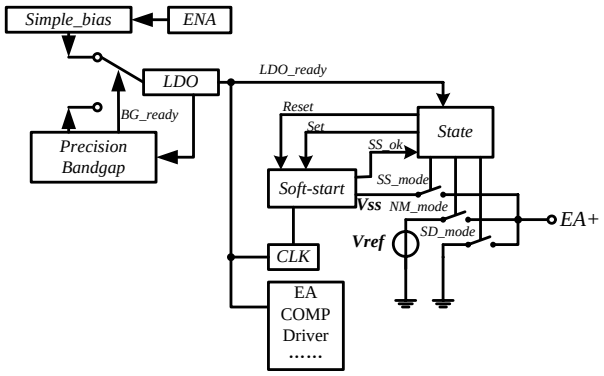

Fig. 3 Illustration of power up procedure.

The diagram of the proposed soft-start is shown in Fig.4. The CLK signal is a clock signal provided by the oscillator included in the switching regulator. A prolonged clock signal is generated by 6-bit frequency divider, named as D_CLK, defining the interval between each step. The frequency divider is built by N in series D-Flip-Flops (DFFS). To achieve a 2ms, 16-step soft-start procedure, D_CLK is devised to have a period of 128us. Expression is given as (1). D-CLK triggers the 4-bit Gray Code generator. Gary Code generator sends 4-bit Gary Code to DAC, and DAC translates the codes to a raising signal *V*ss.

$$t = 2^{N} \times T_{CLK} \quad (1)$$

The time chart is shown in Fig.5. When the *SS* mode is selected, V_{SS} goes into point ①. The number of soft-start steps N_{step} is design flexibility, and a 16-step example is illustrated in this paper. More steps can be developed by designers to obtain better performance of soft-start without taking too much area. After point ①, the voltage V_{SS} rises step by step under the designed frame. At point ②, the 16 counter is completed. When another D_CLK pulse comes, the Gray code generator overflows, and the *SS_ok* bit is set to be logic 1. At this point the switch turns to normal operation, and V_{ref} is selected. Apparently, the traditional comparator is eliminated, and no co-existed voltage appears. The transition is much smoother.

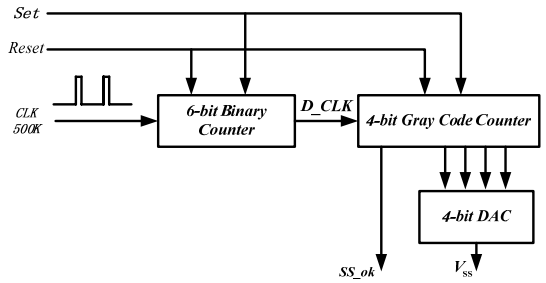

Fig. 4 Diagram of proposed soft-start.

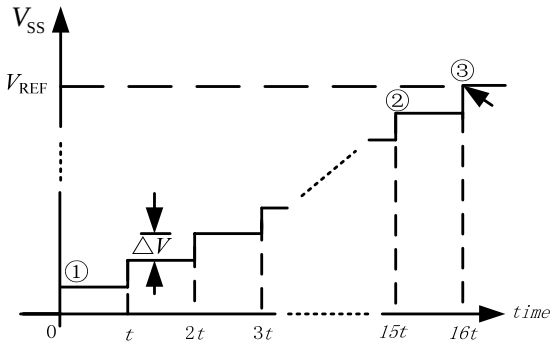

Fig. 5 Time chart of proposed soft-start.

III. Circuit Implementation

Based on the structure of proposed soft-start, a Gray Code generator and DAC are needed. The 4-bit Gray Code counter and 4-bit DAC is presented in this section. The steps length and size can both be modified as designer's request. The only thing to do is to add or less the numbers of DFFs.

A. Gray Code Cenerator

Gray Code is excellent in its way of reducing overturn of the switches, and save power consumption. So Gray Code is chosen to control the 4-bit DAC. Fig.6. illustrated one way to generate the codes. *SS_ok* signal is used to sign the end of soft-start. Once the generator overflows, and *SS_ok* goes to logic 1. V_{ref} is chosen to regulate the output voltage, and the system goes into normal operation.

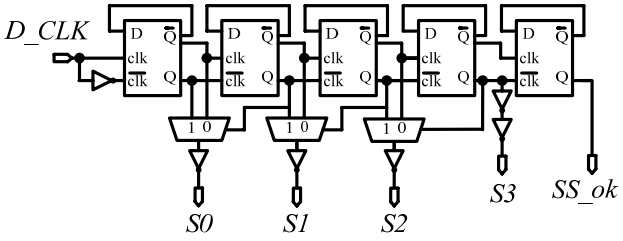

Fig. 6 Schematic of Gray Code generator.

B. 4-bit DAC

The principle of the 4-bit DAC is shown in fig.7. The number of steps is determined by the bits of the Gray Code. There are two branches of resistors, X branch and Y branch. The Y branch is paralleled attached to the X branch. Code (S3, S2) alternate changes the connection node of Y branch to X branch. In other words, Y branch is connected to R1, R2, R3 and R3 respectively. Code (S0, S1) controls SS output node sequentially to lower potential to higher one. The overall resistance remains the same as (2). An additional bias current is added to supply current running in the DAC arrays, so as to reduce the load current from V_{ref}.

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$$R_O = 3R_X + (R_X \| 5R_Y) \quad (2)$$

$$I_{supply} = V_{REF} / R_O \quad (3)$$

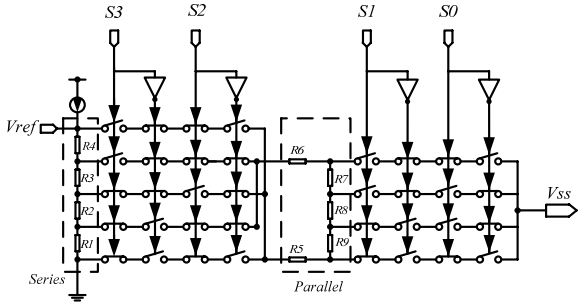

Fig. 7 Schematic of DAC.

IV. Simulation Result

This soft-start is verified in a 12V input, 5V output, and 1A load Buck system, with 68uH inductor and 47uF capacitor. The simulation results are shown in fig.8. It is simulated by Cadence SpectrS under BCD 1.5um process. The waveform indicates a 2ms softs-tart and then the *SS* signal stays at V_{ref}, about 1.2V, for normal operation. The control signals correctly control the soft-start transfer to normal state without a comparator, so the transition is much soother. The total steps and the time of the soft-start can be modified as the state-of-art based on the principle detailed in this paper.

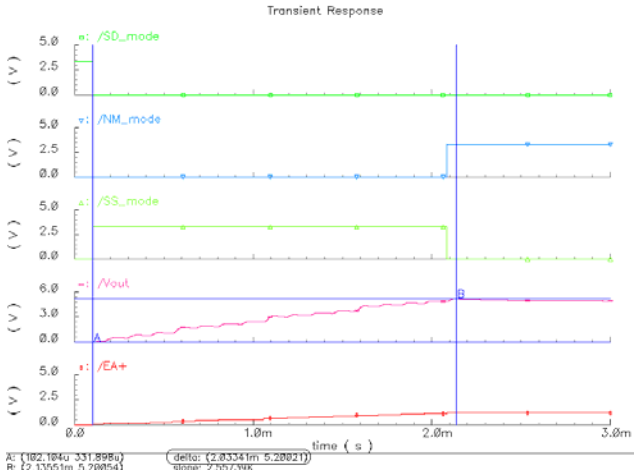

Fig. 8 Simulation results of proposed softstart circuit.

V. Conclusion

This paper presents an on-chip soft-start circuit with novel control structure. This circuit not only excels in output voltage limiting and inrush current diminishing, but also a fully on- chip scheme, which reduces a SS I/O pin and saves PCB space. This compact soft-start technique is also readily compliable to standard COMS process, making it attractive solution to portable devices nowadays.

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