Study and Analysis of the Behavior of a Generic Mesh Architecture of NoC routers

Prabhat K. Sharma, Rakesh Bairathi

***Abstract*—To architect the communication solutions for System on Chip designs at higher level of abstraction, On-Chip communication network of highly efficient routers is desired. This paper describes the behavior of the mesh of a Generic NoC router. The router and then its mesh of 4X4 have been implemented in VHDL. Deterministic Routing and wormhole switching is used. Maximum Flit size is taken i.e. equal to a packet size. The concept of virtual channels is utilized to facilitate the maximum bandwidth utilization of physical channels between two routers. The performance of 4X4 mesh has been evaluated in terms of packet delivery between two IPs and in terms of hardware usage with respect to virtual channels. An analysis of variable packet size and delay has also been done.**

***Index Terms*—Deterministic Routing, Flit, IP Network on Chip, System on chip, Wormhole switching.**

I. Introduction

The shrinking of process technology in Deep Sub Micron region has made it very possible to place an enormous amount of components on a single chip. So, now a days it is not a matter of concern to have much more processing or computing units on a single chip, what exactly is the researchers' new object under scan is the aspect of communication between these processing units. Architecting interconnects (i.e. means of communication) at a higher level of abstraction is a key factor for SoC design [1]. A single wormhole switch (Fig. 1) of mesh topology of a Network on Chip (Fig. 2) is implemented in VHDL. In our implementation, we have taken four input and four output physical channels for the neighboring nodes and one output and input channel for the IP connected to the switch. Switch provides the greater bandwidth utilization because of virtual channels [2]. The bandwidth of each physical channel is divided into four virtual channels. Now, suppose two or more virtual channels want to put their data on the any physical channel, an arbitration policy should be there to resolve the issue of access conflict. In case any conflict occurs due to two or more simultaneous requests for the channel there must be an arbitration scheme to resolve the conflict. These arbitration schemes can be given as:

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- *Fixed Priority*: In this type of arbitration scheme a level of priorities for each contestant is assigned. A contestant, with higher priority will access the channel every time.
- *Rotating Priority*: After serving the request, priority is changed to lowest.
- *Round Robin:* Each contestant has its own turn to transmit the data. And this turn obeys the circular sequence.
- *Random arbitration:* In random arbitration, grant is provided to a contestant in a random fashion.

To resolve the conflict for access, we used fixed priority arbiter which means whenever two or more virtual channels want to put their data on a physical channel, the access will be given to the virtual channel with higher priority.

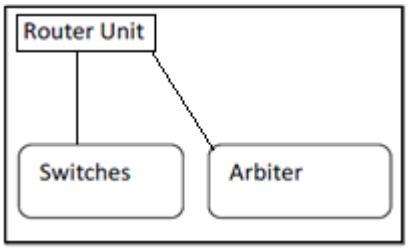

Fig. 1 Basic Routing Block

II. Performance in terms of hardware usage

After modeling the router unit in VHDL, using ISE9.1i design is synthesized and implemented. We used Virtex5 device, Selected Device: 5vlx30ff676-3, at speed grade of (-3). TABLE I provides the hardware occupancy of the router unit in terms of virtual channels. As the number of VCs cause the inefficient utilization of the area of chip, so it is required to have an optimum tradeoff between number of VCs and their performance. We can see that the difference between number of latches in four VC to three VC, Three VC to Two VC, and Two VC to One VC is gradually decreasing. It is clear as the number of VCs increases the requirement of additional latches (in comparison with the previous count) is also growing up. This fact ties up an upper bound while selecting number of Virtual Channels. In future, emphasis can be put on to find a generalized trade off analysis between the area and the performance while increasing number of flip flops.

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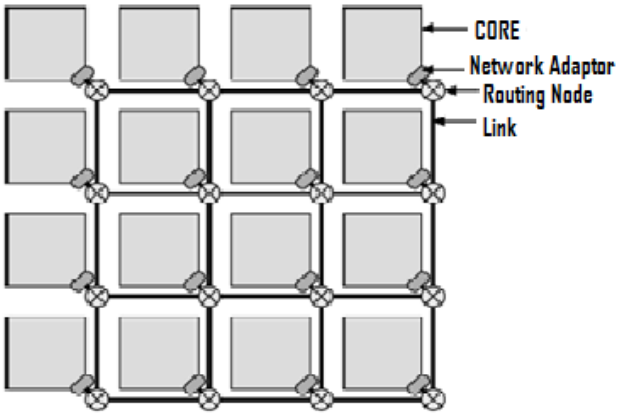

Fig. 2 Topological illustration of a 4-by-4 mesh structured NoC

III. Performance in Terms of Packet Delivery

We designed 2x2, 4x4 units from the basic router unit. Packet delivery in a 4x4 mesh is very complex and completely random behavior. As the packet delivery is controlled by the addressing and routing information within the packet, the selected path has to play a major role. Packet may be dropped because of following reasons (i) wrong address information, or (ii) not any virtual or physical channel is found free, or it may be because of (iii) no permission is granted from arbiter to access the PC.

TABLE I
HARDWARE USAGE IN TERMS OF VIRTUAL CHANNELS

No. of Virtual Channels	No. of Latches	No. of Slice Registers	No. of Slice LUTs	No. of unused Flip-Flops
Four	137	835	1359	544
Three	111	792	1319	529
Two	85	783	1285	502
One	70	780	1268	491

The 4x4 and 2x2 meshes have been tested for various and of course random cases. It was found that the behavior of 4x4 is much unpredictable and random (as shown graphically in Fig. 3) than the behavior of 2x2 mesh. This is but natural conclusion as number of possible paths is very much larger in the previous case. Table II shows the number of packet lost against the number of source IPs. This particular case is very much random and can be used to show the non-deterministic behavior of packet delivery.

IV. Variable Packet Size and Delay Analysis

The overall logic was redesigned for variable packet size. It was assumed that the packet will supposed to be ended when a predefined sequence of bits is encountered within the packet body. The delay increases (almost linearly) as the packet size increases.

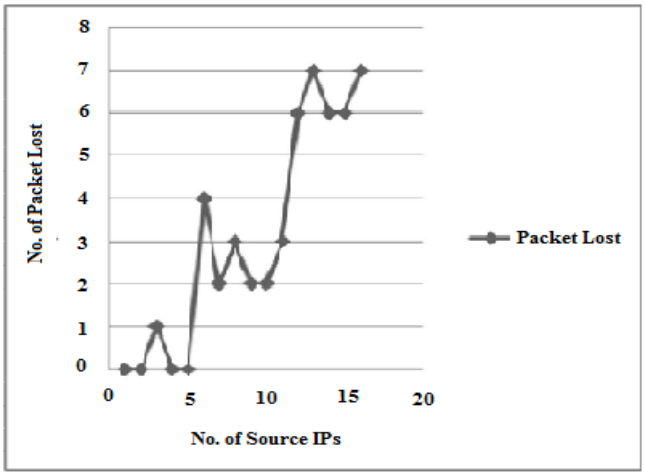

Fig. 3 Random behavior of 4x4 mesh

The variable packet size incorporates the concept of flits in itself. Table 2 shows the linear variation in the delay with packet size.

TABLE II
RANDOM BEHAVIOR OF 4X4 MESH

No. Of source IPs	Packet Lost	No. Of source IPs	Packet Lost
16	07	08	02
15	06	07	04
14	06	06	02
13	07	05	00
12	06	04	00
11	03	03	01
10	02	02	00
09	03	01	00

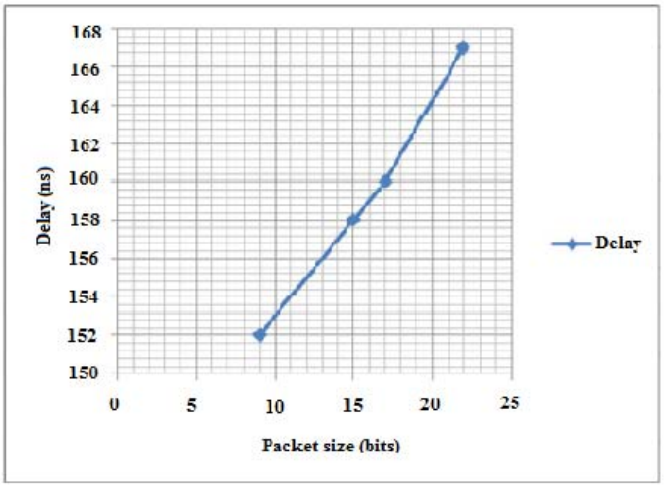

Fig. 4 Packet size VS delay

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V. System specification

The complete implementation work was carried out on the system with following specifications:

Operating System:

Microsoft Windows XP Professional
Version 2000, Service Pack 2

Computer:

Intel® Core™2 Duo CPU
E4500 @ 2.20 GHz
2.19 GHz, 1 GB of RAM

VI. Conclusion

The Packet delivery from source to destination is completely a random process and this randomness is, but naturally, the function of traffic conditions on the channels. While dealing with the switches with virtual channels, the non-availability of virtual channels is also a limiting factor (though channel utilization is increased using concept of virtual channels). The delay increases (almost linearly) as the packet size increases. In future, emphasis can be put on to find a generalized trade off analysis between the area and the performance while increasing the number of virtual channels. Increase in the numbers of virtual channels provides the better utilization of the net bandwidth; on the other hand it will increase the cost while considering the chip area a cost factor.

This work can be extended for a general flit concept. Performance can be compared for various arbitration schemes. A comparative analysis of variable packet size and fixed packet size along with the generalized latency and throughput can be a point of emphasis in future.

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