Hybrid DPWM with Analog Delay Locked Loop

Xuzhen Shen, Xiaobo Wu, and Jing Lu, Lin Qin

***Abstract*—This paper presents an 11-bit hybrid digital pulse width modulator (DPWM). The DPWM includes a 5-bit counter and two 3-bit delay lines. Analog DLLs are used to lock the delay to required time, providing wide operating frequency range. The module also provide sampling trigger to start voltage/current sampling. The hybrid DPWM operates at 500KHz switching frequency. Simulation results validate the function of the proposed DPWM.**

***Index Terms*—Digital pulse width modulator (DPWM), delay line, analog delay locked loop (ADLL).**

I. Introduction

Digital pulse width modulator (DPWM) is an important part of digital switching power controller. It converts the digital duty ratio into PWM wave. High resolution DPWM is required to avoid limit-cycle oscillation in digital SMPS. Many architectures are proposed since 1997[1], such as delay line, sigma-delta and hysteretic modules, etc. Sigma-delta type can achieve high resolution without high bits of DPWM, but suffers from the problem of poor transient response [2]. Hysteretic module is easy to implement and can reach high resolution, however its switching frequency is not constant [3]. Delay line types are popular for its simplicity. Hybrid DPWM can achieve high resolution without taking very large die size. Delay locked loops (DLL) are necessary to synchronize different levels of delay line. Digital DLL are fully synthesizable, however suffers from the problem of discrete delay time and size cost, because each delay cell is composed of integer number of logic units [4]. Analog DLL can adjust the delay time continuously, and the delay cells can be kept small.

This paper presents an 11-bit ([10:0]) hybrid DPWM [4]. The module is composed of a 5-bit counter [5] and two 3-bit delay lines [6]. The 5-bit counter generates high bits of output ([10:6]), the 3-bit delay lines generate the middle ([5:3]) and low bits ([2:0]). The solution takes the least die size. Analog delay locked loop (DLL) is used to adjust the delay time of delay line and lock it to required time. This module is also implemented with sampling trigger which is used to start the sampling circuit.

Section II introduced four types of sampling instant setting. The detail architecture of proposed DPWM is presented in Section III. Simulation results are shown in Section IV.

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II. Sampling Instant Consideration

In digital switching power supplies, the controller samples the voltage/current at the *(n)*th cycle, converts the sampled value into digital code and processes the code by digital compensator, then the DPMW module updates the duty ratio at the beginning of *(n+1)*th cycle and another cycle begins. Due to the characteristics of SMPS, the setting of sampling instant is important. Fig.1 presents four typical types of sampling instant setting. Type I and III are valley and peak value sampling. Type II and IV start at the center of PWM on and off time, which sample the average value of voltage/current.

For type I the time T_c from the sampling instant to PWM duty ratio updating equals almost the switching period. The periods T_c of the other three types are variable. Type II has a T_c at least half of the switching period. For type III and IV the T_c may approach to zero, with the time cost of sample and process, the updating of duty ratio will be delayed at least one cycle, which will slower the response of the system.

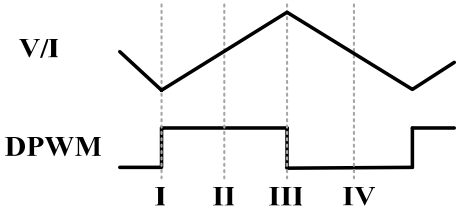

Figure 1. Sampling instant setting of SMPS.

III. Hybrid DPWM Architecture

The structure of proposed hybrid DPWM is as shown in Fig. 2. It's composed of three stages. The first stage is a 5-bit counter, it counts up by one at the time t_{clk} which is period of input clock, this stage generates the most significant 5 bits. The second and third stages are 3-bit delay lines, the second counts for the middle 3 bits and the third counts for the least significant 3 bits. The Analog delay locked loops (ADLL) are used to adjust the delay time of delay lines.

A. Counter as the first stage

The output switching frequency f_{sw} of DPWM is related with the input clock frequency f_{clk} and number bits *n* of the counter,

$$f_{sw}=\frac{f_{clk}}{2^n} \quad (1)$$

The counter based DPWM is simple and fully synthesizable. An important advantage is size efficiency. As for delay line based DPWM, increasing one bit of resolution is at the cost of

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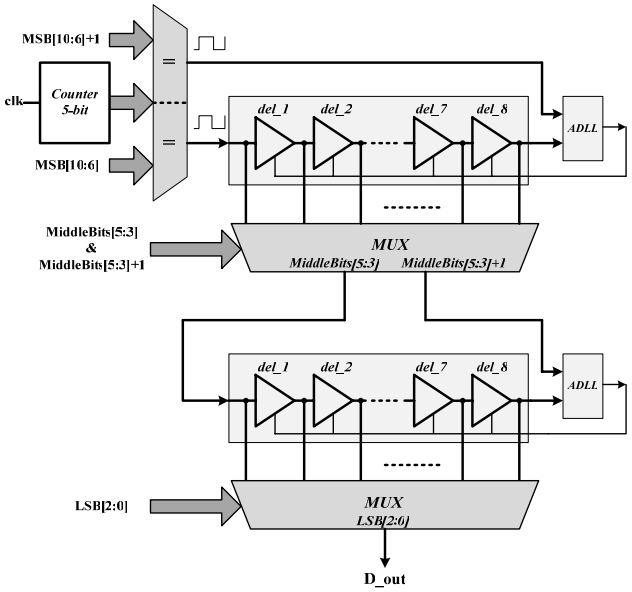

Figure 2. Structure of proposed hybrid DPWM.

doubling the size. While for counter based type, a latch and several NAND gates are enough. However, for a given output switching frequency f_{sw}, a high resolution requires very high input clock frequency, which means high power dissipation. So the number bits of counter should be moderate. In this paper, the counter based first stage is kept as 5-bit. For desired 500KHz switching frequency, the input clock frequency should be 16MHz.

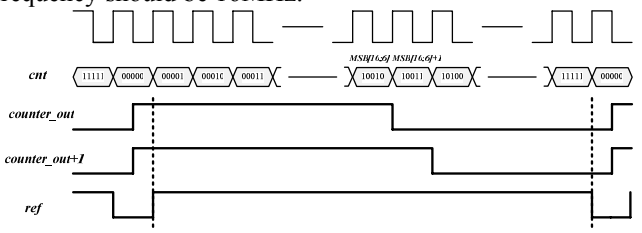

Figure 3. Timing diagram of counter.

The counter counts up at each input clock period, as Fig.3 shows. When the counter value *cnt*="MSB[10:6]", *counter_out* is set to 0. The falling edge then propagates to the second stage. Signal *counter_out+1* is set to 0 when *cnt*="MSB[10:6]+1" , this signal is sent to ADLL to synchronize the middle 3-bit delay line. Due to the characteristics of counter, the effective bits are from "00000" to "11110", which represent the duty from 0% to 93.75%. With the second and third stage, the DPWM can reach a maxim duty of 96.8%.

B. Analog Delay Locked Loop

There are digital and analog types of DLL. Digital module is fully synthesizable but size cost to be adjustable [4]. Analog delay line can be adjusted without changing the delay cell. A typical analog delay locked loop is usually composed of delay lines and a charge pump, the delay time can be changed by adjusting the current of the delay cells [5].

In the proposed DPWM, the second and the third stages are identical 3-bit analog DLLs. The delay cell is as Fig. 4, eight identical delay cells connected in series build up a 3-bit delay line. In Fig.4, *Inv_2* and *M1* form the basic starved inverter, it should be note that this starved inverter can only delay the raising edge of its input. *Inv_1* and *Inv_4* are added to generate a steeper raising and falling edge which means shorter transfer time. This will improve the accuracy especially when the delay time is long.

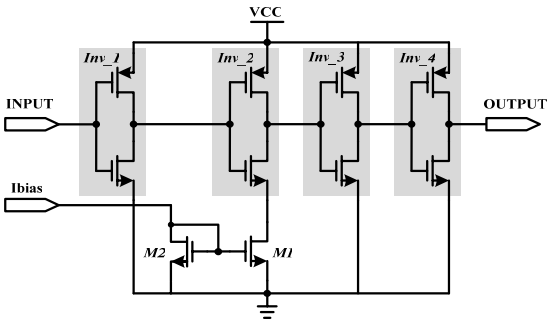

Figure 4. Proposed analog delay cell.

For both digital and analog delay lines, nonlinearity is a problem due to mismatch. Carefully consideration should be taken in circuit layout.

The locked loop principle is similar to that of [6]. Output of the 8th delay cell *del_8* is compared with the reference signal generated by the previous stage, and the result is used as charge signal for charge pump, as shown in Fig.5. A simple V-I circuit is added to convert the voltage into bias current for starved inverters, which improves the noise rejection.

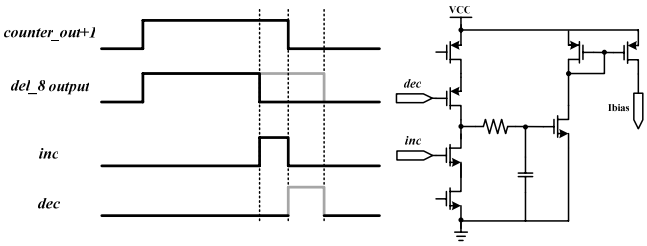

Figure 5. Timing diagram of ADLL comparator.

C. Sampling instant setting

The proposed DPWM provide type I and II of sampling trigger introduced in Section II. Once it reaches the time, the module will output a trigger signal to start the sampling circuit such as ADC.

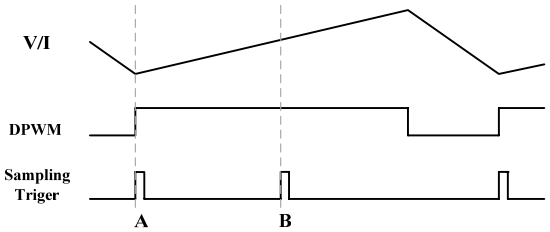

Fig.6 Timing diagram of type I/II sampling trigger.

Type I can be easily achieved by utilizing the rising edge of PWM output as shown the time point A in Fig.6. Type II trigger can be generated by loading half duty (Duty/2) into the DPWM.

IV. Simulation Results

The proposed DPWM is simulated by CADENCE Spectre with TSMC 0.35um mixed signal process. The module is of 11-bit resolution, with a 5-bit counter, a 3-bit middle level delay line and 3-bit low level delay line. Input clock frequency to the counter is f_{clk}=16MHz and the counter generates a PWM wave with switching frequency f_{sw}= $f_{clk}/2^5$=500KHz. The middle level delay line divides the

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period T_{clk}=1/ f_{clk} into 8 equal pieces T_{middle}=7.8125nS, each piece of time is then divided by the low level delay line into 8 pieces T_{low}=977pS.

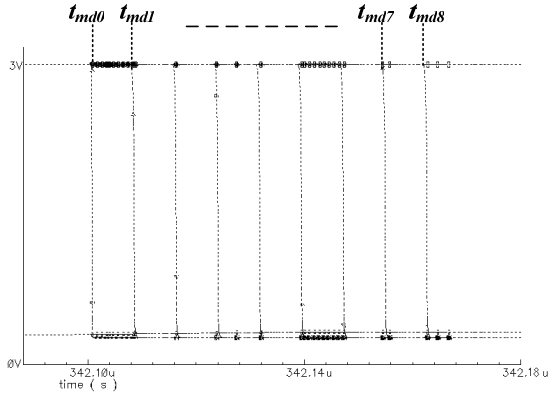

Figure 7. Waveform at delay cells of middle level delay line.

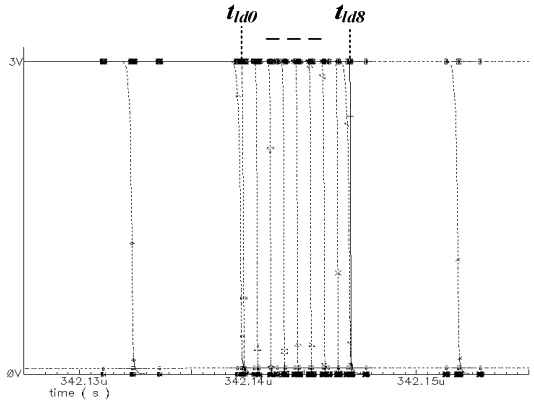

Figure 8. Waveform at delay cells of low level delay line.

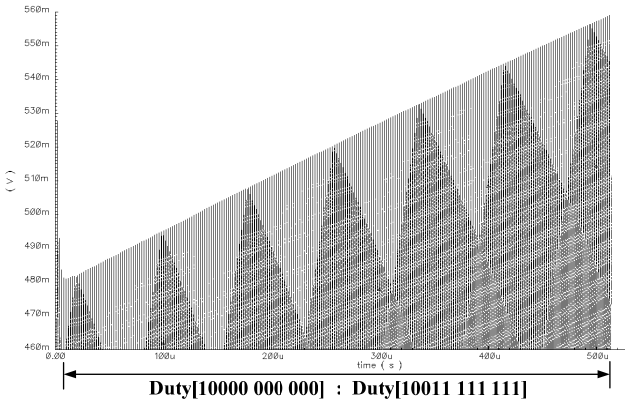

Figure 9. Output of the DPWM module.

Fig.7 and Fig.8 show the falling edge at each delay cell of middle and low level delay lines. A RC filter is connected at the output of DPWM module, the voltage at the capacitor represents the pulse width. Fig.9 gives the output of the RC filter with the input duty from "10000 000 000" to "10011 111 111".

V. Conclusions

This paper introduces a high resolution hybrid DPWM with analog DLL. With the ADLL, the delay line can be accurately locked to input clock. This module also provides two types of sampling trigger to start sampling circuit. The function of this module is simulated at the switching frequency f_{sw}= 500KHz.

References

[1] A.Syed, E.Ahmed, D.Maksimovic, E.Alarcon, "Digital pulse width modulator architectures" *IEEE PESC* 2004, Vol. 6, pp. 4689–4695, June 2004.

[2] Z. Lukic, N. Rahman, A. Prodic, "Multibit Σ-Δ-PWM Digital Controller IC for DC-DC Converters Operating at Switching Frequencies Beyond 10 MHz", *IEEE Trans. on Power Electronics*, vol. 22, no. 5, pp. 1693-1707, Sept. 2007

[3] L.Corradini, A. Bjeletic, R.Zane, D.Maksimovic, "Fully digital hysteretic modulator for DC-DC switching converters" *IEEE ECCE* 2009, pp.3312 – 3319, Sept 20-24, 2009

[4] V. Yousefzadeh, T. Takayama, D. Maksimovic, "Hybrid DPWM with Digital Delay-Locked Loop", *Computers in Power Electronics*, 2006, COMPEL '06, IEEE Workshops on, pp. 14-48.

[5] W.Gu-Yeon, M.Horowitz, "A low power switching power supply for self-clocked systems," *International Symposium on Low Power Electronics and Design*, pp. 313 – 317, Aug. 1996.

[6] A. P. Dancy and A. P. Chandrakasan, "Ultra low power control circuits for PWM converters," in Proc. *IEEE PESC'97 Conf.*, 1997, pp. 21–27.

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