A MOSFET-Only Delta-Sigma Modulator for Implantable Neural Signal Sensors

Rui Fan, Jian Xu, Xiaobo Wu†

***Abstract*-A low voltage high linearity MOSFET-only Delta-Sigma modulator for implantable neural signal sensors is presented in this paper. In order to reduce the capacitor area significantly, most of the capacitors in the modulator are implemented by the single PMOSFET MOSCAPs in inversion region. The rest capacitors are realized by series compensated MOSCAPs to ensure high linearity over the wide swing. A DC level shift technique is employed in the first integrator to guarantee the PMOSFET in the inversion region and thus extend the input signal swing. Besides, a 4-bit quantizer is applied to increase the signal-to-noise-and-distortion-rate (SNDR) and decrease the output swing of each integrator for the linearity optimization of MOSCAPs. The bottom terminal parasitic effect of PIP (poly-insulator-poly) capacitors is also eliminated completely as a result of MOSCAPs application. The modulator is simulated in a 0.35μm n-well standard CMOS process and achieves 104dB SNDR at 8k-Hz signal bandwidth. Compared with the PIP capacitor design, this work reduces about 77% of the total capacitor area.**

***Index Terms*-MOSFET-only, inversion region, Delta-Sigma modulator, MOSCAP.**

I. INTRODUCTION

Coincident with the biomedical development, implantable devices gain increasingly attention in both industry and institutes, since they can benefit from the high level of integration in submicron CMOS technologies. One of the most important concerns in implantable devices design is the chip size. In Delta-Sigma modulators for implantable devices, a large part of the area is consumed by sampling and integrating capacitors. However, in a standard 0.35μm CMOS process, the capacitance density (capacitance per unit area) for a PIP capacitor is only 0.889fF/μm^2, and there is about 20% parasitic capacitance at the bottom terminal. Therefore, circuit designers have to face a considerable cost on capacitor area as well as the parasitic effect of PIP capacitors.

One promising way to solve the problems without special processes is to use the parasitic capacitor of a MOSFET, which is also called MOSCAP. As shown in Fig. 1, its highest capacitance density in a certain region is 5 times as much as that of the PIP capacitor, because the capacitor of thin oxide dielectric layer at the gate of a MOSFET, C_{ox}, constitutes a high density capacitor. However, the capacitance density shows strong dependence on the voltage at both nodes because the charge distributes differently in accumulation, depletion and inversion regions. The capacitance variance of MOSCAPs restricts their use in high resolution Delta-Sigma modulators.

In former works [2] and [3], the modulators achieved no more than 75dB SNDR. They are not suitable for high resolution measurement. The input signal of the modulators is limited to less than -6dB, so they cannot deal with large signal swing. Therefore, their practical value is undermined. As the capacitance density of the serially compensated MOSCAP in depletion capacitors is even lower than that of MIM capacitor, the area efficiency of the modulators is not so satisfactory. In addition, the parasitic capacitance of the serial MOSCAP is not considered yet.

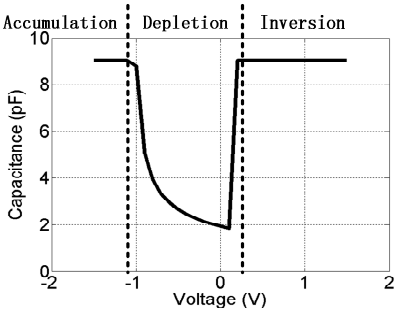

Fig. 1. C/V feature of a MOSCAP

In this work, most of the capacitors in modulator are substituted by single PMOSFET MOSCAPs in inversion region, so the area declines significantly. A DC shift in the input and feedback signals is employed to extend the input swing. A 4-bit quantizer is used to improve the SNDR and reduce the output swing in each integrator. There is no parasitic capacitor like PIP capacitors or serial MOSCAPs in [2][3], so operational amplifiers (opamp) in the modulators can be implemented more easily.

Section II discusses the MOSCAP structure and its C/V feature. Then a compensation method is presented to linearize the capacitance. Section III shows the modulator topology and MOSCAP application. Details of circuits are presented in this section. Section IV illustrates the simulation results and is followed by the conclusion.

II. MOSCAP DESIGN

A. Traditional MOSCAP

For a PMOSFET as shown in Fig 2, it can be viewed as a device of four nodes with parasitic capacitor between each node. Thus, a MOSCAP can be realized by choosing two from the four nodes as input/output nodes and leaving others properly connected and biased. Moreover, various types of complex MOSCAP can be derived from the combination of different single PMOSFET MOSCAPs. Nowadays, to save

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ISBN: 978-988-18210-4-1
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

area, MOSCAPs with high density are often used in applications where capacitance accuracy can be neglected. So MOSCAPs are seldom employed in high resolution ADCs because the linearity and accuracy of capacitors are essential for element matching and system accuracy.

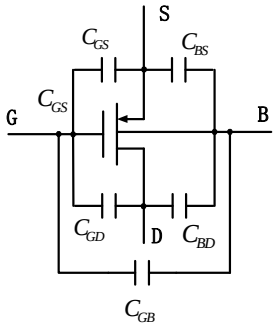

Fig. 2. A P MOSFET and its parasitic capacitance

B. *Linearity compensation of MOSCAP*

In Fig. 3 and Fig. 4, the crossover section of a typical PMOSFET MOSCAP and the C/V characteristics are shown. As depicted, this MOSCAP works in three regions as the input voltages increases: accumulation, depletion and inversion. In accumulation and inversion regions, it shows great advantages in capacitance density and linearity, but in depletion region, the capacitance density and linearity both deteriorate.

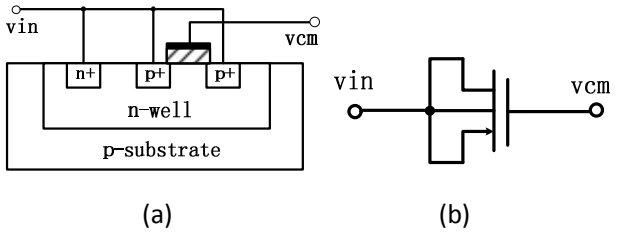

Fig. 3. (a) The crossover section and (b) the circuit of a PMOSFET MOSCAP

The reason for this variance is as follows. While in inversion region, the source and drain can be considered as one connected node and they screen the charge change in the body. Thus in other words, the sum of C_{GS} and C_{GD} is the gate oxide capacitance, C_{ox}, plus the overlap capacitance, $C_{ov,}$ between the gate and p-well.

$$C_{MOSCAP}=C_{GB}+C_{GS}+C_{GD}=C_{ox}+2C_{ov} \quad (1)$$

In accumulation region, C_{GS} and C_{GD} reduce to the value of the overlap capacitance, C_{ov}. Source and drain of the MOSFET are disconnected because the inversion layer disappears. Then C_{GB} becomes the gate oxide capacitance. The total capacitance of the MOSCAP is as follows:

$$C_{MOSCAP}=C_{GB}+C_{GS}+C_{GD}=C_{ox}+2C_{ov} \quad (2)$$

In depletion region, as a result of serial connection of the gate oxide capacitor and the depletion layer capacitor, C_{GB} decreases. The total capacitance varies because the depletion layer Capacitance, C_{dep}, or more exactly the width of the depletion layer, varies with the voltage V_{GB}. Therefore, C_{GB} is voltage dependent and smaller than C_{ox} as (3).

$$C_{MOSCAP}=C_{GB}+C_{GD}+C_{GS}=\frac{1}{C_{ox}^{-1}+C_{dep}^{-1}}+2C_{ov} \quad (3)$$

As Fig. 4 shows, when the input voltage vin is 0.2V higher than vcm, the PMOSFET is in inversion region. The capacitance MOSCAP is not only linear but also dense. Unfortunately, the common mode voltage, vcm, of the operational amplifier (opamp) in Delta-Sigma modulator is usually higher than ground, so the input signal swing is limited if the single PMOSFET MOSCAP is used.

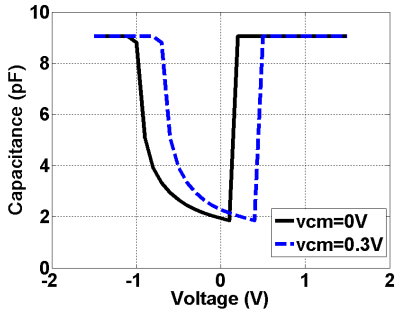

Fig. 4. MOSCAP C/V characteristics

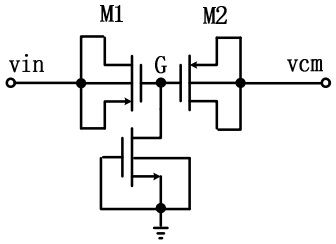

Fig. 5. The MOSCAP in series connection

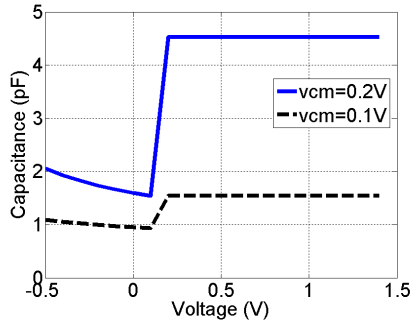

Fig. 6. C/V feature of series compensated MOSCAP

Although the PMOSCAP shows strong dependence of vcm in depletion region, linearity can be truly improved by using some circuit design techniques. In Fig 5, the serial compensation technique is applied for high linearity. When two PMOSFET MOSCAPs are anti-serially connected, the voltage of node G where the two gates connect is virtual ground. Therefore, the linear range of the MOSCAP is extended. The PMOSFET M1 operates in inversion region and the resultant capacitance of the two serial capacitors is invariant, if vin and vcm are both higher than 0.2V, as shown in Fig. 6. The NMOSFET ensures that there is a high resistance path from the node G to the ground. However, a drawback should be noted. When the common mode voltage vcm is lower than 0.3V, the resultant capacitance will become small because the MOSFET M2 is in depletion

ISBN: 978-988-18210-4-1
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

region, and its capacitance is of small value.

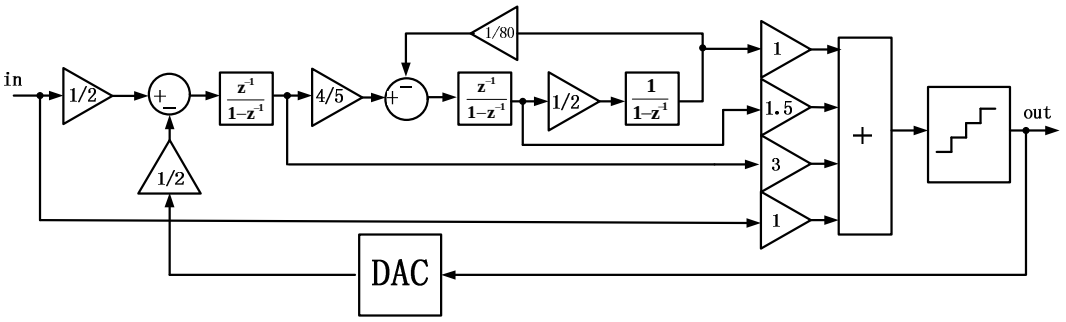

Fig. 7 . Behavior model of the Delta-Sigma modulator

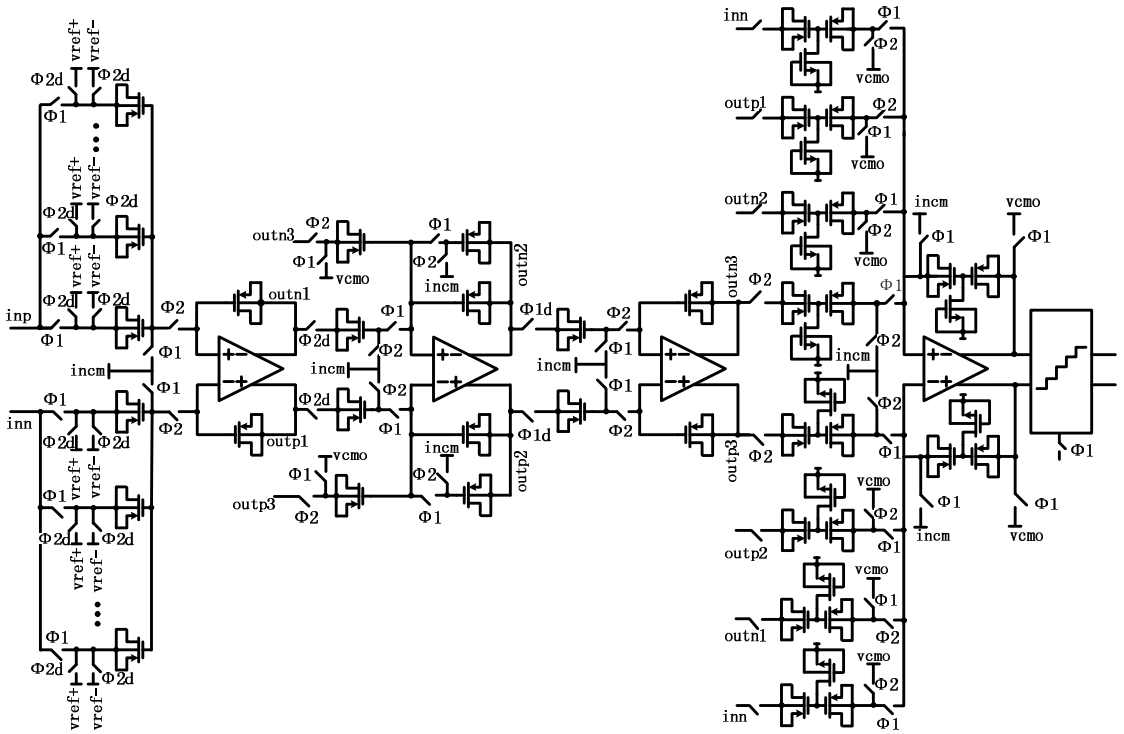

Fig. 8. Modulator circuits with the MOSCAP application

III. Modulator Design

A. Modulator Architecture

In Fig. 7, the modulator structure is depicted. A three-order modulator with a structure of "chain of integrators with local resonator feedbacks and feedforward summation" (CRFF) is used in this work since the expected area of the chip is small and 14-bit can be achieved without much power consumption. An active adder is composed by the feedforward active adder to sum up and scale down the feedforward signal. To attain a high resolution and reduce the signal swing, a 4-bit quantizer is used instead of a unit quantizer.

B. DC Level Shift and MOSCAP Application

As mentioned in section II, high linearity and density are both achieved when MOSCAPs operate in accumulation and inversion region, so the output scope of each integrator in modulator should be carefully scaled and, moreover, types of MOSCAPs should also be chosen accordingly.

In the first integrator, the input signal swing is as large as 0.8 V_{pp}, excluding the feedback reference voltage. In order to take advantage of the high density of the single PMOSFET MOSCAP, the input and feedback signals are shifted to a higher voltage to ensure the MOSCAPs in inversion region. There is no need to reset the common mode input voltage of the opamp in the first integrator, because the opmap is disconnected to the MOSCAPs while sampling. Furthermore, in spite of the DC level shift of input signal, the influence is canceled by fully differential structure. In the second and third integrators, the capacitors are also implemented by single PMOSFET MOSCAPs because the small output swings of the integrators keep the MOSCAPs in inversion region. At the output of the active adder, the serially compensated MOSCAP is used to accommodate the wide swing. Circuit details are shown in Fig. 9. Unlike the PIP capacitor, there is no extra parasitic capacitor in MOSCAPs. As the body, source and drain of the MOSFET are connected as one node and gate alone is as the other node, there are no extra parasitic capacitor connected to ground. Thus the parasitic capacitor at the bottom terminal of the PIP capacitor is completely eliminated in the

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circuits. The design requirement of the opamp is relaxed.

IV. Simulation Results

This modulator is simulated in a tsmc 0.35um n-well CMOS process. The supply voltage is 1.5V and clock frequency is 512-KHz. Simulation is performed by using a sinusoidal signal with 2-kHz frequency and 0.6V amplitude. An oversampling rate of 32 results in an 8k-Hz bandwidth. Fig. 10 shows the peak SNDR for sinusoidal signal of -1.9dB. The PIP capacitance per unit area is 0.89fF/μm^2. The density of single PMOSFET MOSCAP is simulated as 4.52fF/μm^2, and the density of serially compensated MOSCAP is 1.13fF/μm^2. Compared with the PIP capacitor, the MOSFET-only modulator attains the same performance with a reduction of 77% of capacitor area. Details of capacitors in each integrator and the adder are depicted in Fig. 9.

Table I

SIMULATED MODULATOR PERFORMANCE

Clock Frequency	512-KHz
Oversampling Rate	32
Signal Bandwidth	8-KHz
Peak SNDR	104dB@-1.9dB
Supply Voltage	1.5V
Process	0.35μm CMOS

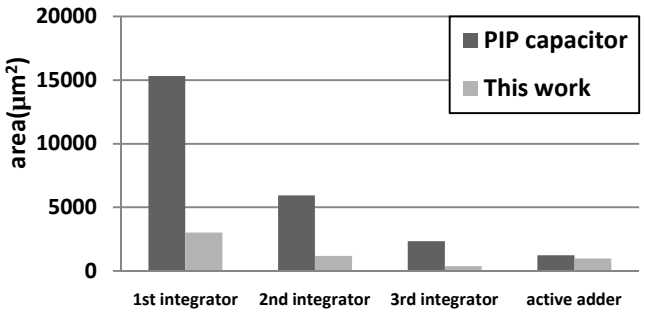

Fig. 9. PIP capacitor area versus MOSCAP area

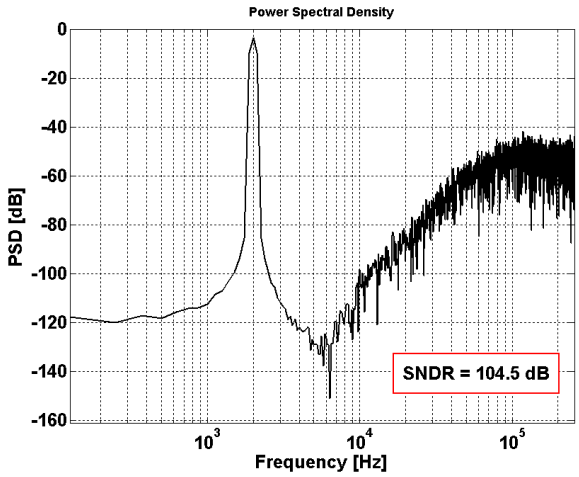

Fig. 10. The simulation results for f_{clk}=512KHz, f_{in}=2KHz and V_{in}=-1.9dB

V. Conclusion

A 1.5V MOSFET-only Delta-Sigma modulator with a DC level shift technique is implemented and simulated. It is compatible with the standard CMOS process and achieves 104dB peak SNDR. The modulator employed single PMOSFET MOSCAPs in inversion region for the three integrators and series compensated MOSCAPs for the feedforward adder. Compared with the PIP capacitor implementation, this work saved 77% of capacitor area. As the capacitors in the first integrator, which occupy a large part of area among the total capacitor, is replaced by single high density PMOSFET MOSCAPs, the capacitor area is further reduced. Besides, there is no parasitic capacitor at the MOSCAP terminals. So the design requirements of opamps in the modulator are also relaxed.

Acknowledgment

This paper is sponsored by the National Natural Science Foundation of China under grant No.90707002. It also gains support from the Analog Devices, Inc. (ADI). The authors would like to thank Mr. Bill Liu, the senior engineers of ADI and his colleagues, for their useful discussions and instruction.

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ISBN: 978-988-18210-4-1
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)