Implementation and Analysis of Quasi-Adiabatic Inverters

Prasad D Khandekar, *IAENG member*, Shaila Subbaraman, and Abhijit V. Chitre

***Abstract*— Sharply increasing need for portable electronic devices has reinforced the need of low power design methodologies in the recent years. Adiabatic logic style is proved to be an attractive solution for low power digital design. The energy is recycled back to power supply instead of being wasted. Many researchers have introduced different adiabatic logic styles in the past few years. This paper discusses the implementation of three quasi-adiabatic logic styles and analyzes the charge flow. All the inverter circuits are designed using 180nm technology in Cadence design environment.**

***Index Terms*—Low Power VLSI, Adiabatic, Energy Recovery.**

I. Introduction

The circuit complexity and processing speed are rapidly increasing whereas silicon area has to be as minimal as possible. This has resulted in the exponential rise in heat generated per unit area. The range and sophistication of applications of digital systems are increasing everyday in portable and embedded computing. Issues such as battery operation time, weight, size etc demand dramatic reduction in power dissipation. It is anticipated that the expected battery life time will not increase by more than 30% over the next few years. In the absence of low power design techniques, future portable systems will suffer from very short battery life time and oversize battery packs. The design engineers of high-end systems also face challenge of the increasing power dissipation with the increase in area-frequency product. The empirical expression for power dissipated is, $P = \alpha \times area \times f_{clock}$ with $\alpha = 0.063$ W/(cm^{2}MHZ). This means that a 5 cm^2 microprocessor clocked at 500 MHz would consume about 160W. Thus, packaging and cooling strategies will have to be refined putting an extra overhead on the cost. In addition to cost and system design issues, the reliability is also affected by the high temperature. The high temperature causes electro migration, gate dielectric breakdown and other silicon failure mechanisms. All these have fuelled the research activity in low power design at universities, research laboratories and industry. Low power digital design is an optimization problem at all abstraction levels of the design viz. technology, device, circuit, logic, architecture, algorithm and system levels. An adiabatic switching technique based on energy recovery principle is one of the innovative solutions at circuit and logic level to achieve reduction in power.

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II. Adiabatic Principle

Energy recovery principle can be best understood by comparing the energy dissipation in conventional CMOS circuit with that of adiabatic switching circuit. CMOS has prevailed as the technology for low power digital design because of its negligible static power dissipation. The leakage currents and sub-threshold injection currents give rise to a static component of CMOS power dissipation. The short circuit power dissipation is also low because it occurs for a very short time. The major contributor is dynamic power dissipation which results from charging and discharging of a load capacitor as shown in fig 1. In case of CMOS inverter, when the input is logic zero, pFET connects V_{dd} to the load capacitor C_L and a charge equals to $Q = C_L V_{dd}$ is stored on the load capacitance. The energy consumed to store this charge is Q. $V_{dd} = C_L (V_{dd})^2$. Fifty percent of this energy is dissipated in the pFET and it is independent of resistance of the pFET and time taken for charging. The remaining fifty percent is stored on the C_L. When the inputs are inverted then the energy stored on the C_L is dissipated in the nFET. Thus, from energy conservation point of view, conventional CMOS logic represents the worst case of energy wastefulness.

The energy dissipated in charging and discharging the load capacitor in one input cycle is $C_L . (V_{dd})^2$ and it is dissipated as a heat. The amount of energy lost is exactly twice the signal energy. To minimize the energy dissipation if we reduce the signal energy then it will also increase sensitivity to background noise. It is therefore important to reduce the switching energy.

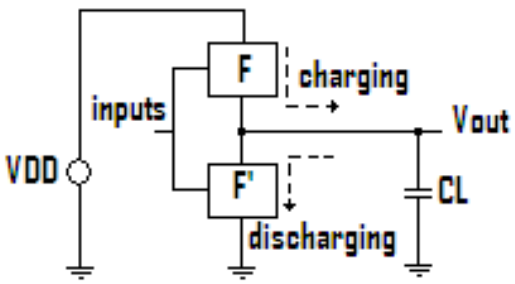

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Fig.1. Conventional CMOS charging and discharging

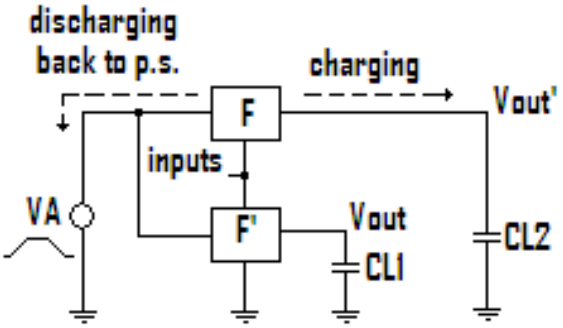

Fig.2. Adiabatic charging

Charges are distinguished as controlling and controlled charge and in case of MOSFET, the controlling charge is on the gate and the controlled charge flows from drain to source in the channel. The energy is dissipated in the pFET or nFET because of the resistance offered by the channel of the FET to this controlled charge. The energy that would be dissipated in the channel can be minimized if this charge transport in the channel is slowed down [1]. A constant current source can be used to deliver a charge of C_L. V_{dd} for a time T. The energy dissipation in the transistor will be,

$$Ediss = P \times T = I^2 \times R \times T = \left(\frac{C_L \times V_{dd}}{T} \right)^2 \times R \times T$$

$$Ediss = \left(\frac{R \times C_L}{T} \right) \times C_L \times V_{dd}^2 \qquad (1)$$

The above equation indicates that it is possible to reduce the energy dissipation by using a constant current source instead of constant voltage supply and increasing charging (or discharging) time T. This principle is called 'adiabatic charging'. The term adiabatic is taken from Thermodynamics and it means without the flow of heat. In adiabatic switching circuit, the energy dissipation can be reduced to an arbitrary degree and thus heat generation is minimized. The charge flow in a typical adiabatic circuit is shown in fig. 2. Instead of using a separate power supply for V_{dd} and for clock, the clock signal can be reshaped and be used for both the purposes. This clock signal is called power-clock following the example given by Denker [10]. Dynamically adjusting the power-clock voltage to comply with constant-current charging results in adiabatic-charging effect. A ramp type power-clock supply VA is shown in the fig. 2. The power-clock voltage is in the form of a ramp or sinusoidal signal. The power-clock supply charges the load capacitor adiabatically during the time it is ramping up and allows has the load capacitor energy to recycle back when it is ramping down. This adiabatic cycling of energy between the logic circuit load and the power-clock supply needs an adiabatic path. It is possible to have the same path for charging and discharging reversibility but it is recommended to have separate paths for charging and discharging as shown in fig.2. Many charge steering and pre-charge design techniques can be employed to design adiabatic circuits.

The adiabatic circuit has adiabatic loss and non-adiabatic loss in addition to leakage loss. The adiabatic loss occurs if the charge is transferred through a transistor which is turned ON. This adiabatic loss can only be avoided if the rise time of pulsed voltage supply is at least three times the time constant of the circuit i.e. by reducing the charge transfer time through the channel.

Whereas, the non-adiabatic loss occurs when there is a nonzero voltage difference between the terminals of a switch when it is turned ON. This non-adiabatic loss can be higher than the adiabatic loss if the operating frequency is lower. The energy dissipated per transition can be reduced by operating the transistors according to two principles [2];

1. When the FET is OFF, the source and drain are brought to the same potential.
2. When the FET is ON, the source potential can vary while the drain floats. The variations should be sufficiently slow so that the drain with a negligible potential difference between source and drain.

The adiabatic switching technique is an effective low power design technique for circuits where the circuit load can be characterized as capacitive. In CMOS circuits, the gate to channel capacitance is the capacitive load (ignoring parasitic capacitances). The channel current is controlled by charging and discharging this capacitance.

An adiabatic path is required between the capacitive load and the regenerator to adiabatically cycle the energy between the two. It is very essential that the characteristics of the charging path and discharging path should be the same and the logic state should be held constant throughout the entire charge and discharge cycle. Many charge steering and precharge design techniques can be employed to design adiabatic circuits. Adiabatic circuits are of two types: quasi-adiabatic circuits and fully adiabatic circuits. Quasi-adiabatic circuits do have non-adiabatic loss whereas fully adiabatic circuits do not have adiabatic-loss as well as non-adiabatic loss. The range of frequency for quasi-adiabatic circuits [3] can be divided into three regions. In low frequency range, the adiabatic losses are minimum and in high frequency range, the leakage losses are minimum. The overall energy dissipation is low in the mid frequency range. These three ranges of frequencies are different for different quasi-adiabatic circuits because the numbers of transistors, power-clock schemes vary.

Full adiabaticity can not be achieved because a digital system can not be isolated from the external environment completely. Hence it can be asymptotically achieved. The fully adiabatic circuit employs reversible logic to eliminate non-adiabatic loss virtually [4]. But the complexity of the adiabatic circuit is high because they have forward and backward logic paths due to reversible logic. The full adiabatic circuits use logic switches and isolation switches. Quasi-adiabatic circuits do not require isolation switches and hence consume less silicon area. Therefore quasi-adiabatic circuit is better design option. The timing of input signal and power-clock supply is not critical in quasi-adiabatic circuits. Implementation and analysis of quasi-adiabatic circuit is discussed in the next section.

III. IMPLEMENATION AND ANALYSIS OF QUASI-ADIABATIC INVERTER

To carry out the analysis, three quasi-adiabatic logic styles were selected viz. Efficient Charge Recovery Logic (ECRL) [5], Clocked CMOS Adiabatic logic (CAL) [6] , and Latched

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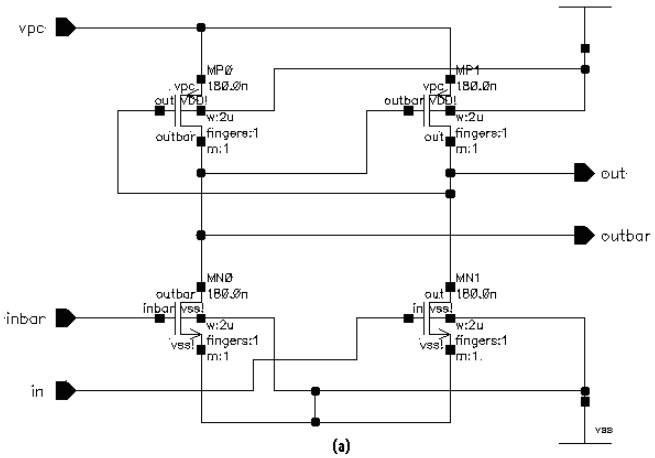
Pass Transistor Adiabatic Logic (LPAL) [7]. The simulation results were compared with that of conventional CMOS 2:1 MUX.

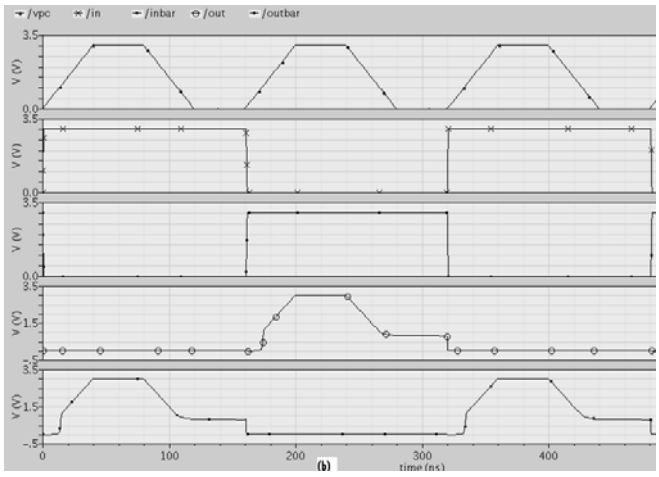
A. ECRL Inverter

ECRL performs precharge and evaluation simultaneously. It dissipates less energy as it does not use any precharge diode. ECRL has the same circuit structure as cascade voltage switch logic with differential switching. The circuit schematic of a simple ECRL inverter is shown in fig. 3a. The signals are dual rail type. Let us assume that 'in' is at logic high and 'inbar' is at logic low. When the power-clock signal 'vpc' rises from zero to V_{dd}, the 'out' is grounded through MN1. During the hold phase, the 'vpc' signal is fixed at V_{dd} and the valid output voltage level is used as input for the next state. After the hold phase, the 'vpc' voltage ramps down to zero and 'out' node recycles its energy back to power-clock supply. Actual input and output waveforms are shown in fig. 3b. The input applied is a pulse type signal.

If the inverters are to be cascaded then multi-phase clock supply needs to be applied. This will allow the next stage to evaluate logic values in the precharge and evaluation phase when the present stage is in the hold state. A chain of four inverters would require four-phase clocking to efficiently recover the charge.



(a) Circuit schematic of ECRL inverter

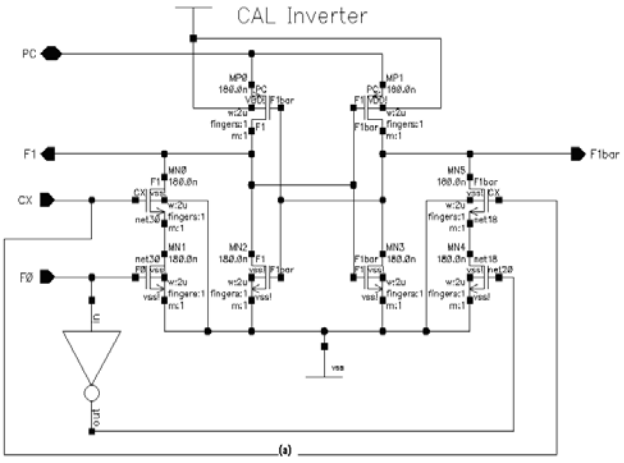


(b) Input and output waveforms of ECRL inverter
Fig.3. ECRL inverter

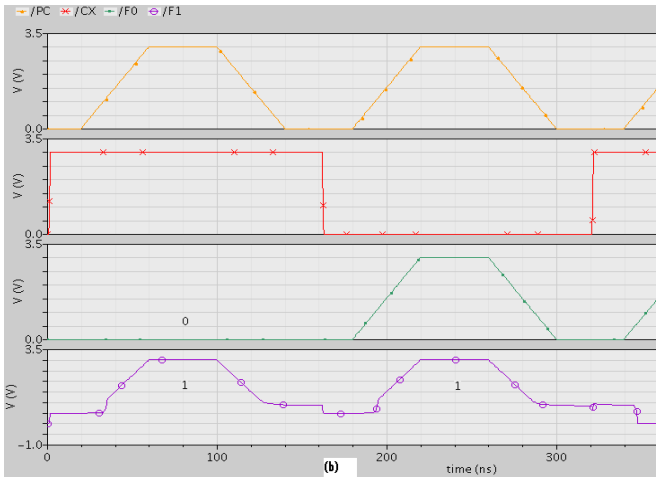
B. CAL Inverter

CAL logic style is designed to overcome the need of the multiphase power-clock supplies required for proper interfacing between stages. CAL logic circuits can be implemented with integrated single-phase power-clock supply and thus eliminates high complexity of both the logic and the required power-clock generator. The basic circuit structure of CAL inverter is shown in fig. 4a and uses a cross coupled CMOS inverters made up of MP0, MN2, MP1, and MN3. An auxiliary timing control signal 'CX' controls transistors MN0 and MN5 those are in series with the logic blocks; for inverters the logic blocks are NMOS transistors MN1 and MN4. The CX-enabled transistors allow the use of single power-clock.

The input and output waveforms after simulating the circuit in cadence design environment are shown in fig 4b. The auxiliary signal CX is a pulse type signal whereas input 'F0' and power-clock supply 'PC' are ramp-type signals. When the CX signal is logic high it allows MN1 to invert the input signal and therefore the output signal high i.e. ramp. The output is considered to be logic high when it replicates the power-clock voltage waveform. Thus, the outputs of adiabatic circuits are not fixed dc logic voltage levels but they follow power-clock voltage shape.



(a) Circuit schematic of CAL inverter



(b) Input and output waveforms of CAL inverter
Fig.4. CAL inverter

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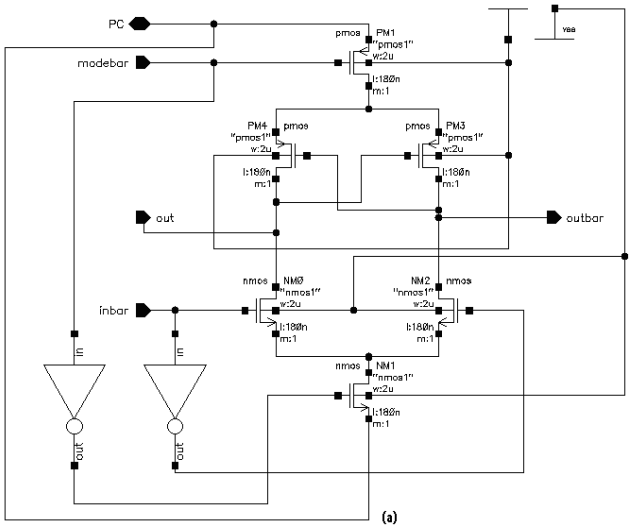
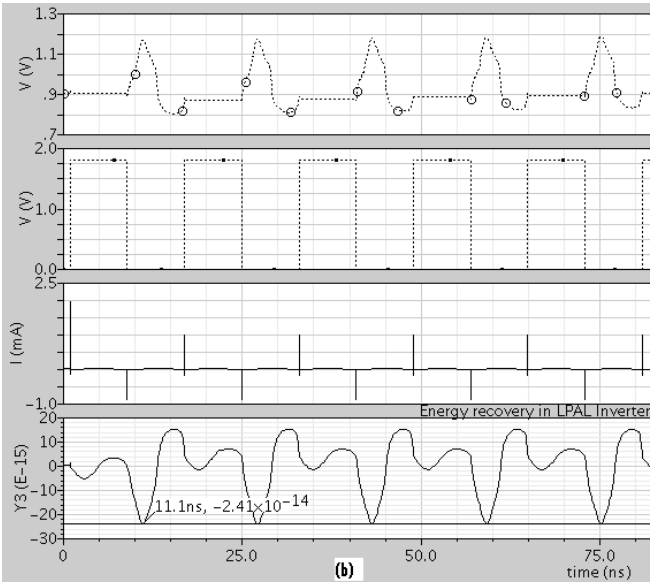
C. LPAL Inverter

A LPAL is a refined version of Pass-Transistor Adiabatic Logic (PAL) style [8] and uses two-additional mode select transistors PM1 and NM1. The circuit schematic of LPAL inverter is shown in fig. 5b. When the 'mode' signal is high the LPAL inverter behaves as a normal PAL inverter. The circuit disconnects itself from the power-clock supply 'PC' when the 'mode' signal is low. The output levels are held at previous levels. This mode reduces adiabatic loss. Authors have used inverters to generate the dual rail input. These two inverters are non-adiabatic and hence consume more power.

Because an adiabatic circuit has dynamic outputs by a dynamic power-clock, the outputs must be latched when applied as inputs to the next combinational logic block which LPAL does. Fig. 5 b shows the energy dissipation in LPAL inverter. It may be noted that energy is being recovered after every input cycle. The energy dissipation after first input cycle is 0.24pJ which is very less as compared to CMOS inverter.



(a) Circuit schematic of LPAL inverter



(b) Input and output waveforms of ECRL inverter

Fig.5. LPAL inverter

IV. CONCLUSION

Reducing power consumption has become an important issue in System on Chip (SoC) and VLSI Design areas. Conventional static CMOS can not avoid an abrupt voltage drop when input transits alternatively. For example, if input changes from zero to V_{dd}, the voltage drops abruptly across the load capacitor and ground through NMOS. Adiabatic logic achieves low power by maintaining small potential differences across the transistors while they are conducting, and allowing the charge stored in the output load capacitors to be recycled [9]. A power-clock supply plays an important role in adiabatic switching. When it ramps up or down steadily, the power-clock supply causes a very small drop across the switching device. The power-clock supply not only supplies the energy but also recovers it. Adiabatic inverters are the simplest form of benchmark circuit to demonstrate the principle of energy recovery and the adiabatic principle. Our experiments on adiabatic inverters show that the energy recovery can be up to 90% if the transistors are minimally sized. The adiabaticity is observed up to a frequency governed by the circuit time-constant

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