Low Power Op-Amp Based on Weak Inversion with Miller-Cascoded Frequency Compensation

Maryam Borhani, Farhad Razaghian

***Abstract*—A design for a rail-to-rail input and output operational amplifier is introduced. The circuit operates with 0.8 V single supply. The rail-to-rail input stage with controlled g_m is obtained by biasing transistors in weak inversion and one-times current mirror. The opamp provides a DC gain of 78 dB and gain-bandwidth (GBW) of 1.7 MHz at a 13 pF, 108 kΩ load by using 0.18 μm CMOS process (V_{tn}= 0.4 V and V_{tp}= -0.4 V). The power consumption is 10 μW and g_m variations are 6.4% over the entire input common-mode voltage range.**

***Index Terms*—Low Voltage, Rail-to-Rail, Weak Inversion, Constant G_m.**

I. Introduction

In recent years, the importance of integrated circuits design with low supply voltage is increased. The operational amplifier (opamp) which is a fundamental building block in the analog and mixed- mode circuits, is not an exception [1].

Some reasons can be given for the need to low voltage circuits [2]. First, as the integrated devices dimensions become smaller, gate-oxide with several nanometers thickness is subjected to lower breakdown voltages, so it requires lower supply voltage for ensuring device reliability. The second reason is due to increasing the demand of battery-powered portable equipment. In the portable devices such as laptop, implantable cardiac pacemakers, wireless communication devices and hearing aids, low power dissipation is important to have suitable battery life and weight. In these applications, the supply voltage has to be reduced in order to have reasonable operation period from a battery. The third reason is dictated by increasing packaging density of the components on silicon chip. The chip can dissipate limited amount of power per unit area, hence power per electronic function has to be reduced in order to prevent overheating of the silicon chip.

The low supply voltage limits the input common-mode and dynamic range of op amps [3]. In order to obtain a large dynamic range and high signal-to-noise ratio, the common-mode range (CMR) must be kept as large as possible. As the result, to compensate the reduced input common-mode and dynamic range, the operational amplifier should be able to deal with signals that extended from the negative supply rail to the positive supply rail, i.e., rail-to-rail.

In this paper, a compact two stages operational amplifier with rail-to-rail input and output signal swing is presented by using the approach from [4], [5]. The supply voltage sub-1v is employed. Hence, most of the transistors operate in weak inversion.

The performance of the proposed amplifier is described in section II. The design parameters are given in section III. The simulation results are presented in section IV and the conclusions are drawn in section V.

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II. Circuit Description and Operation

The overall architecture of the proposed operational amplifier is shown in Fig. 1. In the next subsections, the input and output stages and frequency compensation of the opamp will be discussed.

A. Constant-G_M Rail-to-Rail Input Stage

The conventional scheme to design rail-to-rail input stages is through utilizing complementary differential pairs by placing a p-channel differential pair and n-channel pair in parallel [6], [7]. There are basically three operation regions [8]; when the input CM voltage, $V_{i,\,cm}$ is near the positive or the negative supply, only the nMOS or the pMOS differential pair is active, respectively. For $V_{i,\,cm}$ around middle range, both differential pairs are active. This common-mode range overlap provides a forbidden voltage region in the amplifier' s common-mode input range. If the applied $V_{i,cm}$ falls within this range, it will not be amplified properly. In order to avoid a forbidden voltage region in the middle range, the supply voltage has to be at least:

$$V_{SUP(\min)} = V_{gs,n} + V_{gs,p} + V_{ds,n} + V_{ds,p} \quad (1)$$

where $V_{gs,\,n}$, $V_{gs,\,p}$ are the gate-source voltages of the differential pairs and $V_{ds,\,n}$, $V_{ds,\,p}$ are the saturation voltages of the current sources. If the input transistors operate in strong inversion, considering threshold voltages of about 0.4 V and saturation voltages of 0.2 V, we have a supply voltage of 1.2 V. In order to reduce this value, we tend to bias transistors in weak inversion.

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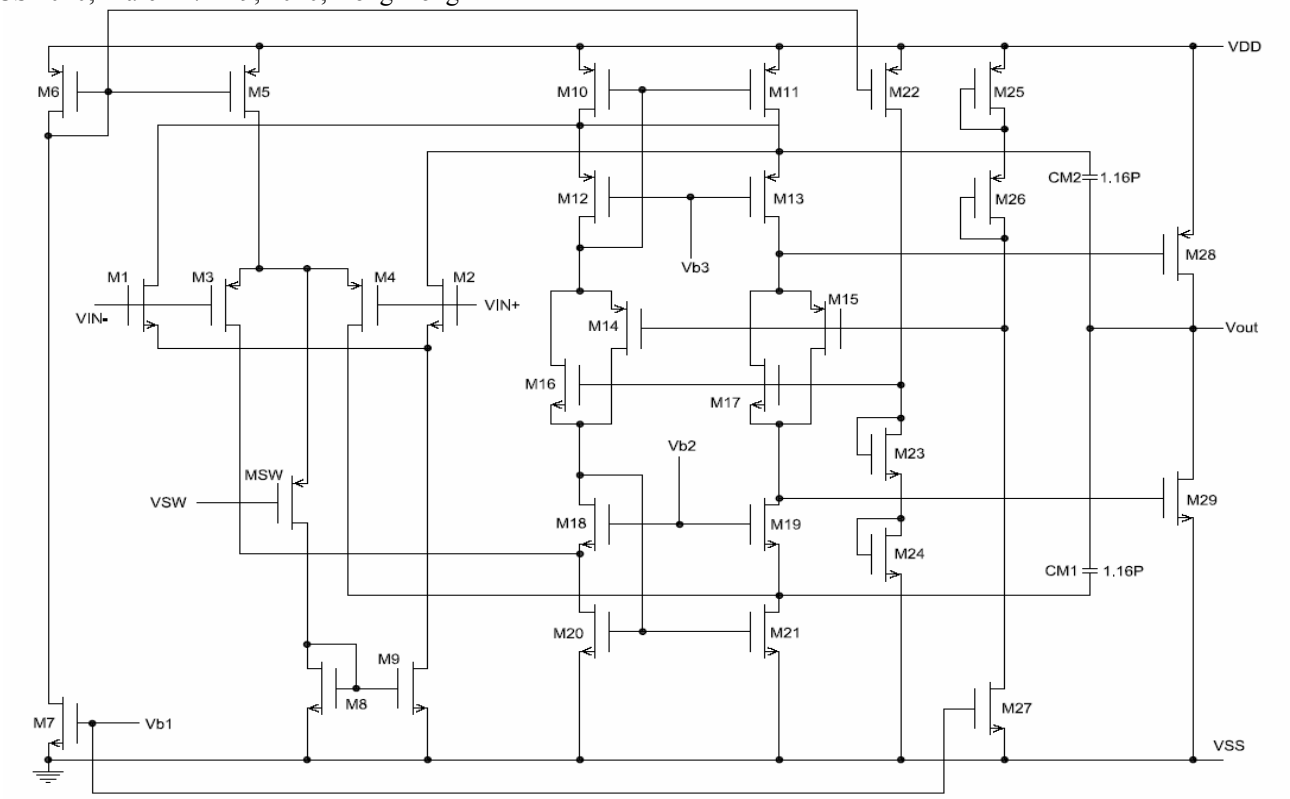

Fig. 1. Overall architecture of the proposed operational amplifier

However, the total transconductance (g_{mT}) of input stage when both differential pairs are active is twice of that when just one pair is on. This fact impedes optimal frequency compensation, since the unity-gain bandwidth of the op-amp is proportional to that transconductance. Hence, some extra circuitry and constant-g_m techniques are required to keep the total transconductance constant.

Several techniques have been reported to overcome gm variations problem [1], [4], [9-11]. In the Most of these methods, the input stage transistors are biased in strong inversion and are employed complex biasing forms.

However, this is a simple solution. This idea is based on a bipolar counterpart [7]. In the bipolar technology (MOSFET in weak inversion), the transconductance is proportional to the collector (drain) current by:

$$g_m = \frac{I_C(I_D)}{nU_T} \tag{2}$$

where n is the weak inversion slop factor, and U_T = KT/q is the thermal voltage.

In the input stage given in Fig. 1, if transistors M_1-M_4 operate in weak inversion, the total g_m is given by [11]:

$$g_{mt} = \frac{I_n}{2n\,U_T} + \frac{I_p}{2nU_T} \tag{3}$$

where I_n and I_P are the tail currents of the input pairs.

Therefore, in order to have a constant g_m operation the sum of the tail currents must be according to the following expression:

$$I_p + I_n = I_{total} = Cons\tan t \tag{4}$$

where I_{total} is the drain current of the transistor M_5.

The g_{mt} control of the input stage is performed by means of the current switch MSW and one-times current mirror M_8-M_9. When the $V_{i,\,cm}$ is near to V_{ss}, gate-source voltage of the current switch MSW, VSW, is positive and this transistor is off. As a result, the entire drain current of M_5, I_{total} flows to the pMOS pair. When the $V_{i,\,cm}$ rises, VSW decreases and when it becomes negative, the MSW starts to conduct. If the $V_{i,\,cm}$ increases continuous, the transistor MSW conducts half of I_{total} at a certain point. Its current becomes more and more, until it be equalled to I_{total} and mirrored via the current mirror M_8-M_9, to the source node of the nMOS pair and hence pMOS pair is completely turned off. Part of I_{total} directs to pMOS pair when the amount of $V_{i,\,cm}$ is around the middle range of the supply voltage and the rest of it flows to MSW. Then it is guided to the nMOS pair via current mirror M_8-M_9. Consequently, sum of the tail currents of the pMOS and nMOS pairs is kept equal to I_{total}. The turning point (I_p=I_n) is determined by the VSW voltage. For the nMOS and pMOS pairs with the same threshold voltage, the VSW voltage must be exactly half of the power supply voltage. If the weak inversion slop factor, n, is different for the nMOS and pMOS pair, the g_m will change over the entire common mode voltage range. This problem can be entirely solved by correcting the gain factor of the current mirror M_8-M_9. When the current switch MSW guides the current I_{total} from the pMOS to nMOS pair gradually, the offset of the input stage will change and lead to degradation of the Common Mode Rejection Ratio (CMRR).

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In order to overcome the above problem, the offset change must be distributed over the common mode input range. This requires that the W/L ratio of the current switch MSW be small in compare with the input pairs M_1-M_4.

The g_m controlled by mentioned way offers small die area and low power dissipation, besides a constant g_m operation. Because, the current switch MSW and the current mirror M_8-M_9 are small in compare with the input stage transistors. Also, this method has not effect on noise of the input stage. This is due to the produced noise in the g_m control circuit, is incorporated with the tail currents of the complement input pairs. Hence, it behaves as a common-mode signal. As the result, the generated noise of the g_m control can be neglected, assuming that the input pairs M_1-M_4 are matched.

Fig. 2 shows the normalized g_{mt} curve versus to $V_{i, cm}$.

B. Output Stage

In order to achieve the rail-to-rail output voltage range the output transistors M_{28}-M_{29}, must be in the common-source configuration. Due to efficient use of the power supply, they should be biased in class AB. Also, the class-AB control must be compact in order to better use of die area [4], [6].

In Fig. 1, the feedforward class-AB control is performed by M_{15} and M_{17}. These transistors are biased by two in-phase signal currents from cascodes M_{13} and M_{19} and their gate-voltages are maintained at a constant value by the stacked diode-connected transistors (M_{25}-M_{26} and M_{23}-M_{24}). In the output stage of the reported circuit in [6], the class-AB control, and the quiescent current in the output transistors are sensitive to supply voltage changes. Here, we use of the floating current source to obtain the insensitive quiescent current to supply voltage variations. The floating current source (M_{14} and M_{16}) has the same architecture as the feedforward class-AB control, and hence the power supply voltage dependency of the class-AB driver, is automatically compensate. The transistors, M_{10}, M_{14}, M_{25}, M_{26} and M_{16}, M_{20}, M_{23}, M_{24} create two translinear loops that determine the value of the floating current source.

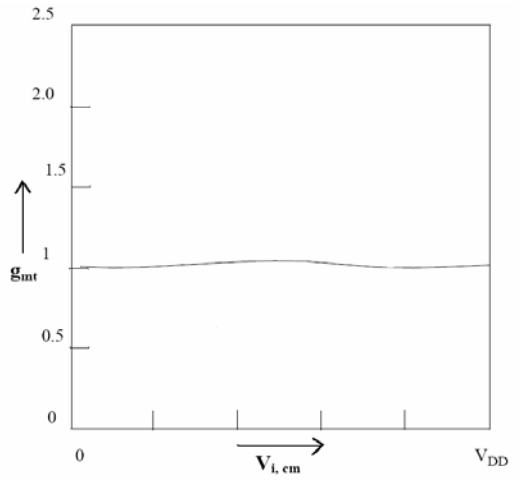

Figure 2. The normalized g_{mt} curve versus to $V_{i, cm}$

C. Frequency Compensation

Frequency compensation is needed due to provide stability in the Two- stage opamps. For a special value of power consumption, each of compensation techniques presents a trade-off between the bandwidth and stability [12].

In this implementation, frequency compensation is performed by the cascoded Miller which compared to classical Miller compensation, have some advantages. Firstly, it is well known that, the two-stage opamp gain can be improved by using of the cascode architectures. If applied cascode is placed in the Miller loop, non-dominant pole is shifted to higher frequency and this, results in a larger unity-gain frequency. Hence, for the same value of bandwidth, the amplifier with cascoded-Miller compensation can offer higher Power Signal Rejection Ratio (PSRR) and lower power consumption. Also, in [4] is shown that the opamp with this compensation responds to small and large signals, faster than classical Miller compensation, and gives a better slew-rate. However, a weak point of this compensation is that the amplifier peaks at high output currents and the worst case situation takes place for a load capacitor that is equal with the Miller capacitor.

Since in this paper, power consumption is a key factor, therefore the cascoded Miller is used.

In Fig. 1, cascoded Miller compensation is performed by connecting the Miller capacitors to the source of the cascode transistors, M_{13} and M_{19}, instead of connecting to the gate of the output transistors.

III. DESIGN PARAMETERS

The aspect ratios of the transistors in Fig. 1, as well as the value of capacitors CM_1 and CM_2 are given in Table I. The g_m control operation with low power supply voltage is obtained through designing all transistors with large aspect ratios operating in weak inversion except the current sources.

Transistor M_5 always operates in saturation region, and never in linear region, through properly selecting the gate-voltage VSW of MSW.

IV. SIMULATION RESULTS

The opamp is simulated with TSMC 0.18 μm CMOS technology. The threshold voltages of nMOS and pMOS transistors are in the range of 0.4 V. The supply voltage V_{DD} is 0.8 V. The load is a 13 pF capacitor in parallel to 108 kΩ resistor. Fig. 2 shows the normalized g_{mt} curve versus to $V_{i, Cm}$. The simulated g_{mt} variation is 6.4%. Fig. 3 Shows the frequency response of the opamp. The DC gain is 78 dB, unity-gain bandwidth is 1.7 MHz, and phase margin is 68°. The simulation results are presented in Table II.

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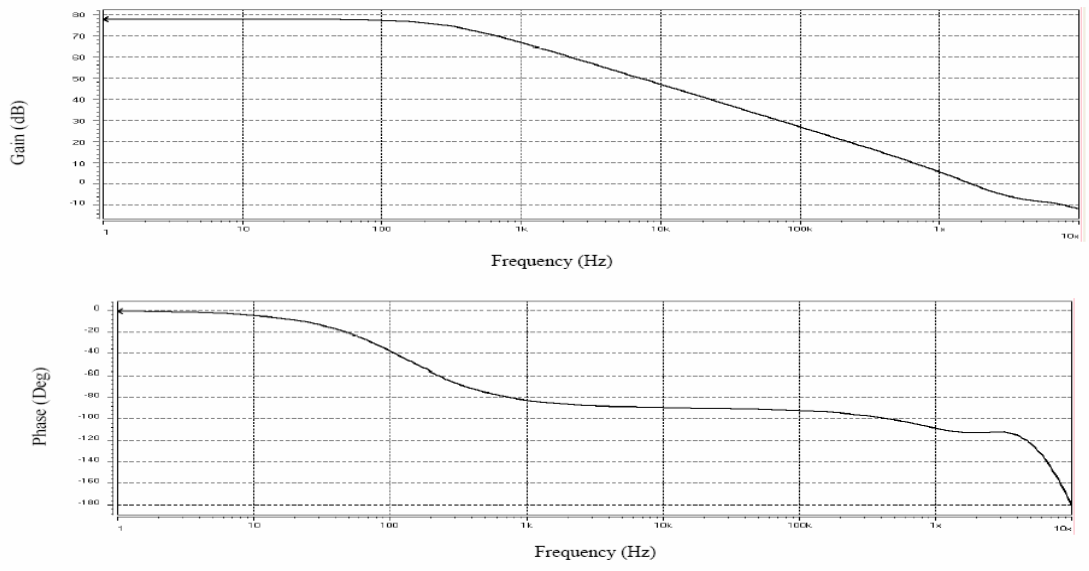

Fig. 3. Frequency response of the proposed operational amplifier

TABLE I
COMPONENT VALUES

Components	W(μm) / L(μm)
M_1, M_2	60/0.4
M_3, M_4	150/0.4
M_5, M_{10}, M_{11}, MSW	22.5/5
M_6, M_{22}	6.25/5
M_7, M_{27}	2.5/5
M_8, M_9, M_{20}, M_{21}	9/5
M_{12}, M_{13}	30/0.4
M_{14}, M_{15}, M_{26}	90/0.2
M_{16}, M_{17}, M_{23}	36/0.2
M_{18}, M_{19}	12/0.4
M_{24}	6/0.2
M_{25}	15/0.2
M_{28}	180/0.2
M_{29}	72/0.2
CM_1, CM_2	1.16pF

TABLE II
SUMMARY OF AMPLIFIER PERFORMANCE

Parameters	Values
Process	0.18 μm
Supply Voltage	0.8 V
g_m Variation	6.4%
Power	10 μw
Bandwidth	1.7 MHZ
Phase margin	68°
Dc gain	78 dB
Input Rang	Rail-to-Rail
Output Rang With (1kΩ load)	Rail-to-Rail
Slew Rate	0.8 V/μS

V. CONCLUSION

This paper has presented a new design strategy for a constant-g_m rail-to-rail low power operational amplifier. In the proposed circuit, power consumption is reduced by biasing the transistors in weak inversion and using of the cascoded Miller compensation. The constant-g_m operation is achieved using one-times current mirror that has a constant transconductance only when input stage pairs are biased in weak inversion. The simulation results have been provided.

REFERENCES

[1] S. Yan, J. Hu, T. Song and E. Sanchez-Sinencio, "A Constant-g_m Rail-to-Rail Op Amp Input Stage Using Dynamic Current Scaling Technique," in *Proc. 2005 IEEE International Symposium on Circuits and Systems Conf*, Kobe, Japan, pp. 2567-2570.

[2] C. J. B. FAYOMI, M. SAWAN and G. W. ROBERTS, "A Design Strategy for a 1-V Rail-to-Rail Input / Output CMOS Opamp," in *Proc. 2001 IEEE International Symposium on Circuits and Systems Conf*, pp. 639-642.

[3] M. peng, M. M. Hossain, W. A. Davis, H. T. Russell Jr and R. L. Carter, "A 1-V Quasi Rail-to-Rail Operational Amplifier with a Single Input Differential Pair," in *proc. 2007 IEEE Region 5 Technical Conf*, Fayetteville, AR, pp. 93-96.

[4] R. Hogervorst, J. P.Tero, R. G. H. Eschauzier, and J. H. Huijsing, "A Compact Power-Efficient 3 V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp. 1505-1513, Dec. 1994.

[5] G. Ferri and W. Sansen, "A Rail-to-Rail Constant-g_m Low-Voltage CMOS Operational Transconductance Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 10, pp. 1563-1567, Oct. 1997.

[6] J. Citakovic, I. R. Nielsen, J. H. Nielsen, P. Asbeck and P. Andreani "A 0.8V, 7μA, Rail-to-Rail Input/Output, Constant G_M Operational Amplifier in Standard Digital 0.18μm CMOS," in *proc. 2005 IEEE 23rd NORCHIP Conf*, pp. 54-57.

[7] J. H. Huijsing and D. Linebarger, "Low-Voltage Operational Amplifier with Rail-to-Rail Input and Output Ranges," *IEEE Journal of Solid-State Circuits*, vol. sc-20, no. 6, pp. 1144-1150, Dec. 1985.

[8] S. Sakurai and M. Ismail, "Robust Design of Rail-to-Rail CMOS Operational Amplifiers for a Low Power Supply Voltage," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 2, pp. 146-156, Feb. 1996.

[9] J. F. Duque-Carrillo, R. Perez-Aloe, and J. M. Valverde, "Constant-Gm Rail-to-Rail Common-Mode Range Input Stage With Minimum CMRR Degradation," *IEEE Journal of Solid- State Circuits*, vol. 28, no. 6, pp. 661-667, June. 1993.

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ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

[10] J. H. Huijsing, R. Hogervorst and K. de Langen, " Low-power low-voltage VLSI operational amplifier cells," *IEEE Trans. Circuits and Systems-I: Fundamental Theory and Applications*, vol. 42, no. 11, pp. 841-852, Nov. 1995.
[11] R. Hogervorst, J. H. Huijsing, *Design of low-voltage, low-power operational amplifier cells*, Kluwer Academic Publishers, 1996.
[12] H. Aminzadeh and K. Mafinezhad, "On the Power Efficiency of Cascode Compensation over Miller Compensation in Two-Stage Operational Amplifiers," in *proc. ISLPED'08*, Bangalore, India, 2008, pp. 283-287.

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