Addressing Method for the Components of On-Chip Communication

Prabhat K. Sharma, Rakesh Bairathi

***Abstract*—In this paper we propose a hierarchical addressing scheme for Network-on-Chip applications. This scheme will facilitate a user to transmit a lesser number of overhead bits while transmitting a message to some other user. The number of overhead bits required will be dependent on the distance (in terms of number of routing nodes or routers) from source IP to destination IP. We also define a channel utility factor and show how the overall utilization of the channel increases with this scheme.**

***Index Terms*—Channel capacity, IP, Network-on-Chip, System-on-Chip, Table-lookup routing, virtual channels, wormhole routing.**

I. Introduction

The bus based communication model remains convenient for present days SoCs that integrates around five processors and rarely, more than ten bus masters [1]. However, to achieve a required throughput, a monolithic shared bus is often inefficient because of scalability problems [2] and high capacitive load driving and higher frequency requirements [3]. Borrowing the concept from computer networks, [1] proposes a three layer protocol stack model for on chip networks. Network on chip should be treated as prominent concept of communication in SoCs. NoC does not constitute an explicit new architecture for intrachip communication but is rather a concept which presents a unification of on-chip communication solutions [4].

Fig. 1 shows the pictorial representation of a 4X4 NoC. A Network adapter is an interface between an IP and a router. Routing node represents a router and link is the physical channel for communication between two routers. These routers are generally wormhole routers, which employ virtual channel for the flow control. Network throughput can be increased by dividing the buffer storage associated with each physical channel into several virtual channels [5]. Authors in [6] proposed a virtual channel flow control mechanism for wormhole routers.

A SoC can be viewed as a micro-network of components and NoC as an abstraction of communication among the components. Except some distinctive characteristics, such as timing and energy constraints, the models, techniques and tools from the computer network design field can also be applied to Network on Chip. High Speed of communication or greater rate of flow of information, over the link, in between the NoC components is obviously a desired requirement for on chip communication. This paper is organized in the following way: section II describes the addressing methods which are being used in computer networks. Section III explores the proposed scheme for NoC applications and section IV explains channel utility factor and the effect of proposed scheme on the overall channel utilization. Finally, section V concludes the paper and elaborates the future aspects.

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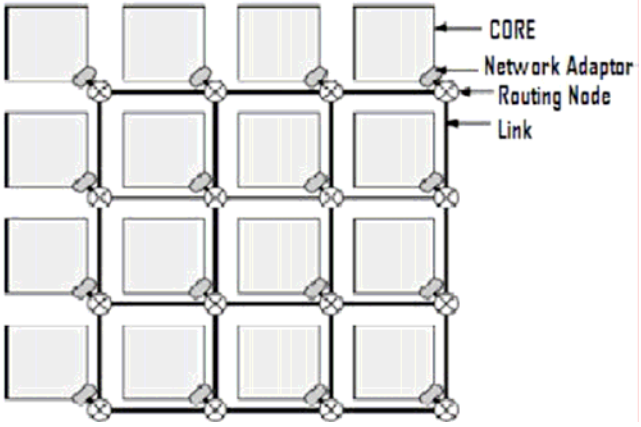

Fig. 1 A 4X4 Mesh NoC Structure

II. Addressing in Computer Networks

Message is transmitted in form of packets or frames over the network link. Each packet, then, individually has to travel over the transmission link following some routing directives. Hence each packet or frame carries routing and addressing information along with the message bits. For Examples, in a LAN an Ethernet packet/frame has the structure given in Fig. 2 [7].Being generalized, every packet in computer network (whether it belongs to any set of protocols), belongs to any pair of source and destination some overhead (including SA, DA and other pre-info and post-info bits). Suppose a message of N bits which is broken into p packets. The number of bits in a packet can be given by $N_m = N/p$ bits. When these N_m bits are transmitted over the link some addressing information N_a and overhead N_o must be added to it. This overhead includes the bits for synchronization, SOF (start of frame), EOF (End of frame) and other fields' information in it. Now the packet that has to travel over the link consists of $Np = N_a + N_o + N_m$ bits. The number of bits Na and No generally remain constant for a given set of rules or protocols. So, every time, when a

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packet is transmitted it carries some constant overhead additional to information bits.

III. Hierarchical Addressing scheme (HAS)

Every IP connected to routers in NoC (mesh topology) is assigned a global address in such a way that the global addresses of two directly connected IPs must have only single bit difference (Fig. 3). It means the number of bit changes in the global addresses of two IPs will indicate the distance between them. For a NoC with mesh topology, the number of routers between two IPs situated at d distance to each other can be given by (d+1). It is obvious that this number of routers will be same for the possible shortest path exist for the given source destination pair in a mesh topology. If b number of bits required to resolve the internal port addresses of a single router, then to address the complete path travelling address will contain TA = (n X b) = (d+1).b bits.

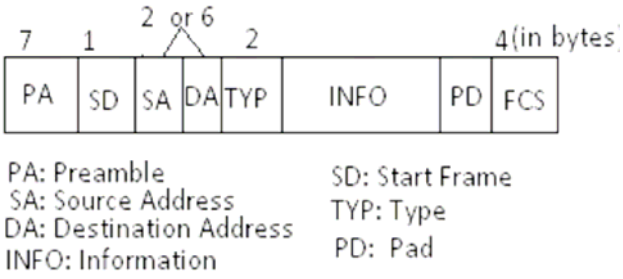

Fig. 2 Ethernet Frame

When an IP sends the packet to its router, every packet by IP to its router consists of global address of source and destination and the information bits. At routing node global addresses of source and destination are extracted out from the packet and the distance between given source and destination can be found out. Now router will assign a travelling address from its lookup table for the given source and destination pair. Now, in case of wormhole routing header fill consist of only TA not the global addresses of source and destination. Here as the simplest case the flit size is supposed to be equal to a packet size. At destination port, destination router will find the global address of the source IP by reversely traversing the travelling address in its lookup table. By doing so we are transmitting more number of message information in a packet.

Flow chart in Fig. 4 elaborates the mechanism that takes place at a routing node when a packet from its IP arrives to it. It is clear from Fig. 1 that only one IP is directly connected to a routing node (via network adapter).

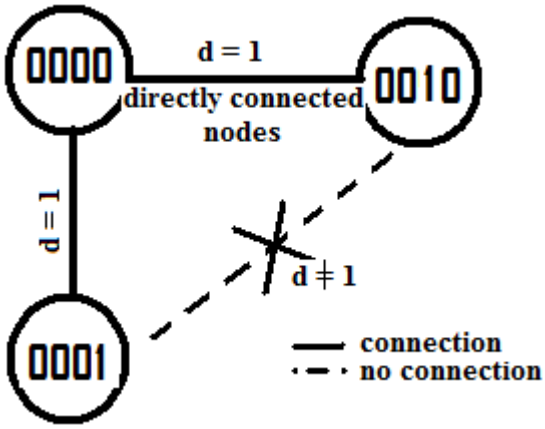

Fig. 3 Global Address assignment

IV. Channel utilization

We define a channel utility factor which measures the amount of true information transferred over the link of capacity C bits/sec.

$$U_{ch} = N_m / N_p; \quad \text{where } 0<U_{ch}<1.$$
$$= [N_p + (N_a + N_o)] / N_p$$
$$= 1 + (N_a + N_o) / N_p$$

For a fix Na and N_o, U_{ch} will remain constant. But if N_a is replaced by travelling address TA

$$Uch = 1 + (TA + N_o) / N_p$$
$$= 1 + ((d+1).b + N_o) / N_p$$

Now, utilized channel capacity (which indicates flow of true information over the channel of capacity C bits/sec)

$$C^u = U_{ch.} C$$

For Np = 64 bits and d ranges 1 to 6, various curves as Uch versus distance, total overhead bits (Na +No) versus distance and Nm versus Uch are plotted in Fig. 5, Fig. 6 and Fig. 7 respectively.

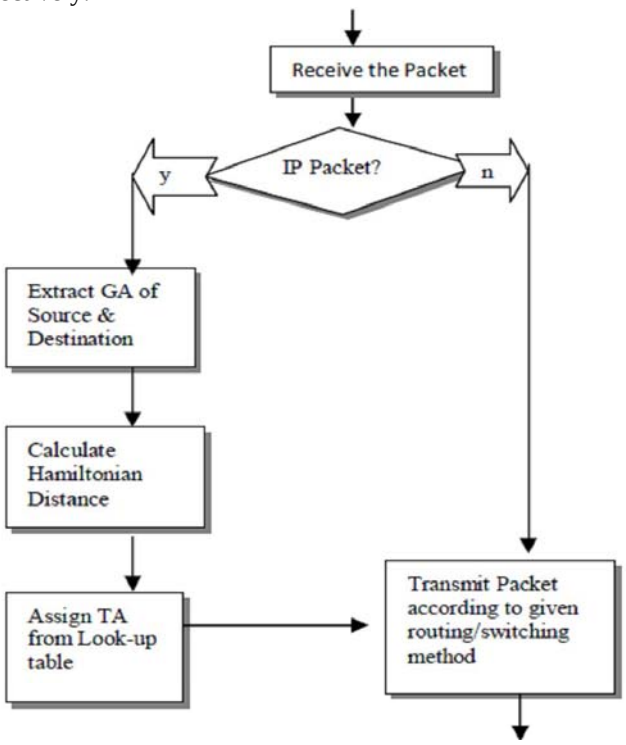

Fig. 3 Basic mechanism of HAS

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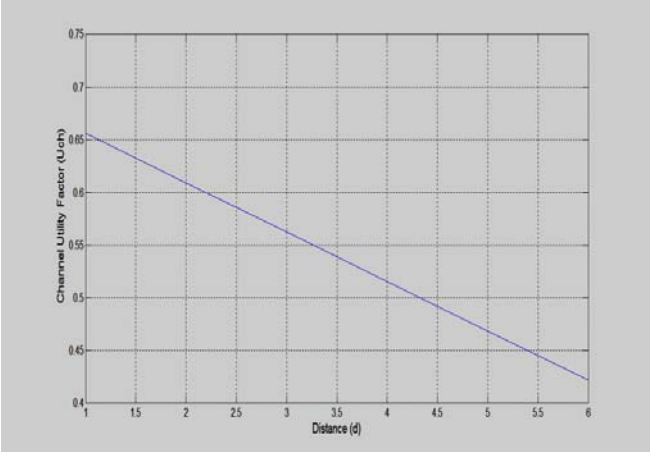

Fig. 5 U_{ch} Vs Distance

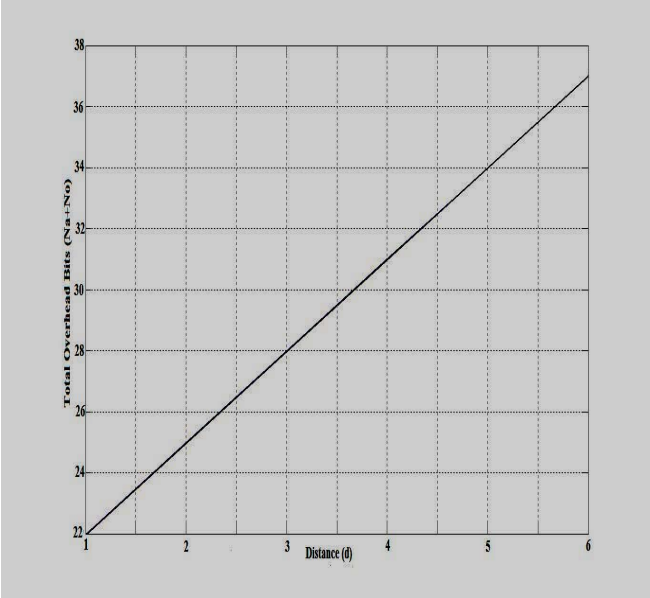

Fig. 6 U_{ch} Vs Distance

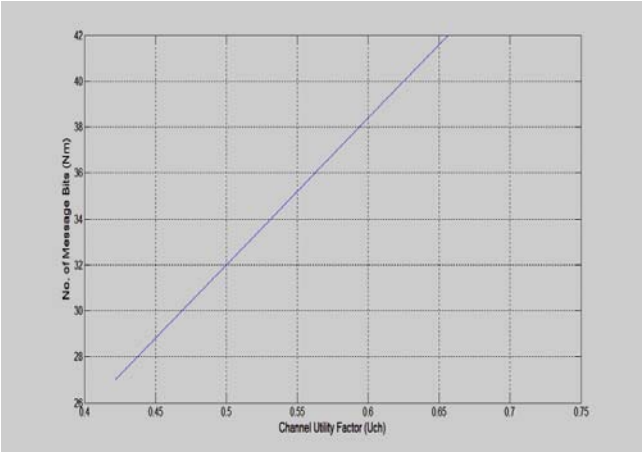

Fig. 7 No. of message bits Vs U_{ch}

V. Conclusion

The obvious requirement for the proposed scheme is to place a look up table at each node. But such an implementation is not practical because the size of lookup table places an artificial upper bound on the network size. Also the large table is inefficient in the use of chip area. This scheme provides better channel utilization by sending larger number of message bits in a lesser time for the available resources. As this scheme always provide a shortest path on the basis of bit change in the global addresses of source and destination, an obviously required flexibility can be introduced in the case when there is any congested link appears in between the assigned travelling path. Furthermore the size of lookup table can be reduced to alleviate larger buffer size and chip area constraints.

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