All-Grounded Passive Element Voltage-Mode Universal Filter Using Single DDCCTA

Orapin Channumsin, Tattaya Pukkalanun and Worapong Tangsrirat, *Member, IAENG*

***Abstract*— In this paper, a novel single-input three-output (SITO) second-order multifunction active voltage filter with high-input impedance is proposed. The proposed circuit employs one differential difference current conveyor transconductance amplifier (DDCCTA) as active element together with one grounded resistor and two grounded capacitors as passive elements. The circuit offers the following attractive features : (i) the simultaneous realization of lowpass, bandpass and highpass responses from the same topology, (ii) no requirements for component matching conditions, (iii) electronic controllability of important filter parameters, (iv) simpler structure due to contains only one DDCCTA and three passive elements, and (v) low sensitivity performance. To confirm the theoretical analysis, PSPICE simulation results are included using 0.5 μm MIETEC CMOS technology parameters.**

***Index Terms*— Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA), voltage-mode circuit,**

I. Introduction

RECENTLY, a relatively new active building block, the so-called differential voltage current conveyor transconductance amplifier (DVCCTA), was introduced [1]. The DVCCTA device is obtained by cascading of the differential voltage current conveyor (DVCC) with the transconductance amplifier (TA) in monolithic chip for compact implementation of analog function circuits [1]-[3]. Thereafter several different applications of the DVCCTA have been presented in the technical literature, particularly from the area of frequency filters [3]-[5]. Among these, the authors in [3] proposed the voltage-mode biquadratic filter configuration with high-input impedance using one DVCCTA and two grounded capacitors. However, only two standard filter functions (i.e. LP and BP) can be obtained simultaneously. All the recently published universal voltage-mode filters in [4]-[5] employ two floating capacitors, and require critical matching component constraints for each filter response. In addition, these two proposed configurations also do not posses high input impedance.

In this paper, a voltage-mode biquadraric universal filter with one high input impedance and three output terminals based on the differential difference current conveyor transconductance amplifier (DDCCTA) is presented. The DDCCTA can easily be implemented from a DVCCTA by adding the Y3 terminal. Contrary to the previously reported single active element-based voltage-mode filters [3]-[10], the proposed circuit offers the following advantageous features :

(i) It uses a single DDCCTA, one grounded resistor and two grounded capacitors, which are the minimum components necessary for realizing a biquadratic filtering function from the same topology. From the point view of the advantages of simplicity, cost reduction, power consumption and space saving, it is important to implement active voltage biquad filters using a minimum number of active and passive elements [11].

(ii) All passive elements are grounded, which is advantageous in the reduction of parasitic impedance effects as well as in easy integrated circuit implementation [12]-[13].

(iii) It can simultaneously realize LP, BP and HP responses from the same topology.

(iv) It does not require component matching conditions.

(v) It has high-input impedance, which can be directly connected in cascade to realize high-order filters [14].

(vi) The natural angular frequency (ω_0) and the quality factor (Q) are electronically controllable through the transconductance parameter (g_m) of the DDCCTA.

(vii) It has low sensitivity performance.

II. Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA)

The DDCCTA element is based on the use of the DDCC as an input stage and the TA as an output stage. As shown in Fig.1, the port characteristics of the DDCCTA can be described by the following expressions :

$$I_{Y1} = I_{Y2} = I_{Y3} = 0,\ V_X = V_{Y1} - V_{Y2} + V_{Y3},\ I_Z = I_X,\ I_O = g_m V_Z \tag{1}$$

where g_m is the transconductance parameter of the DDCCTA.

The internal structure of the DDCCTA in CMOS technology is shown in Fig.2. The scheme is based on the internal circuit of the DDCC [15], which is followed by a TA [16]. In this case, the transconductance gain (g_m) of the DDCCTA can be given by :

$$g_m = \sqrt{\mu C_{ox} \frac{W}{L} I_B} \tag{2}$$

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O. Channumsin, T. Pukkalanun and W. Tangsrirat are with the Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Chalongkrung road, Ladkrabang, Bangkok 10520, Thailand (phone: +662-326-4205; fax: +662-326-4205; e-mail: pinmut@hotmail.com, tattap@yahoo.com, drworapong@yahoo.com).

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where I_B is an external DC bias current, μ is the effective channel mobility, C_{ox} is the gate-oxide capacitance per unit area, W and L are channel width and length, respectively. It should be noted that the g_m-value of the DDCCTA can be adjustable electronically by I_B.

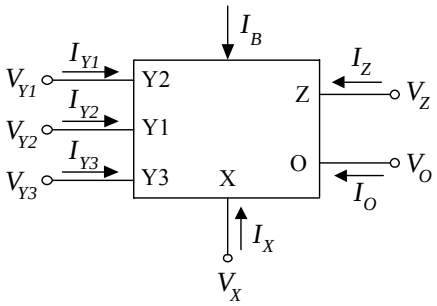

Fig. 1 Electrical symbol of the DDCCTA.

III. Proposed Filter Configuration

Using a single DDCCTA and a canonical number of passive elements (one resistor and two capacitors), the voltage-mode universal filter with one input terminal and three output terminals can be obtained as shown in Fig.3. It can be seen that the input of the proposed filter is applied to the Y_1 terminal of the DDCCTA. Therefore, the circuit has the advantage of high-input impedance. Since all the passive components are grounded, it is therefore suitable for integrated circuit implementation point of view. By routine circuit analysis using equation (1), the voltage transfer functions of the proposed filter in Fig.3 can be given by :

$$HP(s) = \frac{V_{o1}(s)}{V_{in}(s)} = \frac{s^2}{D(s)} \tag{3}$$

$$LP(s) = \frac{V_{o2}(s)}{V_{in}(s)} = \frac{\left(-\frac{g_m}{R_1C_1C_2}\right)}{D(s)} \tag{4}$$

and

$$BP(s) = \frac{V_{o3}(s)}{V_{in}(s)} = \frac{\left(\frac{s}{R_1C_1}\right)}{D(s)} \tag{5}$$

where

$$D(s) = s^2 + \left(\frac{s}{R_1C_1}\right) + \left(\frac{g_m}{R_1C_1C_2}\right) \tag{6}$$

From above expressions, the HP, LP and BP responses are available at the node voltages v_{o1}, v_{o2} and v_{o3}, respectively. Also note that there is no need of any component-matching constraints for all filter response realizations.

Also, from equations (3)-(6), the natural angular frequency (ω_0), bandwidth (BW) and quality factor (Q) of the proposed filter can be found as :

$$\omega_0 = \sqrt{\frac{g_m}{R_1C_1C_2}} \tag{7}$$

$$BW = \frac{1}{R_1C_1} \tag{8}$$

and

$$Q = \sqrt{\frac{g_mR_1C_1}{C_2}} \tag{9}$$

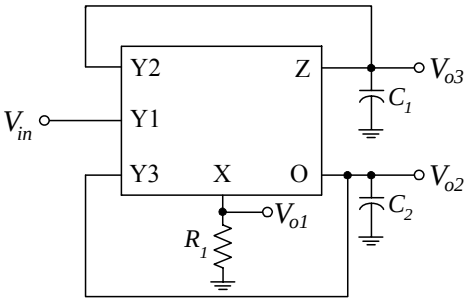

Fig.3 : Proposed single DDCCTA voltage biquad.

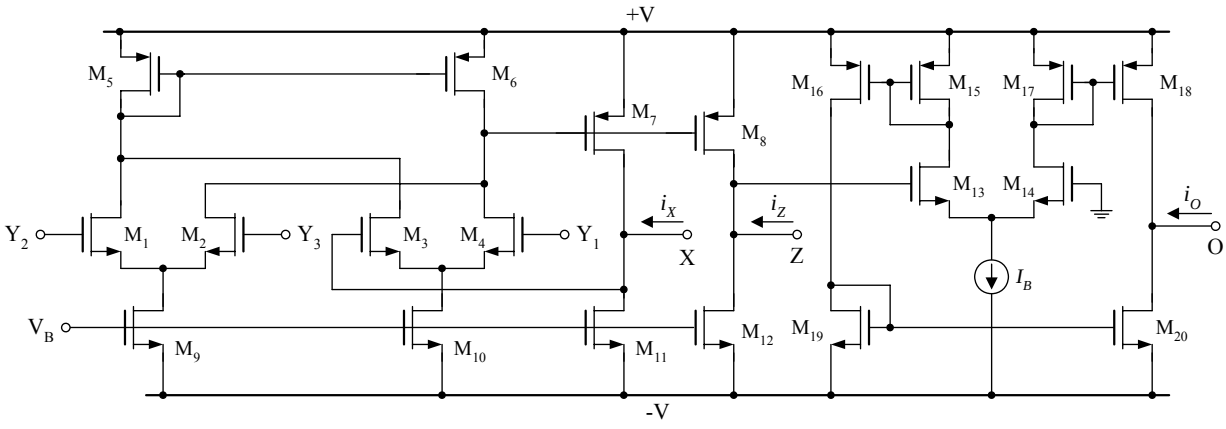

Fig.2 : CMOS implementation of the DDCCTA.

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Equations (7)-(9) show that the parameters ω_0 and Q for all the filter responses can electronically be tuned by varying g_m. For the fix-valued capacitors, the ω_0 can be adjusted arbitrarily without disturbing Q by simultaneously changing g_m and R_1 and keeping the product g_mR_1 constant. On the other hand, the parameter Q can be tuned without disturbing ω_0 by simultaneously increasing g_m and R_1 and keeping g_m/R_1 constant.

IV. Non-ideality Effects

Taking into consideration the DDCCTA non-idealities, the port characteristics in equation (1) can be rewritten as :

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2} + \beta_3 V_{Y3},\ I_Z = \alpha I_X,\ I_O = g_m V_Z \quad (10)$$

where and $\beta_k = 1 - \varepsilon_{vk}$ for k =1, 2, 3 and $\alpha = 1 - \varepsilon_i$. Here, ε_{vk} ($|\varepsilon_{vk}| << 1$) and ε_i ($|\varepsilon_i| << 1$) represent the voltage and current tracking errors of the DDCCTA, respectively. Thus, re-analysis of the proposed circuit in Fig.3 yields the non-ideal parameters as follows :

$$\omega_0 = \sqrt{\frac{\beta_3 \alpha g_m}{R_1 C_1 C_2}} \quad (11)$$

$$BW = \frac{\beta_2 \alpha}{R_1 C_1} \quad (12)$$

and

$$Q = \frac{1}{\beta_2}\sqrt{\frac{\beta_3 g_m R_1 C_1}{\alpha C_2}} \quad (13)$$

The sensitivity analysis shows that :

$$S_{g_m}^{\omega_0} = S_{\beta_3}^{\omega_0} = S_{\alpha}^{\omega_0} = -S_{R_1}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = \frac{1}{2} \quad (14)$$

$$S_{\beta_2}^{BW} = S_{\alpha}^{BW} = -S_{R_1}^{BW} = -S_{C_1}^{BW} = -S_{\beta_2}^{Q} = 1 \quad (15)$$

$$S_{g_m}^{Q} = S_{\beta_3}^{Q} = -S_{\alpha}^{Q} = S_{R_1}^{Q} = S_{C_1}^{Q} = -S_{C_2}^{Q} = \frac{1}{2} \quad (16)$$

$$S_{\beta_1}^{\omega_0} = S_{\beta_2}^{\omega_0} = S_{g_m}^{BW} = S_{\beta_1}^{BW} = S_{\beta_3}^{BW} = S_{C_2}^{BW} = S_{\beta_1}^{Q} = 0 \quad (17)$$

Clearly, all the active and passive sensitivities are within unity in magnitude.

V. Simulation Results

To verify theoretical analysis, the proposed single DDCCTA-based voltage-mode universal filter of Fig.3 has been simulated with PSPICE program using MIETEC 0.5 μm CMOS technology process parameters. The DDCCTA was performed by the CMOS structure given in Fig.2 with supply voltages of +V = -V = 3 V, and V_B = -1.22 V. The aspect ratios of CMOS transistors are given in Table 1.

Table 1 Transistor aspect ratios of the DDCCTA circuit shown in Fig.2.

Transistors	W (μm)	L (μm)
M_1 - M_4	1.8	0.7
M_5 - M_6	5.2	0.7
M_7 – M_{10}	20	0.7
M_{11} – M_{12}	58	0.7
M_{13} – M_{20}	4	1.0

The filter is designed to realize LP, BP and HP responses with $f_0 \cong \omega_0/2\pi$ = 1.6 MHz and Q = 1. For this purpose, the active and passive components are chosen as : $g_m \cong$ 101.44 μA/V (I_B = 16.5 μA), R_1 = 10 kΩ and $C_1 = C_2$ = 10 pF. The simulated responses comparing with the theoretical values are shown in Fig.4. From the results, it can be observed that the simulation results agree very well with theoretical predictions.

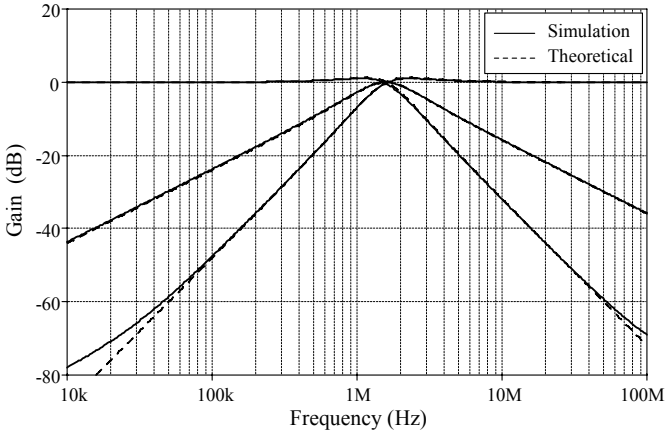

Fig.4 : Simulated frequency responses of LP, BP and HP for the proposed biquad in Fig.3.

In order to investigate a time-domain response of the proposed voltage-mode universal filter, a 1.6 MHz sinusoidal input voltage with 200 mV peak is applied to the filter. The results obtained are shown in Fig.5. It can be measured from simulations that in case of BP response the total harmonic distortion (THD) of about 0.38% and the total power consumption of about 0.83 mW are obtained.

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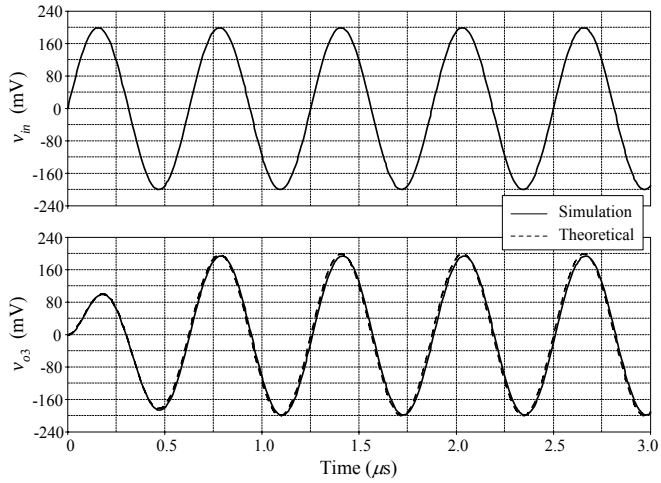

Fig.5 : Input and output waveforms of the BP responses for a 1.6-MHz sinusoidal input voltage of 200 mV (peak).

VI. Conclusion

A single-input three-output voltage-mode universal filter for simultaneously realize LP, BP and HP responses without changing the configuration and requiring extra active component has been presented. The presented circuit uses one DDCCTA, one grounded resistor and two grounded capacitors, which is a canonical structure and suitable for integration. It has high-input impedance, and exhibits electronic controllability of both ω_0 and Q through the bias current of the DDCCTA. Also, no critical component matching conditions are required. Both its active and passive sensitivities are low.

References

[1] A. Jantakun, N. Pisutthipong, and M. Siripruchyanun, "A synthesis of temperature insensitive/electronically controllable floating simulators based on DV-CCTAs", *Proceedings of ECTI-CON 2009*, *Pattaya*, *Thailand*, pp. 560-563, 2009.

[2] A. Lahiri, W. Jaikla and M. Siripruchyanun, "Voltage-mode quadrature sinusoidal oscillator with current tunable properties", *Analog Integr. Circ. Sig. Process.*, vol.65, no.2, pp.321-325, 2010.

[3] W. Jaikla, M. Siripruchyanun and A. Lahiri, "Resistorless dual-mode quadrature sinusoidal oscillator using a single active building block", *Microelectron. J.*, vol.42, no.1, pp.135-140, 2011.

[4] N. Pandey and S. K. Paul, "Analog filters based on 0.25 μm CMOS differential voltage current conveyor transconductance amplifier (DVCCTA)", *Proceedings of India Int. Conf. Power Electron. (IICPE 2010)*, *New Delhi*, *India*, pp.1-5, 2010.

[5] N. Pandey and S. K. Paul, "VM and CM Universal Filters Based on Single DVCCTA", *Active and Passive Electronic Components*, vol.2011, Article ID 929507, 7 Pages, 2011.

[6] M. A. Ibrahim, H. Kuntman and O. Cicekoglu, "Single DDCC biquads with high input impedance and minimum number of passive elements", *Analog Integr. Circ. Sig. Process.*, vol.43, pp.71-79, 2005.

[7] S. Maheshwari, "High performance voltage-mode multifunction filter with minimum component count", *WSEAS Trans. Electronics*, vol.5, pp.244-249, 2008.

[8] Y. Z. Liao, H. P. Chen and W. T. Lee, "Versatile universal voltage-mode filter employing minimum components", *IEICE Electronics Express*, vol.6, no.17, pp.1246-1252, 2009.

[9] E. Yuce, "Voltage-mode multifunction filters employing a single DVCC and grounded capacitors", *IEEE Trans. Instrum. Meas.*, vol.58, no.7, pp. 2216-2221, 2009.

[10] H. P. Chen and T. Y. Hsieh, "Voltage-mode highpass, bandpass and lowpass filters using a single DVCC", *Proceedings of Progress in Electromagnetics Research Symposium*, *Xi'an*, *China*, pp. 517-520, 2010.

[11] A. U. Keskin, "Multi-function biquad using single CDBA", *Electrical Engineering*, vol.88, pp.353-356, 2006.

[12] M. Bhusan, and R. W. Newcomb, "Grounding of capacitors in integrated circuits", *Electron. Lett.*, vol.3, pp.148-149, 1967.

[13] R. Senani and V. K. Singh, "KHN-equivalent biquad using current conveyors", *Electron. Lett.*, vol.31, pp.626-628, 1995.

[14] J. W. Horng, "High input impedance voltage-mode universal biquadratic filter with three inputs using DDCCs, *Circuits Syst. Signal Process.*, vol.27, no.4, pp.553-562, 2008.

[15] W. Chiu, S. I. Liu, H. W. Tsao and J. J. Chen, "CMOS differential difference current conveyors and their applications", *IEE Proc. Circuits Devices Syst.*, vol.143, no.2, pp.91-96, 1996.

[16] D. R. Bhaskar, A. K. Singh, R. K. Sharma, and R. Senani, "New OTA-C universal current-mode/trans-admittance biquads", *IEICE Electronics Express*, vol.2, pp.8-13, 2005.

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