Pulsewidth Control Loop with Low Control Voltage Ripple

Shao-Ku Kao, and Yong-De You

Abstract—**A pulsewidth control loop (PWCL) with low control voltage ripple is proposed in this paper. The charge pump circuit with charge sharing circuit decreases the ripple of control voltage. By decreasing the control voltage ripple for reducing the stability problem of the loop. The jitter of the output clock is reduced due to the low control voltage ripple. It is demonstrated by simulation results in a 0.18μm CMOS process. The simulation shows that the frequency range of input signal is from 100MHz to 1GHz, the duty cycle range of the input signal is from 40% to 60%. The proposed circuit can reduce the output clock jitters by 37.7% and 50.6% for the 1GHz and 100MHz,respectively.**

Index Terms—**pulsewidth control loops (PWCL), duty cycle corrector (DCC), fast locking, low jitter, lock detector.**

I. Introduction

In order to meet the high speed circuit, the system clock plays an important role in today CMOS VLSI circuit. Normally, the system clock is connected by the clock driver and buffers to distribute clock over the entire chip. However, the duty cycle of clock signal due to the inverter chain is difficult to fix a 50%. Many systems adopt accurate duty cycle at 50% when clock signal passes through clock driver and buffer. Such as double sampling analog-digital converter (ADC) and DDR SDRAM, both edge of clock are required to sample the input data that duty cycle must be maintained at 50%, else the circuit generates a error.

Convention pulsewidth control loop (PWCL) [1] consists of control stage, buffer stage, ring oscillator, charge pump, differential pair comparator. If ring oscillator experiences power, voltage and temperature (PVT) variation may cause the duty cycle of output not 50%, leading to a possibly unstable operation. In mutual-correlated PWCL [3] used input signal to generate complementary output signal to overcome PVT and reduce output clock jitter. However, mutual-correlated PWCL has narrow operating frequency range. Fast-locking PWCL [4] can reduce locking time of PWCL and preset output duty cycle. Fast-locking PWCL may cost large silicon area and power consumption. The high linearity PWCL [6] can achieve wide frequency range and reduce locking time. But, the high linearity PWCL needs a long reset time to detect the frequency and duty cycle before enter the normal tracking operation.

In the view of the above PWCL, the proposed circuit uses the charge sharing theorem [7] to reduce ripple of charge pump output voltage. The jitter of differential pair amplifier output voltage is suppressed by low ripple output voltage of charge pump. The proposed circuit reduces the jitter of output clock with wide operation frequency range. It tolerates an input duty cycle of 40%~60% for input clock. The proposed PWCL architecture is discussed in section II. The HSPICE circuit simulation results are illustrated in section III. Section IV gives the conclusion.

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Shao-Ku kao Author is with Department of Electrical Engineering and Green Technology Research center, Chang Gung University, Tao-Yuan, Taiwan, R.O.C. (e-mail: kaosk@mail.cgu.edu.tw).

Yong-De You Author was with Department of Electrical Engineering, Chang Gung University, Tao-Yuan, Taiwan, R.O.C.

I.Circuit Descriptions

The proposed low control voltage noise PWCL shown in Fig. 1. It consists of a control stage (CS), a buffer, a signal input to complementary output circuit (STC), two charge pump with charge sharing circuit (CPCS), two multiplexers (MUX), a lock detector (LD) and a differential pair amplifier (Amp). The STC converts the input clock to complementary signals [3]. The multiplexers generate *VCP* and *VCN* according to the LD. The input signals of multiplexers are generated by the CPCS. The output voltage, *VCP/VCOUT_P* and *VCN_VCOUT_N* of the CPCS are generated according to the duty cycle of input clocks *Clkout* and *Clkref* of STC, respectively. The differential pair amplifier detects the difference between *VCP* and *VCN* generates a feedback control voltage *Vctrl* to the CS to adjust the duty cycle of output clock. When *VCP* largest than *VCN*, the control voltage *Vctrl* is risen. When *VCP* smallest than *VCN*, the control voltage *Vctrl* is fallen. Initially, to reduce the lock time, the output of CPCS are *VC_N* and *VC_P* are the output of MUX at begin of lock state. They both feed into the differential pair amplifier and generate the control voltage *Vctrl*. When $| VC\_P - VC\_N | = 0.01 \cdot VC\_N$, the lock detector is enabled to select the D1 of MUX. The outputs of MUX become the *VCOUT_N* and *VCOUT_P*. The *VCOUT_N* and *VCOUT_P* are the charge sharing output voltage. Finally, the duty cycle of *Clkout* and *Clkref* both reach 50%. The voltage of *VCP* equals voltage of *VCN*. A stable and low ripple control voltage *Vctrl* is generated to achieve decreasing the output clock jitter.

The control voltage *Vctrl* is employed to adjust the pulsewdith of the output clock. Therefore, the ripple of the control voltage *Vctrl* directly affects the jitter of output clock. The ripple of the control voltage *Vctrl* can be reduced using a large capacitor that results large silicon area. The ripple of control voltage *Vctrl* due to the amplifier inputs, that are two outputs voltage of MUX, *VCN* and *VCP*. To reduce the variation of the *VCN* and *VCP*, a modified the conventional charge pump is proposed. The modified the charge pump circuit with charge sharing circuit is shown in Fig. 2. It is composed of conventional charge pump, two equal capacitors

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C1 and C2 and a switch. The modified the charge pump circuit with charge sharing circuit can be analyzed in two phases according to the voltage level of the input clocks, *Clkout* and *Clkref*, as shown in Fig. 3. Assume the control voltage *Vctrl* is on steady state, when | *VC_P* – *VC_N* | = 0.01·*VC_N*. In the high level phase, the input clock of *Clkout/Clkref* switch to its high level, only capacitor C1 is discharged according to the duty cycle of input clocks. The voltages of *VC_P* and *VC_N* are drop and the voltages of *VCOUT_N* and *VCOUT_P* maintain as before. During the low level phase, due to the voltages of *VC_P* and *VC_N* smaller than *VCOUT_N* and *VCOUT_P*, the charge in capacitor C2 is shared with C1 at begin of the low level phase. Afterward, both capacitors are charged to a potential according to the lower level of input clocks. The timing diagram of CPCS is shown in Fig. 4. Since the charge sharing occurs very cycle, the output voltage, *VCOUT_N*/*VCOUT_P* will converge to a less variation voltage when 50% duty cycle of *Clkout/Clkref* is generated. When the loop in the steady state, the amplitude of conventional charge pump output voltage *VC* can be expressed as

$$\mathrm{VC} = \frac{\mathrm{T_{per}} \cdot \mathrm{Iref}}{2\mathrm{C}} \tag{1}$$

Where T_{per} is the period of input clock, and Iref is charge pump charge and discharge current, C is output capacitor. When the loop in the steady state, the output voltage amplitude of modified the charge pump circuit with charge sharing circuit *VOUT* can be expressed as

$$\mathrm{VOUT} = \frac{\mathrm{Iref} \cdot \mathrm{T_{per}}}{2(\mathrm{C1}+\mathrm{C2})} \frac{\mathrm{C2}}{(\mathrm{C1}+\mathrm{C2})} \tag{2}$$

If C1=C2=C/2, then the output voltage can be expressed as

$$\mathrm{VOUT} = \frac{\mathrm{Iref} \cdot \mathrm{T_{per}}}{4\mathrm{C}} \tag{3}$$

At Equation (3), due to the charge sharing scheme, the capacitor value is double compare to the Equation (1). The less variation of the *VCN* and *VCP* feed to the amplifier. Therefore, with charge sharing scheme reduces amplitude of control voltage *Vctrl*. The ripple of the *Vctrl* is reduced. It has been proven the jitter of the output clock can be reduced with the same size of the capacitor as compared with previous work [2].

II. Simulation result

A 0.18μm CMOS process model is used for the HSPICE simulation. Fig. 5 and Fig. 6 show the output duty cycle can be corrected to 50% at the input clock with 60% and 40% duty cycle, respectively. The output duty cycle error is less than ±1% at frequency of 1GHz as shown in Fig. 5 and Fig.6. Fig.7 presents the jitter of output clock between proposed circuit and conventional CP. With HSPICE simulation, it indicates 3.2 ps and 5.14 ps peak-to-peak jitter of the propose PWCL and conventional CP, respectively. Fig. 8 plots peak-peak jitter of output clock between proposed circuit and conventional CP. The proposed circuit reduces the peak-peak jitter of output clock at frequency range from 100MHz to 1GHz. From the simulation results, the proposed circuit reduces the output clock jitter by 37.7% and 50.6% at 1GHz and 100MHz, respectively.

III. Conclusion

This paper presents pulsewidth control loop with low control voltage ripple. With modified the charge pump with charge sharing circuit to reduce jitter of output clock. The jitter of output clock is induced by the ripple of charge pump output voltage. With charge sharing circuit, the variation of output voltage of the charge pump is reduced. The proposed circuit is demonstrated by simulation results in 0.18μm CMOS process. At 1 GHz and 100 MHz, the proposed circuit reduces the peak-to-peak jitter of output clock by 37.7% and 50.6% compared to the conventional CP used in mutual-correlated PWCL [2].

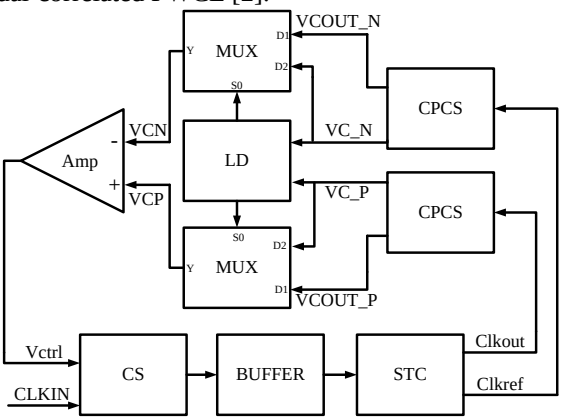


Fig. 1 Propose pulsewidth control loop with low control voltage

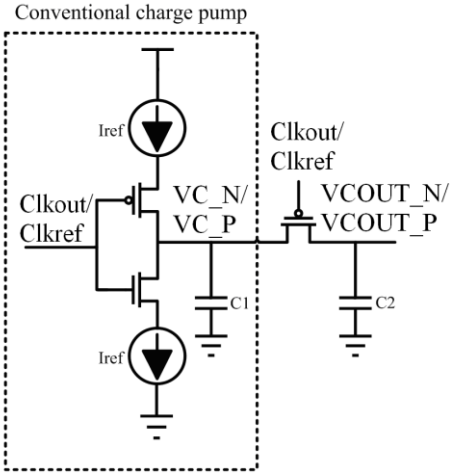


Fig. 2 Charge pump with charge sharing circuit

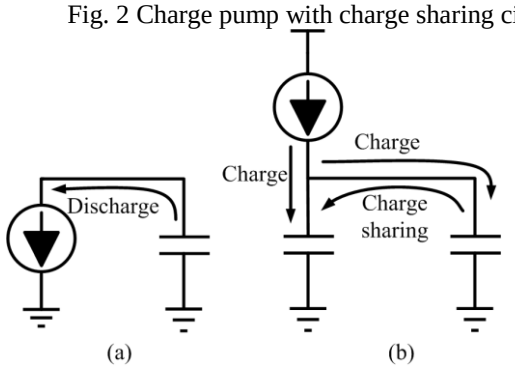


Fig. 3 Two phase of CPCS (a) Low level phase (b) High level phase

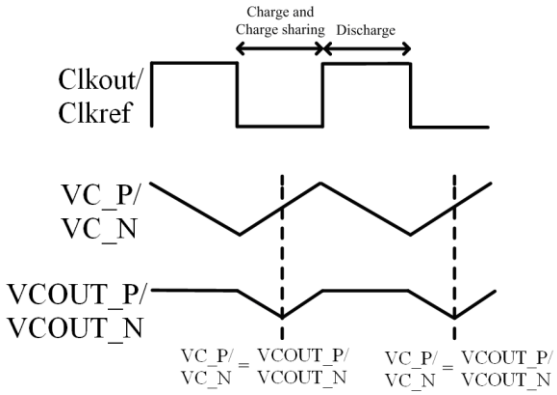


Fig.4 Timing diagram of CPCS during charge sharing

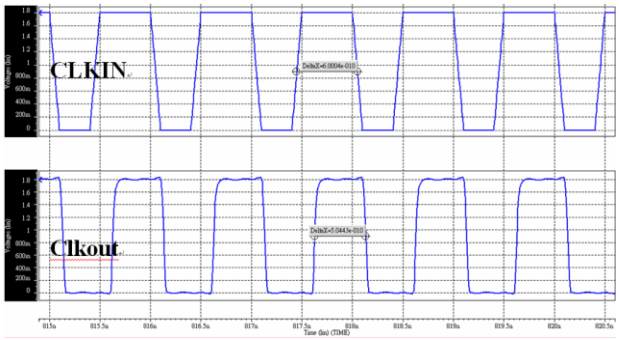


Fig.5 60% duty cycle of input clock at 1GHz

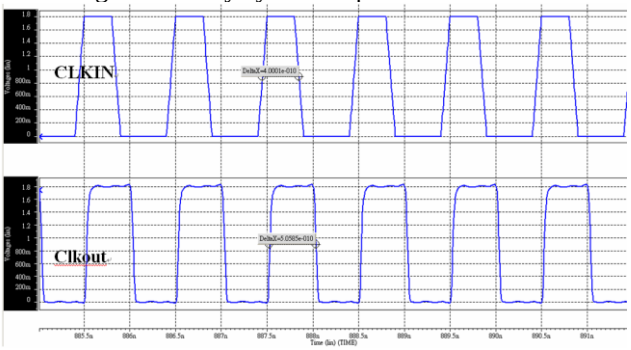
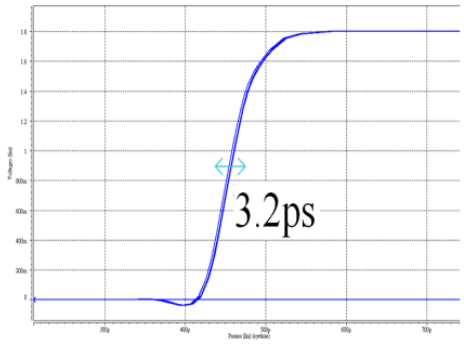
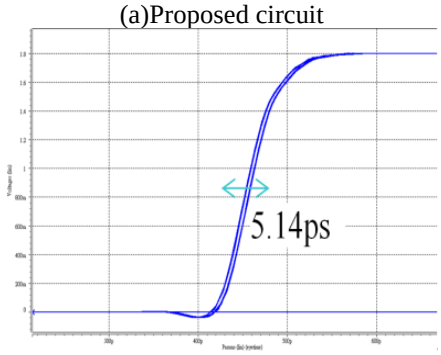


Fig. 6 40% duty cycle of input clock at 1GHz



(a)Proposed circuit



(b) Conventional CP

Fig. 7 Output clock jitter at 1GHz

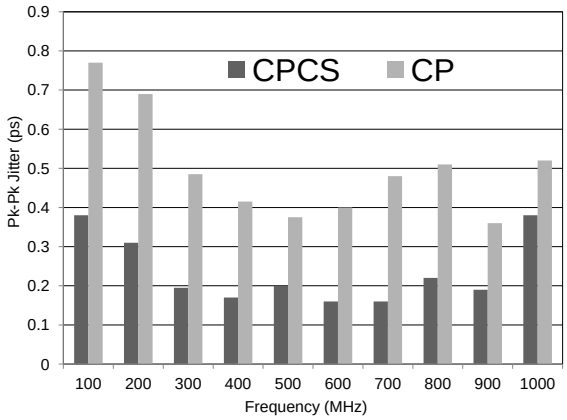


Fig. 8 Output clock jitter versus operation Frequency

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