Multi Chip Packaging (MCP) or Not MCP?

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***Abstract*—In a small form factor design, multi chip packaging (MCP) or not is always a critical decision to make. The intend of this paper is to explore prior art where multi chip packaging decision sound as well as the consideration needed for multi chip packaging execution from die design engineer perspective.**

***Index Terms*—Multi chip packaging, cost, die**

I. Introduction

MULTI chip packaging(MCP) is an electronic module system where multiple bare die are package on single substrate. The advantages of MCP implementation are:

- Lower Cost: MPC's cost saving is the result of fewer packages with few number of leads, a simplified board layout, and the feasibility of mixed technologies in the same package.
- Mixed Signal Application: MCP allows the integration of chips made of different technologies in one package
- Lower Power Consumption: Smaller drivers are needed resulting in lower IO drive strength configuration needed for inter chip transfer within the same package, thus lower power consumption
- Higher Integration Density: MCP allows high integration density through substitution of several packages for one slightly larger but single package. It will either free board real estate for other use or help reduce the board size
- Improved Performance: Closer and shorter interconnection lengths between dies enhance system speed dramatically through MCP implementation
- Time To Market: MCP finds its niche in packaging as transitory stage between product needs and chip integration through insertion of several dies into the same package that allows much faster introduction of the product into the market compared to integrating all the desired functions on a new single chip. Timely introduction is essential since the highest profit margins are always achieved in the early stages of the product life cycle
- Reliability: Smaller system through MCP implementation can be protected from electromagnetic interference, liquids and gases more easily than a larger system
- Simplification Of Motherboard Design: Subsystem with high wiring demands can be integrated on MCP with limited number of external connections, thus reduce the number of wiring layers required on the motherboard
- Reusability/Standardization: An MCP can integrate functions required in family products, thereby creating a component that can handle like single IC. Some functions can be integrated as logical and physical blocks in new designs

This paper is intended to share the prior art to multi chip packaging consideration as well as necessary consideration for MCP integration. Due to the design complexity, wafer size, fab process, technology node and signoff PVT, it may not impact all designers but do hope the reader may benefit from this sharing.

II. Multi chip packaging implementation type

For multi chip packaging implementation, in general can be summarized as in table 1[2][3].

For multi chip packaging implementation, it is driven by product definition, time to market, reusability as well as cost as the main driver. For the purpose of this paper discussion, it will mainly focus on the flat chip implementation style where analysis will be driven by cost perspective. Expensive multi chip packaging implementation such as through silicon via consideration will be excluded from this discussion due to cost as primary reason.

During multi chip packaging planning initiative phase, there are few key considerations needed, such as

1. Inter die spacing in the range of mm may be key limiting factor in packaging routing congested design or limited package body die size scenario
2. Inter chip IO sharing or interchip IO connection where extra packaging routing is required
3. Power plane budget as well as power plane resource sharing

The above consideration is essential for better resource sharing and mitigate package pin count limitation for multi

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chip package implementation.

III. Multi Chip Packaging Usage Cost

To simplify the discussion of this paper, the based assumption made is the cost of combine package solution will be lower than individual package of each chip. The gross die count per wafer(GDPW)[1] extraction for this paper is done based on 300mm diameter wafer. The analysis for multi chip packaging usage cost will be divide into 4 main category which differentiate by process as well as die size.

A. Usage Cost 1: Homogeneous Process Heterogeneous Die Size

For the homogeneous process die consideration where process node and metal scheme is identical, 2 separate heterogeneous die size is analyzed and the normalized total die cost analysis is as shown in table 2 and table 3.

From table 2, it is observed that having 2 individual die size of $250mm^2$ and $8mm^2$ in multi chip packaging solution does not yield the lowest total die cost ownership. When the area of the second die grow from $8mm^2$ to $125mm^2$, it bring more economical reason to implement it as multi chip packaging then integrate it on single die solution for lowest total die cost as shown in table 3

B. Usage Cost 2: Heterogeneous Process Heterogeneous Die Size

For heterogeneous process and heterogeneous die size consideration, further analysis is carried out on the scenario where MCP implementation does not yield the lowest total die cost ownership and solution required through heterogeneous process as well as the solution for single integrated die where MCP implementation yield the lowest total die cost ownership with heterogeneous process taken into consideration.

From table 2, for 2 separate chips of $250mm^2$ and $8mm^2$ die size, MCP implementation on homogenous process does not yield the lowest total die cost ownership. Further analysis is done on heterogeneous process to determine the necessary cost reduction needed on smaller die ($8mm^2$) needed in order to meet the lowest total die cost ownership. The result is as shown in table 4.

From table 4, it is observed that 40% cost reduction needed on $8mm^2$ die in order to achieve lowest total die cost ownership for multi chip packaging implementation. Such requirements can only be achieve with lower metal scheme as well as multi layer mask implementation on $8mm^2$ die size in order to meet the cost budget required.

In the event where multi chip packaging solution is preferred due to lowest total die ownership, future investigation is carried to determine the lowest cost of ownership by chip integration. The result is as shown in table 5.

From table 5, in order to achieve lowest cost of total die ownership for single integrated die solution, 50% die area reduction is required while meeting the logic gate density on advance technology node(N+1) compare to current process(N). The analysis above does account for the guestimate of 45% mask cost increment for transition into one generation fabrication node ahead as well as guestimate of 30% design cost increment in one generation fabrication node advancement.

C. Usage Cost 3: Homogeneous Process Homogeneous Die Size

For homogeneous process and homogeneous die size implementation such as DDR memory array, stack die is always the preferred solution traditionally.

From table 6, it is observed that for the same die on homogeneous process, MCP implementation always yield the lowest total die cost ownership

D. Usage Cost 4: Heterogeneous Process Homogeneous Die Size

In the event of heterogeneous process integration is allowed, die size integration with 50% combine die area reduction will yield the lowest total die cost ownership with the extra overhead from mask and design cost taken into consideration. The result of the analysis is as shown in table 7

IV. Summary

The summary of MCP usage cost is as shown in table 8.

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REFERENCES

[1] Wafer web reference http://en.wikipedia.org/wiki/Wafer_(electronics)
[2] Packaging reference source http://www.statschippac.com
[3] Robert Doering, Yoshio Nishi, Handbook of Semiconductor Manufacturing Technology,2nd Edition.chapter 32 Integrated-circuit packaging, chapter 35 economics of semiconductor manufacturing

Table 1. Multi Chip Packaging Summary

Multi Chip Packaging Type	Implementation Details	bonding type
flat chip implementation	multiple dies with die to leadframe bonding.No substrate	wire bond
	multiple dies with die to die bonding.No substrate	wire bond
	multiple dies with jumper chip. No substrate	wire bond
	multiple dies on substrate	flip chip/wire bond
	multiple dies with silicon interposer for through silicon via	flip chip
none flat chip implementation	vertical stack dies with spacer material in between	wire bond
	vertical stack dies with adhesive layer for through silicon via	wire bond/flipchip
	package on package stacking	wire bond/flipchip
	fully molded package on package with through mold via	wire bond/flipchip

Table 2 Normalized Die Cost Analysis on 300mm Wafer For Homogeneous Process Heterogeneous Die Size

Costing Type	Process	Chip Size (mm^2)	GDPW	Cost Per Die	Total Die Cost
MCP	N	250	241	0.00414938	0.004265806
	N	8	8589	0.00011643	
Integrated with fixed floorplan Aspect Ratio	N	258	233	0.00429185	0.004291845
Multi Project Wafer	N	258	209	0.00478469	0.004784689
Integrated with fixed die height and area and grow width	N	258	237	0.00421941	0.004219409

Table 3 Normalized Die Cost Analysis on 300mm Wafer For Homogeneous Process Heterogenous Die Size

Costing Type	Process	Chip Size (mm^2)	GDPW	Cost Per Die	Total Die Cost
MCP	N	250	241	0.00414938	0.006129576
	N	125	505	0.00198020	
Integrated with fixed floorplan Aspect Ratio	N	375	153	0.00653595	0.006535948
Multi Project Wafer	N	375	139	0.00719425	0.007194245
Integrated with fixed die height and area and grow width	N	375	161	0.00621118	0.00621118

Table 4 Normalized Die Cost Analysis on 300mm Wafer For Heterogeneous Process Heterogeneous Die Size

Costing Type	Process	Chip Size (mm^2)	GDPW	Cost Per Die	Saving Multiplier	Total Die Cost
MCP	N	250	241	0.004149378	1	0.00421923
	N	8	8589	0.000116428	0.6	
Integrated with fixed floorplan Aspect Ratio	N	258	233	0.004291845		0.00429185
Multi Project Wafer	N	258	209	0.004784689		0.00478469
Integrated with fixed die height and area and grow width	N	258	237	0.004219409		0.00421941

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Table 5 Normalized Die Cost Analysis on 300mm Wafer For Heterogeneous Process Heterogeneous Die Size

Costing Type	Process	Chip Size (mm^2)	GDPW	Cost Per Die	Total Die Cost
MCP	N	250	241	0.00414938	0.006129576
	N	125	505	0.0019802	
Integrated with fixed floorplan Aspect Ratio	N	375	153	0.00653595	0.006535948
Multi Project Wafer	N	375	139	0.00719425	0.007194245
Integrated with fixed die height and area and grow width	N	375	161	0.00621118	0.00621118
Integrated with 40% die area reduction on advance technology node	N+1	225	275	0.00685455	0.006854545
Integrated with 50% die area reduction on advance technology node	N+1	187.5	335	0.00562687	0.005626866

Table 6 Normalized Die Cost Analysis on 300mm Wafer For Homogeneous Process Homogeneous Die Size

Costing Type	Process	Chip Size (mm^2)	GDPW	Cost Per Die	Total Die Cost
MCP	N	30	2245	0.000445434	0.000890869
	N	30	2245	0.000445434	
Integrated with fixed floorplan Aspect Ratio	N	60	1099	0.000909918	0.000909918
Multi Project Wafer	N	60	903	0.00110742	0.00110742
Integrated with fixed die height and area and grow width	N	60	1101	0.000908265	0.000908265

Table 7 Normalized Die Cost Analysis on 300mm Wafer For Heterogeneous Process Homogeneous Die Size

Costing Type	Process	Chip Size (mm^2)	GDPW	Cost Per Die	Total Die Cost
MCP	N	200	301	0.00332226	0.006644518
	N	200	301	0.00332226	
Integrated with fixed floorplan Aspect Ratio	N	400	145	0.00689655	0.006896552
Multi Project Wafer	N	400	145	0.00689655	0.006896552
Integrated with fixed die height and area and grow width	N	400	145	0.00689655	0.006896552
Integrated with 50% die area reduction on advance technology node	N+1	200	301	0.00626246	0.006262458

Table 8 Multi Chip Packaging Usage Cost Summary

Multi Chip Package Usage Cost	Keynotes
Homogeneous process heterogeneous die size	Thorough total cost study is needed as integrated die solution will not always yield the lowest total die cost ownership on homogenous process
Heterogeneous process heterogeneous die size	MCP may still be lowest total die cost ownership solution in the event of the dies of different metallization scheme on same fabrication technology node is used
Homogeneous process homogeneous die size	MCP is always the preferred solution from total die cost ownership
Heterogeneous process homogeneous die size	Integrated chip with 50% combined die area reduction on one fabrication technology node advancement will result in lowest total die cost ownership provided total metallization does not increase

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