Floating Capacitance Multiplier Circuit Using Full-Balanced Voltage Differencing Buffered Amplifiers (FB-VDBAs)

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***Abstract*—This paper presents the resistor-less realization of a floating capacitance multiplier circuit using full-balanced voltage differencing buffered amplifiers (FB-VDBAs) as active components. The presented capacitance simulator contains only two FB-VDBAs together with a single grounded capacitor without any passive resistors. The equivalent capacitance value of the realized capacitance simulator can be tuned electronically by controlling the transconductance values of the FB-VDBAs. Anapplication of the proposed tunable capacitance multiplier in realizing the *RLC* bandpass filter is also. Simulations by PSPICE program for standard 0.35-μm BiCMOS process parameter shave been provided to verify the theory.**

***Index Terms*— full-balanced voltage differencing buffered amplifier (FB-VDBA), electronically tunable, resistor-less circuit, floatingcapacitance multiplier.**

I. Introduction

In the design of integrated circuits, it is still a limiting impractical to fabricate large-valued physical capacitors because of occupied chip area [1]. This justifies the existences of many design techniques for implementing capacitance multiplier circuits using various modern electronic active building elements [2]-[13]. However, all of them need either two of more active devices or more than one passive element for floating capacitance simulation [2]-[13]. The simulator presented in [3]-[7] employ floating passive components, which is not very attractive for further integration. Moreover, the works of [3]-[5], [7]-[11] still use some external passive resistors. It should be noted that the circuit using a minimum number of active and passive elements is important from the point of view of VLSI implementation, power consumption, cost and area on the chip.

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Recently, the newly introduced active element called full balanced voltage differencing buffered amplifier (FB-VDBA) [14]. To demonstrate the usefulness and easy implementation in fully-balanced structures, several interesting applications of FB-VDBA in mainly analog signal processing and generation circuits were also introduced [14]-[18]. The major advantage of the FB-VDBA can be thought as the feasibility and versatility. This is due to the fact that the FB-VDBA combines the simplicity of the fully-balanced structure with the classical voltage differencing feature of the VDBA.

The solution proposed here consists of a floating capacitance multiplier circuit made up of two FB-VDBAs and one grounded capacitor. The resulting circuit is canonic in nature and resistor-less structure, as well as very suitable for integrated circuit implementation point of view. The equivalent capacitance value (C_{eq}) of the proposed actively simulated floating capacitor can be adjustable electronically by the transconductance gains of the FB-VDBAs. To further demonstrate the usability of the floating capacitance simulator, an active *RLC* bandpass filter design has been given. PSPICE simulation results are given to verify the workability of the designed floating simulator circuit and its application.

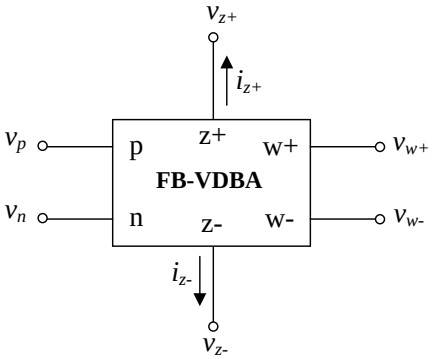

Fig. 1 Schematic symbol of the FB-VDBA.

II. Description of The FB-VDBA

The circuit symbol of the FB-VDBA is shown in Fig. 1. The FB-VDBA device has a pair of high-impedance differential voltage inputs labeled p and n), and a pair of high-impedance current outputs named z+ and z-, and low-impedance outputs of voltage buffer named w+ and w-. The terminal relations of the FB-VDBA can be expressed by the following matrix

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equation [14] :

$$\begin{bmatrix} i_{z+} \\ i_{z-} \\ v_{w+} \\ v_{w-} \end{bmatrix} = \begin{bmatrix} g_m & -g_m & 0 & 0 \\ -g_m & g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_p \\ v_n \\ v_{z+} \\ v_{z-} \end{bmatrix} \quad (1)$$

where the parameter g_m implies the transconductance gain of the FB-VDBA. In Eq.(10), the g_m-value is possible to control electronically via the external supplied current or voltage.

Recently, the possible realization of the FB-VDBA in BiCMOS technology is introduced. Fig. 2 shows the internal BiCMOS structure of the recently introduced FB-VDBA [18]. It is designed by combining bipolar and CMOS technologies in order to utilize the main advantages of each technology, i.e., higher transconductance, higher frequency, low power consumption, and small silicon area. The FB-VDBA in Fig.2 is a combination of the transconductance amplifier as the input stage (M_1-M_2, Q_1-Q_4), the mirror stages (Q_5-Q_7, Q_8-Q_{10}, Q_{11}-Q_{12} and Q_{13}-Q_{14}) transfer the current to ports z+ and z-, respectively, and the unity-gain voltage buffer as the output stage (M_3-M_6 and M_7-M_{10}). The small-signal effective transconductance (g_m) of the FB-VDBA can be written as :

$$g_m = \frac{I_B}{V_T} \quad (2)$$

Where $V_T \cong 26$ mV at 27 ^oC is the thermal voltage. Eq.(2) indicates that the g_m-value of the realized FB-VDBA is tunable linearly and electronically by an external DC bias current I_B.

Moreover, if we assume all the transistors operate in the active region. Therefore, the elective small-signal voltage gains in Fig. 2 are approximately to :

$$\frac{v_{w+}}{v_z} \cong \frac{g_3 g_6}{g_4 g_5} \quad (3)$$

and

$$\frac{v_{w-}}{v_z} \cong \frac{g_7 g_9}{g_8 g_{10}} \quad (4)$$

where g_i denotes the conductance of transistor M_i (i = 1, 2,..,10). Assume that all the transistors have the same g_i-values, thus $v_{w+} \cong v_z$ and $v_{w-} \cong v_z$ as expected.

III. Proposed Floating Capacitance Multiplier

The proposed floating capacitance simulator circuitusing FB-VDBAs as active elements is shown in Fig. 3. The proposed floating inductor constructionly two FB-VDBAs and one grounded capacitor without external passive resistor requirement,thus, the floatingcapacitoriscanonical structure and also more suitablefor integrated circuit implementation point of view.Circuit calculation of the proposed circuit in Fig. 3 shows that the input impedance is equal to :

$$Z_{in} = \frac{v_1 - v_2}{i_C} = \frac{g_{m1}}{sC_1 g_{m2}} \quad (5)$$

where the parameter g_{mi} denotes the transconductance value of i-th FB-VDBA (i = 1, 2).

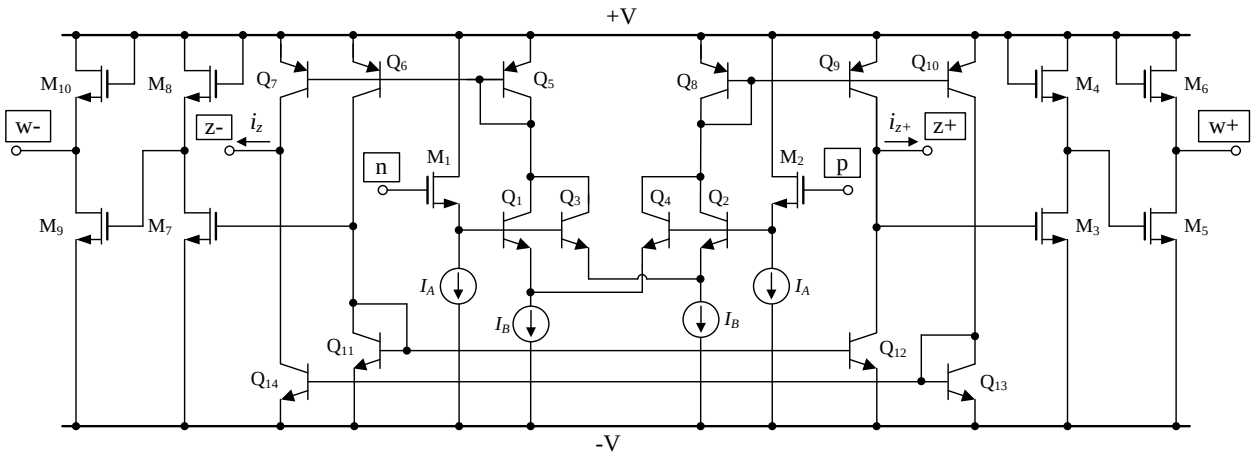

Fig. 2 BiCMOS realization of the FB-VDBA [18].

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Eq.(5) indicates that the proposed circuit can simulate a floating capacitor with an equivalent capacitance C_{eq}:

$$C_{eq} = \frac{C_1 g_{m2}}{g_{m1}} \tag{6}$$

It is to be noted form eq.(5) that the C_{eq}–value is adjustable electronically by tuning g_{m1} and/or g_{m2}.

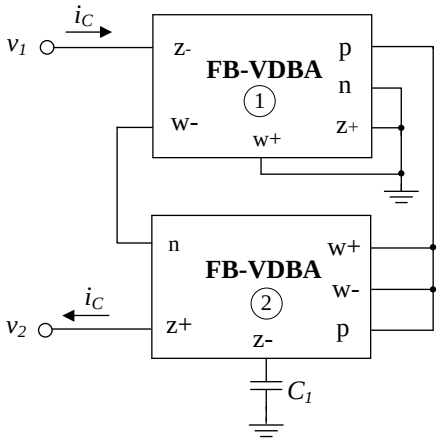


Fig. 3 Proposed actively floating capacitance multiplier circuit.

IV. Circuit Performance Simulations

The performance verification of the proposed FB-VDBA realization in Fig. 3,the circuit was simulated on PSPICE program. In simulations, the FB-VDBA given in Fig. 2 was implemented with standard 0.35-μm BiCMOS process parameters [18]. Transistor aspect ratios (W/L in μm/μm) were selected as : 14/0.7 and 56/0.7 for M_1-M_2 and M_3-M_{10}, respectively. The circuit was biased at : I_A = 25 μA under the supplied voltages of +V = -V = 1 V.

The simulation results of the proposed floating capacitor in Fig. 3 are also performed with the following active and passive components : C_1 = 0.1 nF, $g_{m2} \cong$ 1.92 mA/V ($I_{B2} \cong$ 50 μA) and $g_{m1} \cong$ 3.84 mA/V, 1.92 mA/V, 1.28 mA/V, ($I_{B1} \cong$ 100 μA, 50 μA and 33 μA), to obtain C_{eq} = 0.05 nF, 0.1 nF and 0.15 nF, respectively.

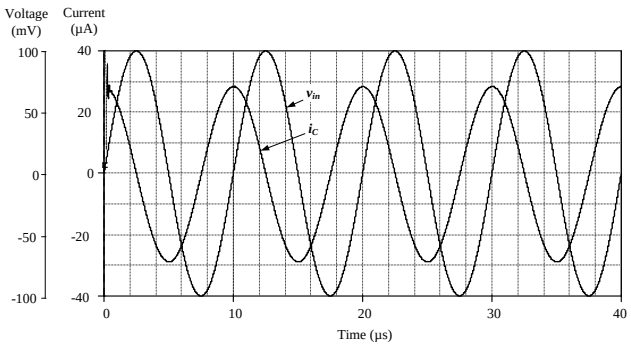
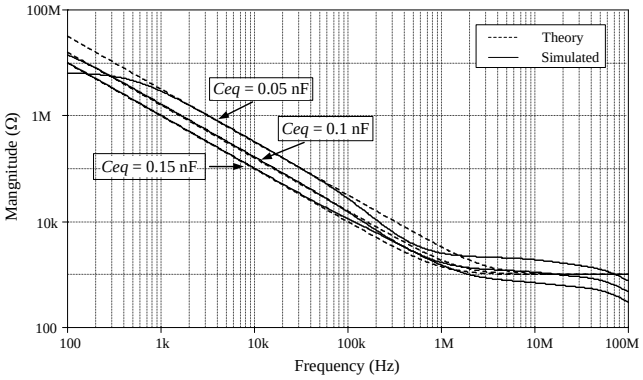
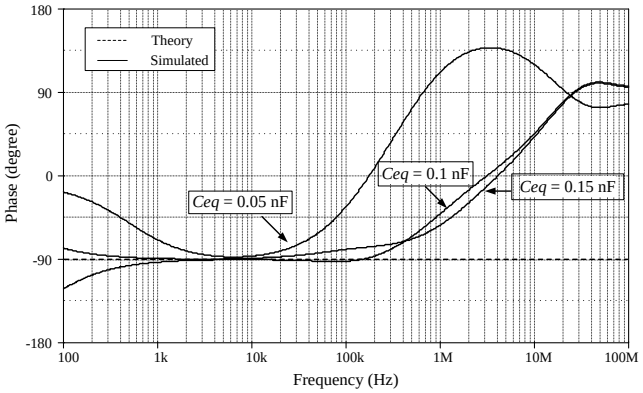


Fig. 4 Simulated transient responses for v_{in} and i_C of the floating inductor in Fig. 3.

Fig. 4 depicts the simulated transient responses for v_{in} (= v_1–v_2) and i_C of the input impedance of the proposed floating capacitance simulator. The results obtained from the simulation show that the current i_C leads the voltage v_{in} by 89.57°. The simulated frequency characteristics of the input impedance of the proposed inductor are shown in Fig. 5.



(a)



(b)

Fig. 5 Theoretical and simulated frequency responses of the proposed floating capacitor circuit in Fig. 3.

(a) magnitude responses (b) phase responses

V. Application Example

As example to demonstrate an application of the proposed floating capacitor of Fig. 3, it is employed in the *RLC* bandpass filter as shown in Fig. 6. The C_{eq} was selected as: C_1 = 0.1 nF and $g_{m1} = g_{m2} \cong$ 1.92 mA/V ($I_{B1} = I_{B2} \cong$ 50 μA) for simulating $C_{eq} \cong$ 1 nF. Fig. 7 shows the idea and simulated frequency responses of the bandpass filter in Fig. 6. It appears, thus, that the simulated and ideal values are in good agreement. In addition, in order to demonstrate the electronic controllability of the proposed floating inductor, the value of C_{eq} in Fig. 6 was respectively varied to 0.05 nF, 0.1 nF and 0.15 nF, by changing $g_{m2} \cong$ 3.84 mA/V, 1.92 mA/V, 1.28 mA/V, respectively while keeping g_{m2} constant at 1.92 mA/V. This tuning leads to obtain the center frequency $f_c \cong$ 270 kHz, 190 kHz and 156 kHz, respectively.

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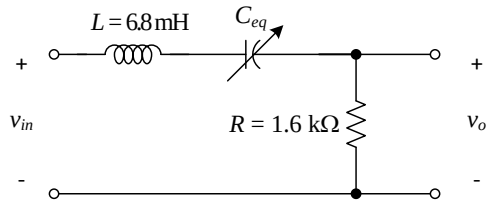

Fig. 6 *RLC* bandpass filter realized with the synthetic floating inductor of Fig. 3.

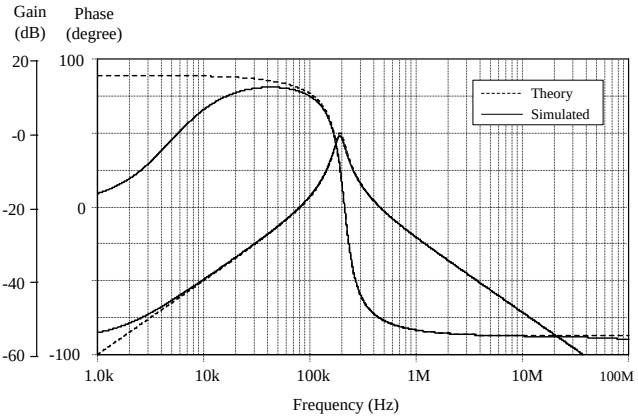

Fig. 7 Frequency responses of the bandpass filter in Fig. 6 at $f_c \cong 193.6$ kHz.

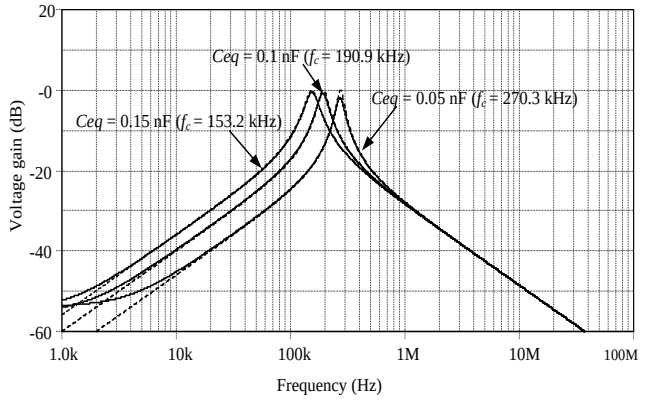

Fig. 8 Gain responses of Fig. 6 with electronically variable C_{eq}.

VI. Conclusion

This paper presents the floating capacitance simulator that employs only two FB-VDBAs and one grounded capacitor, resulting in canonical structure as well as attractive for integration.Its equivalent capacitance values can be adjusted electronically through the transconductance parameter g_m of the FB-VDBA. As an application example, the proposed circuit is demonstrated on the *RLC* bandpass filter. The performance of the proposed FB-VDBA is discussed and also verified by PSPICE simulations using standard 0.35-μm BiCMOS technology.

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