SFG Actualization of General nth-Order Voltage Transfer Functions Using VDBAs

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***Abstract*—This work presents the synthesis of general nth-order voltage transfer functions with voltage differencing buffered amplifiers (VDBAs) using signal flow graph (SFG) technique. Without the employment of external passive resistors, the designed procedure requires only *n* VDBAs and *n* capacitors for nth-order transfer function realization. As application examples, the first-order allpass and standard biquadratic function realizations are demonstrated. The simulation results by PSPICE have also been provided, which verify the usefulness of the presented technique.**

***Keywords* — Signal Flow Graph (SFG), Voltage Differencing Buffered Amplifier (VDBA), universal filter**

I. Introduction

Recently, analog active building blocks were developed and invented continuously. Among these, the voltage differencing buffered amplifier (VDBA) is the newly defined active circuit building block [1]. This device is slightly modified from the conventional current differencing buffered amplifier (CDBA) by replacing the current differencing unit with a transconductance amplifier [2]. The difference between VDBA and CDBA is that the VDBA inputs are voltages as for the CDBA inputs are currents. Many applications based on the use of the VDBAs as active elements in analog signal processing area have also been developed in the literature [3]-[7]. In addition, the works of [8]-[17] have proposed the actively circuit realizations of an nth-order voltage transfer function synthesis based on the signal-flow-graph (SFG) approach employing various active elements. However, all the available SFG circuit realizations employ an excessive number of active and passive elements, at least *n* active devices, *n* resistors and *n* capacitors.

Considering this fact, the work described in this paper mainly focuses on presenting a general synthesis procedure for realizing general nth-order voltage transfer functions. The proposed method is based on drawing a SFG directly from the given transfer function and then obtaining, from the graph, the active-C circuit configurations involving VDBAs. The resulting circuit uses only *n* VDBAs and *n* capacitors without needing any external passive resistors for nth-order transfer function realization. It has been shown that the design procedure proposed here is a canonical number of active and passive elements. Two illustrative examples together with PSPICE simulation results illustrate the usefulness of the proposed design procedure.

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II. Voltage Differencing Buffered Amplifier (VDBA)

The VDBA symbol is shown in Fig. 1. The relative characteristic between current and voltage of this device can be described by the following matrix [18]:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_{w+} \\ v_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_{w+} \\ i_{w-} \end{bmatrix} \tag{1}$$

where g_m is the transconductance gain of the VDBA. According to eq.(1), the differential input voltage between the terminals p and n (v_p- v_n) is then converted to a current at the z-terminal (i_z) by a g_m-parameter. The output voltages at terminals w+ (v_{w+}) and w- (v_{w-}) follow the voltage across the z-terminal (v_z). The voltages v_{w+} and v_{w-} will be of equal magnitude but different phases.

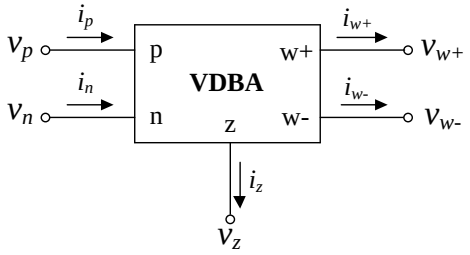

Fig. 1. Circuit symbol of the VDBA.

III. SFG Actualization Procedure

The general form of an nth-order voltage transfer function can be expressed by the following equation:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{b_n s^n \pm b_{n-1} s^{n-1} \pm \cdots \pm b_2 s^2 \pm b_1 s + 1}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_2 s^2 + b_1 s + 1} \tag{2}$$

where V_{in} and V_{out} are the input and the output voltages, respectively. The above equation can be represented by the SFG of Fig. 2. It can be observed that the graph is mainly

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composed of the cascading connection of the sub-graph shown in Fig. 3(a). Each sub-graph performs the lossless integrator, and its corresponding active-C sub-circuit involving VDBA is shown in Fig. 3(b). Therefore, according to Fig. 2 and 3, the resulting VDBA-based circuit can be realized in Fig. 4. It is important to note that the proposed technique requires only *n* VDBAs and *n* capacitors for realizing n[th]-order transfer function.

$$b_1 = \frac{C_1}{g_{m1}}$$

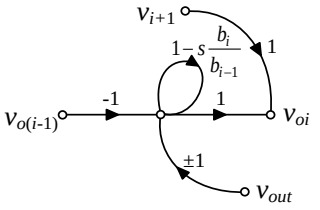
$$\frac{b_2}{b_1} = \frac{C_2}{g_{m2}}$$

$$\vdots$$

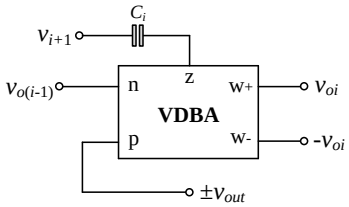
$$\frac{b_{n-1}}{b_{n-2}} = \frac{C_{n-1}}{g_{m(n-1)}}$$

and

$$\frac{b_n}{b_{n-1}} = \frac{C_n}{g_{m(n)}} \qquad (3)$$



(a)



where $\frac{b_i}{b_{i-1}} = \frac{C_i}{g_{mi}}$ and $i = 1, 2, 3, \ldots, n$

(b)

Fig. 3. Sub-graph of Fig. 2 and its corresponding VDBA-based circuit.

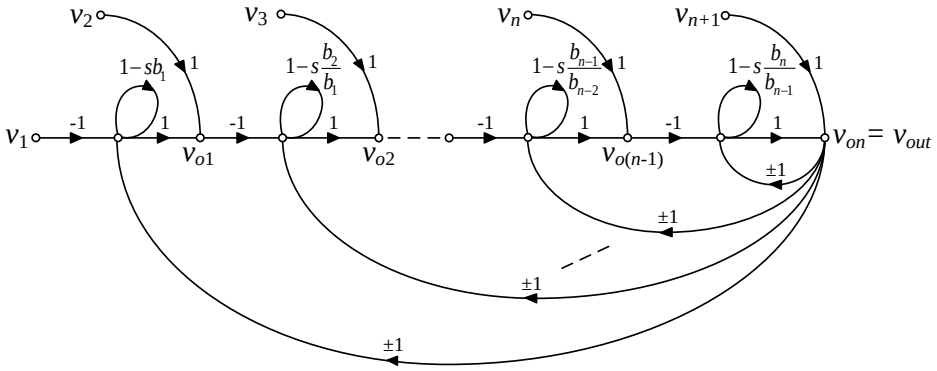


Fig. 2. Signal flow graph representation of eq. (2).

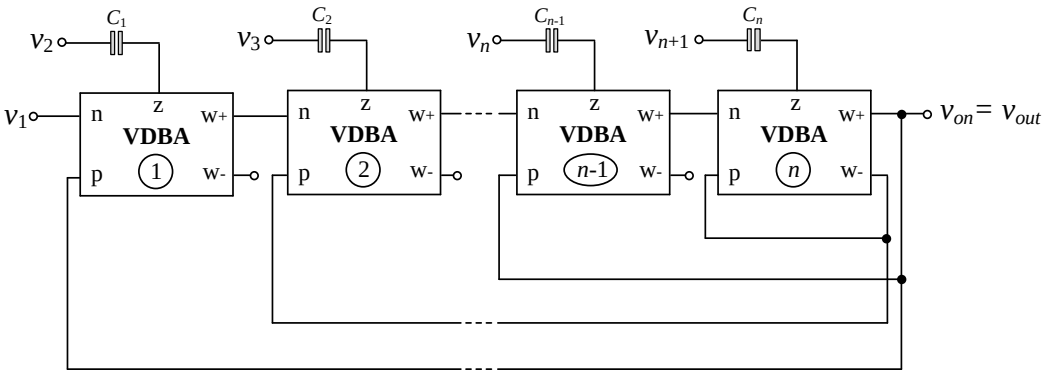


Fig. 4. The realization of n[th]-order universal voltage transfer functions of eq. (2) using VDBAs.

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IV. Illustrative Examples

The utility of the proposed procedure will be demonstrated by the two following examples:

A. First-order allpass realization

The transfer function of the first-order allpass filtering function can be defined by the following equation:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{sb_1 - 1}{sb_1 + 1} \tag{4}$$

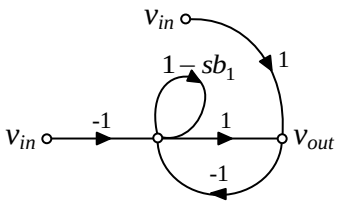
where $b_1 = C_1/g_{m1}$.

The SFG representation of eq. (4) can be given in Fig. 5(a), and its corresponding VDBA-C circuit realization can then be obtained as Fig. 5(b). As can be observed, the realized circuit consists of only one VDBA and one capacitor. In this case, the pole frequency (ω_p) and phase shift (ϕ) of the circuit are obtained as:

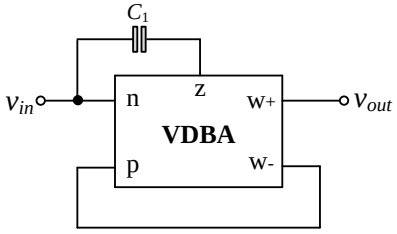
$$\omega_p = 2\pi f_p = \frac{g_{m1}}{C_1} \tag{5}$$

and

$$\phi = \pi - 2\tan^{-1}\left(\frac{\omega C_1}{g_{m1}}\right). \tag{6}$$



(a)



where $b_1 = \frac{C_1}{g_{m1}}$

(b)

Fig. 5. SFG realization of the first-order allpass function.

B. Second-order universal functions

The general form of the standard second-order voltage transfer functions can be given by the following expression:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{b_2 s^2 - b_1 s + 1}{b_2 s^2 + b_1 s + 1}. \tag{7}$$

The above expression can be represented by SFG diagram as shown in Fig. 6(a), and its realization involving VDBA-C can be shown in Fig. 6(b). In this case, two VDBAs and two capacitors are required. As a result of eq. (7), the voltage transfer function of Fig. 6(b) in term of the circuit component values can be written as:

$$V_{out}(s) = \frac{s^2 V_3 - \left(\frac{g_{m2}}{C_2}\right) sV_2 + \left(\frac{g_{m1}g_{m2}}{C_1C_2}\right) V_1}{s^2 + \left(\frac{g_{m2}}{C_2}\right) s + \left(\frac{g_{m1}g_{m2}}{C_1C_2}\right)} \tag{8}$$

where g_{mi} are the transconductance gain of the i-th VDBA (i = 1, 2). According to eq. (8), the standard second-order voltage transfer functions can be realized by the following conditions.

1) The lowpass (LP) function is realized, if $V_1 = V_{in}$ and $V_2 = V_3 = 0$.
2) The highpass (HP) function is realized, if $V_3 = V_{in}$ and $V_1 = V_2 = 0$.
3) The bandpass (BP) function is realized, if $V_2 = V_{in}$ and $V_1 = V_3 = 0$.
4) The bandstop (BS) function is realized, if $V_2 = 0$ and $V_1 = V_3 = V_{in}$.
5) The allpass (AP) function is realized, if $V_1 = V_2 = V_3 = V_{in}$.

Also from eq. (8), the pole frequency (ω_p), and the quality factor (Q) of circuit can be given by:

$$\omega_p = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{9}$$

and

$$Q = \sqrt{\frac{g_{m1}C_2}{g_{m2}C_1}} \tag{10}$$

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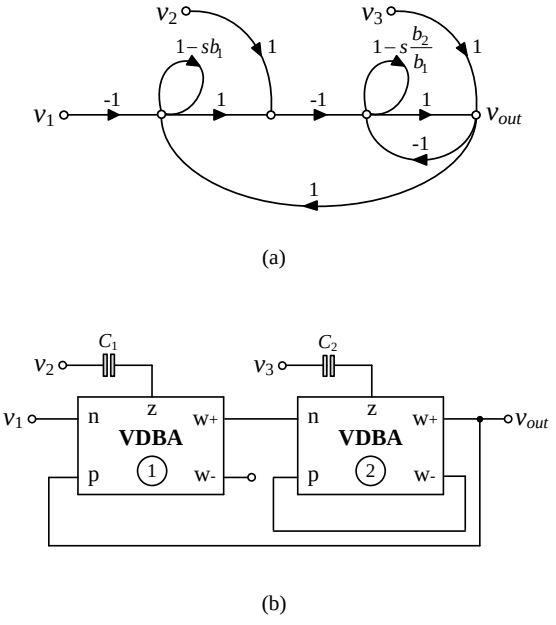

Fig. 6. Realization of the second-order universal filtering functions using SFG. (a) SFG representation (b) circuit realization

V. Simulation Results

To verify the feasibility of the designed procedure, the realized circuits have been simulated with PSPICE program. In simulations, the BiCMOS VDBA shown in Fig. 7 has been performed with the standard 0.35-μm BiCMOS technology [18]. The transistors sizes were chosen as: 14/0.7 and 28/0.7 for all NMOS and PMOS transistors, respectively. The supply voltages were V = ±0.75 V, and biasing currents were I_A = 25 μA. The small-signal effective transconductance (g_m) of the VDBA in Fig. 7 is given by:

$$g_m = \frac{I_B}{V_T} \tag{11}$$

where $V_T \cong$ 26 mV at 27 ˚C is the thermal voltage, and I_B is the external DC bias current.

To obtain the first-order allpass voltage response with the pole frequency of $f_p \cong$ 766 kHz. The circuit was designed with the following active and passive components: I_{B1} = 25 μA ($g_{m1} \cong$ 0.96 mA/V) and C_1 = 0.2 nF. Fig. 8 shows the ideal and simulated frequency characteristics of the first-order allpass filter realization of Fig. 5. The time domain responses are also shown in Fig.9, where the phase shift is recorded to be 84º.

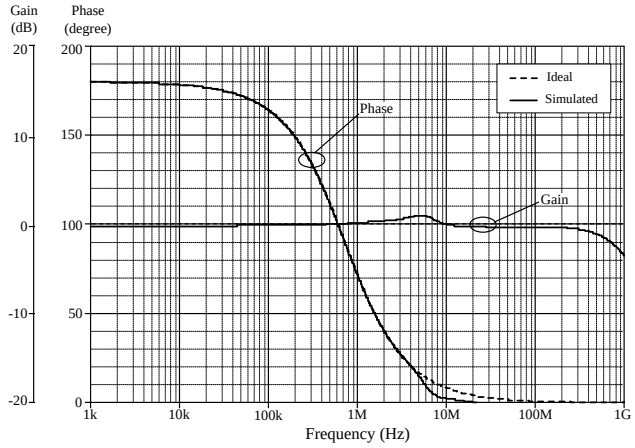

Fig. 8. Frequency response of the first-order allpass filter in Fig.5.

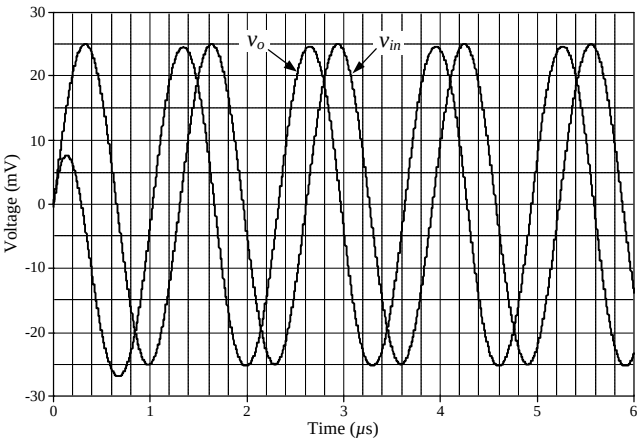

Fig. 9. Time domain responses of the first-order allpass filter in Fig. 5

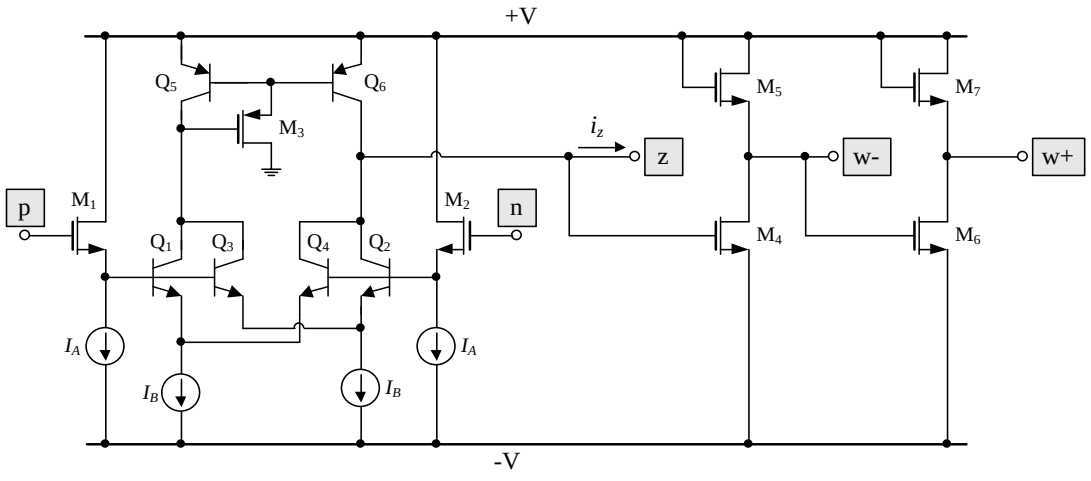

Fig. 7. BiCMOS realization of the VDBA.

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The ideal and simulated frequency responses of the second-order universal biquadratic filter in Fig. 6(b) are shown in Figs. 10 and 11. The results are obtained with $I_{B1} = I_{B2} = 38\ \mu$A ($g_{m1} = g_{m2} \cong 1.414$ mA/V) and $C_1 = C_2 = 1$ nF. This results in $f_p = 255$ kHz and $Q = 1$. From the results, the locations of the simulated f_p are about: 215.29 kHz, 219.92 kHz, 217.30 kHz, and 213.98 kHz for LP, HP, BS, and BP responses, which correspond to the following absolute errors: 4.33%, 3.28%, 3.38%, and 4.92%, respectively.

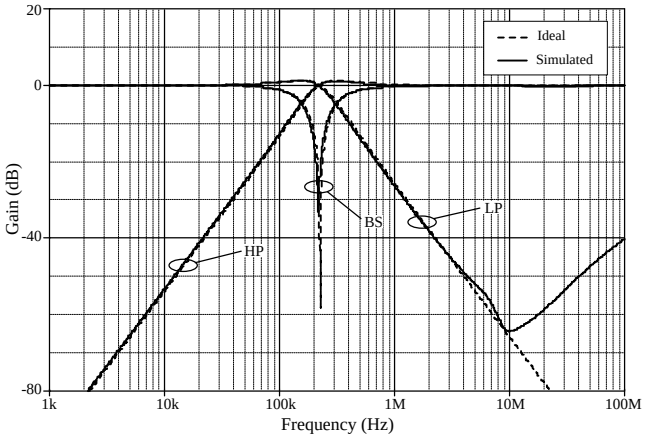

Fig. 10. Frequency characteristics for the LP, HP, and BS responses of Fig. 6(b).

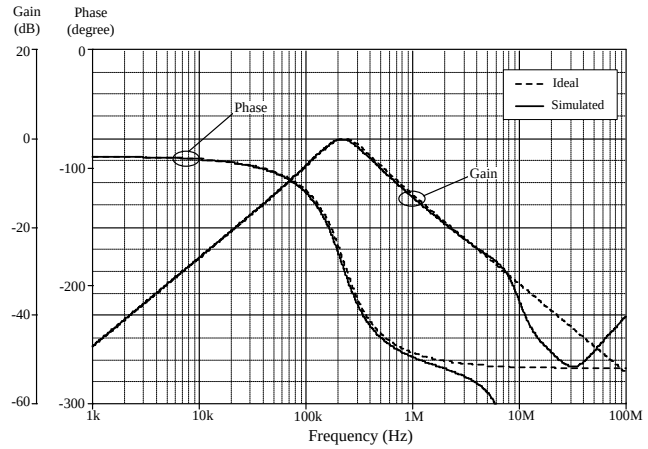

Fig. 11. BP frequency response of Fig. 6(b).

VI. Conclusion

This work has been presented the SFG actualization of nth-order general voltage transfer functions using *n* VDBAs and *n* capacitors. The proposed circuit is canonic in a number of active and passive components and enjoys the ability of electronic tuning. Applications on the first- and second-order filtering function realizations have been provided, which verify the utility of the proposed procedure.

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