A Novel Coupled-Inductor Switched-Capacitor Inverter for High-Gain Boost DC-AC Conversion

Yuen-Haw Chang and Jyun-Jia Liao

***Abstract*—A novel coupled-inductor switched-capacitor inverter (CISCI) is proposed by combining a non-overlapping circuit and sinusoidal pulse-width-modulation (SPWM) controller for the high-gain boost DC-AC conversion and closed-loop regulation. The power part is composed of two cascaded sub-circuits, including: (i) a booster with coupled-inductor and switched-capacitor (one coupled-inductor, 2 pumping capacitor, and one switch controlled by a non-overlapping circuit), and (ii) a half-bridge DC-link inverter (2 capacitors and 2 switches controlled by SPWM), so as to obtain an AC range: +((2+n+nD)/2(1-D))Vs~ -((2+n+nD)/2(1-D))Vs, where D is the duty cycle and n is the turn ratio of coupled-inductor. Practically, the maximum output voltage can reach 12.5 times voltage of source Vs while D=0.5, n=8. Here, the SPWM is employed to enhance regulation capability for the different output amplitude and frequency, as well as robustness to source/loading variation. Finally, the closed-loop CISCI is designed and simulated by OrCAD SPICE for some cases: steady-state and dynamic responses. All results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*—coupled-inductor switched-capacitor inverter, high-gain boost, DC-AC conversion, sinusoidal pulse-width-modulation.**

I. Introduction

Recently years, due to the popularity of mobile devices, e.g. digital camera, e-book, smart phone, notebook, and pad …etc., the power modules of these products always ask for some good characteristics: small volume, light weight, higher efficiency, and better regulation capability. Generally, the traditional power converters have a large volume and a heavy weight because of magnetic elements. Therefore, more manufactures and researchers pay much attention to this topic, and ultimately, requiring DC-DC/DC-AC step-up/down converters realized on a compact chip by mixed-mode VLSI technology.

The switched-capacitor (SC) power converter has received more and more attention because it has only semiconductor switches and capacitors. Thus, this kind of SC converters is one of the good solutions for low-power and high-gain DC-DC/DC-AC conversion. Up to now, the various SC types have been suggested for power conversion. In 1976, Dickson charge pumping was proposed based on a diode-chain structure via pumping capacitors [1]. In 1990s, Ioinovici proposed a SC with two capacitor cells working complementarily, as well as current-mode SC [2][3]. In 2007, Chang proposed a CPLD-based implementation of SC step-down DC-DC converter for multiple output choices [4]. In 2011-2013, Chang *et al*. proposed a series of multistage/ multiphase SC step-up/down DC-DC/DC-AC converter/ inverter [5-8]. In 2013, Chang *et al*. proposed a 2-stage 4-phase switched-capacitor boost DC-AC inverter with sinusoidal PFM control [9]. In 2014, Chang *et al*. proposed a closed-loop high-gain switched-capacitor-inductor-based boost DC-AC Inverter [10].

In order to reach a higher voltage gain, it is one of the feasible ways to adopt the device of coupled-inductor. Nevertheless, the stress on transistors and the volume of magnetic device could be considered. In 2014, Chen *et al*. proposed a coupled-inductor boost integrated flyback converter including high-voltage gain and ripple-free input current [11]. Hamid Bahrami *et al*. suggested a modified step-up boost converter with coupled-inductor and super-lift techniques [12]. In 2015, Chen *et al*. proposed a novel switched-coupled-inductor DC-DC step-up converter and its derivatives [13]. Wu *et al*. proposed a non-isolated high step-up DC-DC converter adopting switched-capacitor cell [14]. Based on the above research, the authors make an attempt on combining SC circuit with one coupled-inductor to propose a closed-loop CISCI here for a higher gain under a fewer element count.

II. Configuration of CISCI

Fig.1 shows the configuration of the closed-loop coupled-inductor switched-capacitor inverter (CISCI) proposed, and it contains two major parts: power part and control part for achieving the high-gain boost DC-AC conversion and closed-loop regulation. These two parts are discussed as follows.

A. Power Part

The power part of this inverter as in upper half of Fig.1 is composed of a coupled-inductor and switched-capacitor booster and a half-bridge DC-link circuit connected in cascaded between supply Vs and output Vout for DC-AC power conversion. This inverter contains coupled-inductor (L_1, L_2), three switches (S_1, Sa, Sb), four pumping capacitors (C_{a1}-C_{a4}), three diodes (D_1-D_3), and one output capacitor (C_L), where it is assumed that $C_{a1}=C_{a2}$ and $C_{a3}=C_{a4}$. The

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Yuen-Haw Chang and Jyun-Jia Liao are with the Department and Graduate Institute of Computer Science and Information Engineering, Chaoyang University of Technology, Taichung, Taiwan, R.O.C. Post code: 413. (e-mail: cyhfyc@cyut.edu.tw, s10327612@gm.cyut.edu.tw).

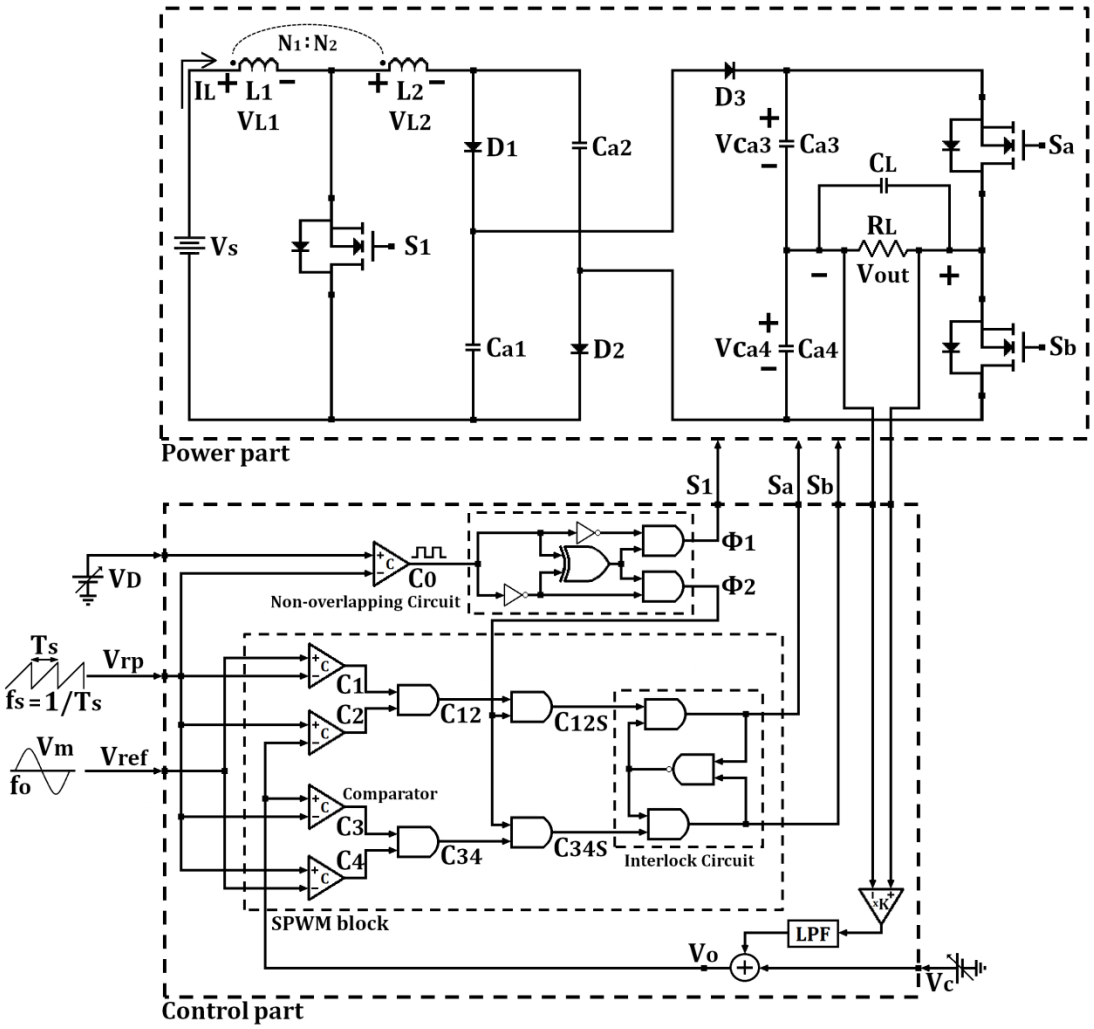

Fig. 1. Configuration of closed-loop CISCI.

coupled-inductor is modeled as an ideal transformer with a turn ratio n ($n=N_2/N_1$). The main function of the booster is to raise the voltage gain between Vs and V_{Ca3} (V_{Ca4}) up to (2+n+nD)/(2(1-D)) at most, where D (0<D<1) is the duty cycle and DTs is the period of charging coupled-inductor in a switching cycle Ts (Ts=1/fs, fs is the switching frequency of control part). And then, by using switches Sa and Sb in the half-bridge DC-link, plus the capacitor voltage V_{Ca3} and V_{Ca4}, the AC output can be achieved for the range of Vout: +((2+n+nD)/(2(1-D)))Vs ~ -((2+n+nD)/(2(1-D)))Vs. Fig.2 shows the theoretical waveforms within a output cycle To (To=1/fo, fo is the output frequency). Here, for the convenience of explanation, an output cycle To contains 20 (or above actually) switching cycle Ts. Each Ts has two Phase: Phase I and II with the different durations DTs and (1-D)Ts. The detailed operations are discussed as follows.

1) Phase I:

During this time interval, S_1 is turned ON and Sa, Sb are turned OFF. Diodes D_3 is turned ON and diodes D_1, D_2 are turned OFF. The relevant topology is shown in Fig. 3(a). The inductor L_1 is charged by source Vs, and the energy is simultaneously transferred from the first side of the coupled-inductor to the secondary side. And then, the inductor L_2 is discharged in series together with C_{a1}-C_{a2} to transfer the stored energy to capacitors C_{a3}-C_{a4} in series.

2) Phase II:

During this time interval, Sa or Sb is turned ON and S_1 is turned OFF. Diodes D_1, D_2 are turned ON and diode D_3 is turned OFF.

(i) While Sa is ON:

The relevant topology is shown in Fig. 3(b). The capacitors C_{a1}-C_{a2} are charged by Vs, V_{L1}, and V_{L2} in series. At the same time, C_{a3} is discharged to supply the energy to C_L and R_L.

(Output range of Vout: $0\sim+\frac{2+n+nD}{2(1-D)}Vs$)

(ii) While Sb is ON:

The relevant topology is shown in Fig. 3(c). The capacitors C_{a1}-C_{a2} are charged by Vs, V_{L1}, and V_{L2} in series. At the same time, C_{a4} is discharged to supply the energy to C_L and R_L.

(Output range of Vout: $0\sim-\frac{2+n+nD}{2(1-D)}Vs$)

Based on the cyclical operations of Phase I and II, the overall step-up gain can reach to the value of (2+n+nD)/2(1-D). Further, with the help of the half-bridge DC-link, the AC output can be realized for the range of +((2+n+nD)/2(1-D))Vs ~ -((2+n+nD)/2(1-D))Vs.

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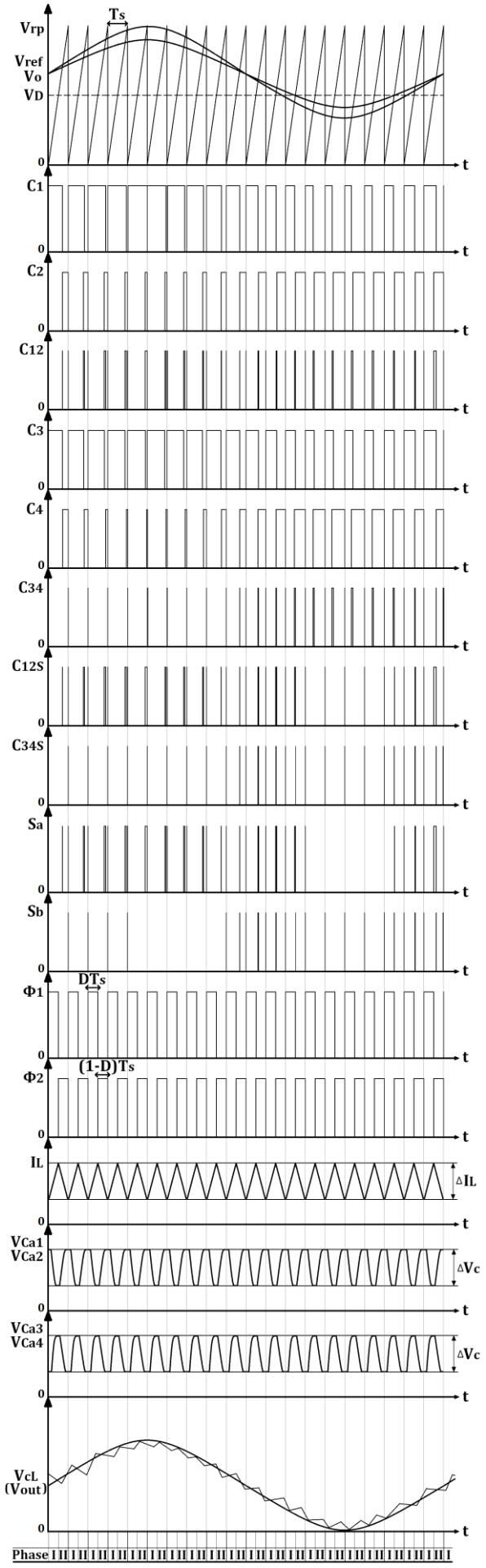

Fig. 2. Theoretical waveforms of CISCI.

B. Control Part

The control part of CISCI is composed of a non-overlapping and SPWM block as in the lower half of Fig. 1. The operations of these two blocks are discussed as follows.

1) Non-overlapping Circuit:

First, an adjustable voltage V_D is compared with a ramp function V_{rp} to generate a non-symmetrical clock signal C_0. And then, this clock is sent to the non-overlapping circuit so as to obtain a set of non-overlapping phase signals Φ_1 and Φ_2. Here, Φ_1 is the driver signal of switch S_1 for charging the coupled-inductor. Thus, D is exactly the on-time ratio (duty cycle) of S_1, and DT_S of Phase I can be regulated by the value of V_D. The main goal is to generate the driver signal of MOSFETs for the different topologies.

2) SPWM block:

From the controller signal flow, the signal V_{out} is attenuated and fed back into the OP-amp low-pass filter (LPF) for high-frequency noise rejection. Next, by using a further DC-shift of V_c, V_o is obtained and compared with the desired output V_{ref} via 4 comparators, and following by using logic-AND to produce a set of control signals C_{12}, C_{34} for realizing SPWM. When e>0 and |e| is raising (e=V_{ref}-V_o), the pulse width of C_{12} is getting bigger. When e<0 and |e| is raising, the pulse width of C_{34} is getting bigger. And then, via the interlock circuit (avoid Sa and Sb being 1 simultaneously) plus coming into the phase of Φ_2, Sa and Sb can be obtained for the SPWM control, and the main goal is to keep V_o on following V_{ref} (sinusoidal reference) to enhance the regulation capability of this proposed inverter. To summarize, based on V_o and V_{ref}, the relevant rules of producing the control/driver signals are listed as below.

1) Φ_1, Φ_2: non-overlapping anti-phase signals from C_0;
   $S_1=\Phi_1$;
2) If $V_D>V_{rp}$, then $C_0=1$; If $V_D<V_{rp}$, then $C_0=0$.
3) If $V_{ref}>V_{rp}$, then $C_1=1$; If $V_{ref}<V_{rp}$, then $C_1=0$;
   If $V_{rp}>V_o$, then $C_2=1$; If $V_{rp}<V_o$, then $C_2=0$;
   If $V_o>V_{rp}$, then $C_3=1$; If $V_o<V_{rp}$, then $C_3=0$;
   If $V_{ref}>V_{rp}$, then $C_4=1$; If $V_{ref}<V_{rp}$, then $C_4=0$;
4) If $C_1=1$ and $C_2=1$, then $C_{12}=1$ (otherwise $C_{12}=0$);
   If $C_3=1$ and $C_4=1$, then $C_{34}=1$ (otherwise $C_{34}=0$);
5) If $C_{12}=1$ and $\Phi_2=1$, then $C_{12S}=1$ (else $C_{12S}=0$);
   If $C_{34}=1$ and $\Phi_2=1$, then $C_{34S}=1$ (else $C_{34S}=0$);
6) SPWM control signals: (^: logic-AND)
   Sa= C_{12S} ^ C_0, for $V_{ref}>V_o$;
   Sb= C_{34S} ^ C_0, for $V_{ref}<V_o$.

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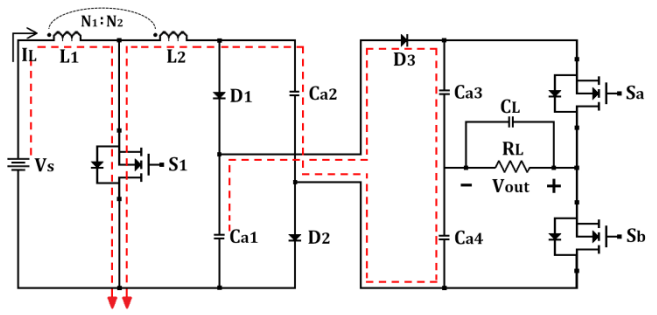

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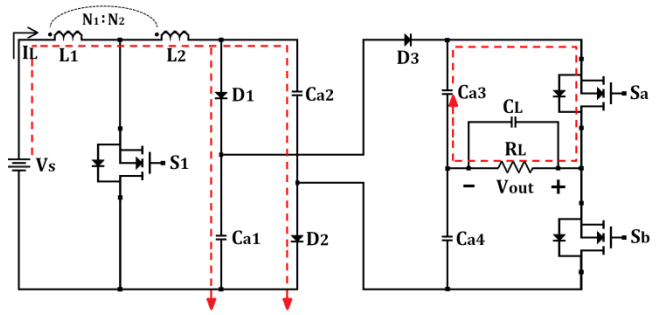

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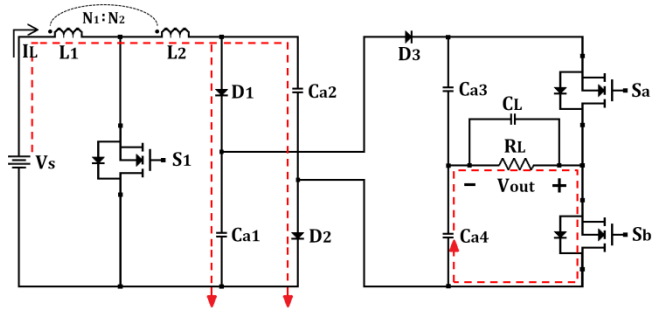


(c)

Fig. 3. Topologies for Phase (a) I, (b) II (Sa:ON), and (b) II (Sb:ON).

III. Examples of CISCI

In this paper, the proposed CISCI is simulated by OrCAD, and all the parameters are listed in TABLE I. There are totally 3 cases for steady-state responses and 4 cases for dynamic responses respectively. Then, these results are illustrated to verify the efficacy of the proposed inverter.

1) Steady-State Responses:

Case 1: fo =60 Hz, Vm =150V

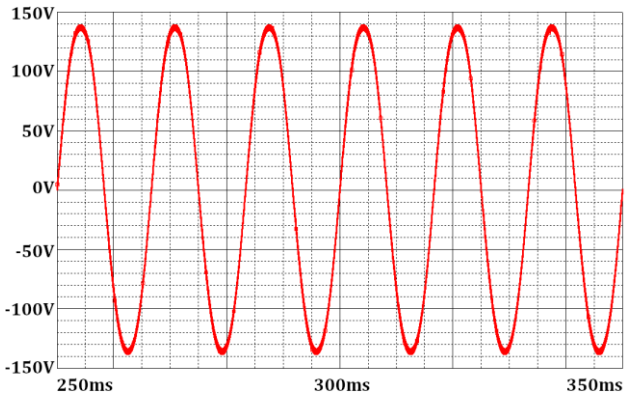
Let the supply source Vs be DC 12V, load RL be 500Ω, and the peak value and output frequency of Vref are Vm =150V, fo=60Hz. The waveform of Vout is obtained as in Fig. 4(a). Vout has the practical peak value of 140V, and the practical output frequency is about 60Hz. The efficiency is 62.5% and THD is 1.858%.

Case 2: fo =60 Hz, Vm =160V

Let the supply source Vs be DC 12V, load RL be 500Ω, and the practical peak value and output frequency of Vref are Vm=160V, fo =60Hz. The waveform of Vout is obtained as in Fig. 4(b). Vout has the peak value of 145V, and the practical output frequency is about 50Hz. The efficiency is 66.25%, and THD is 2.384%.

Case 3: fo =60 Hz, Vm =170V

Let the supply source Vs be DC 12V, load RL be 500Ω, and the practical peak value and output frequency of Vref are Vm=170V, fo =60Hz. The waveform of Vout is obtained as in Fig. 4(c). Vout has the peak value of 150V, and the practical output frequency is about 60Hz. The efficiency is 67.5%, and THD is 3.103%.



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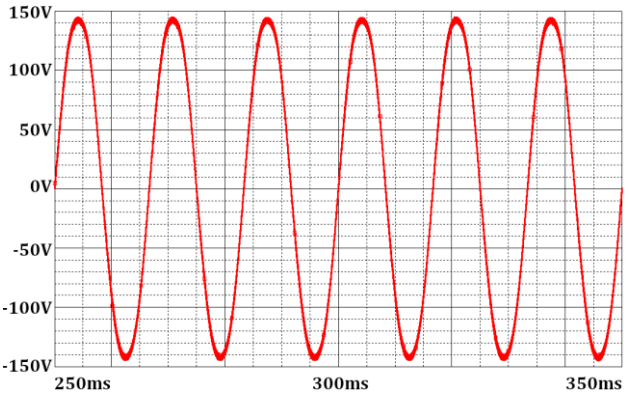

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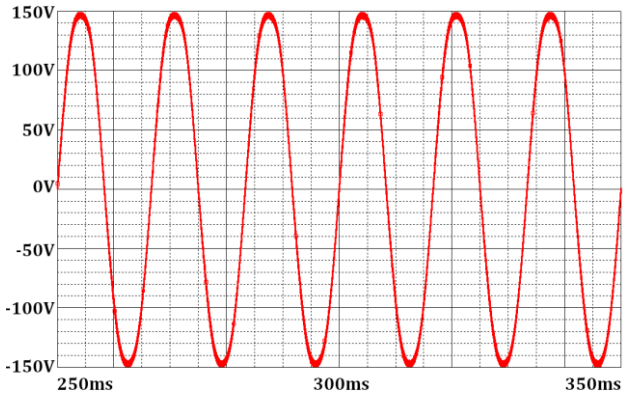

(c)

Fig. 4. Output Vout for Vref: (a) fo=60Hz, Vm=150V; (b) fo=60Hz, Vm=160V; (c) fo=60Hz, Vm=170V.

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TABLE I
Circuit parameters of CISCI.

Supply source (V_S)	12V
Pumping capacitor (C_{a1}, C_{a2})	25μF
Coupled-inductor(L_1, L_2)	100μH, 6400μH (n=8)
Pumping capacitor (C_{a3}, C_{a4})	110μF
Output capacitor (C_L)	1.25μF
Power MOSFETs (S_1, Sa, Sb)	ASW
On-state resistor of MOSFETs (S_1)	50μΩ
On-state resistor of MOSFETs (Sa, Sb)	2.275Ω
Diode (D_1, D_2, D_3)	D1N5822
Load resistor (R_L)	500Ω
Switching frequency (f_S)	50kHz
Output frequency (f_O)	60Hz

2) Dynamic Responses:

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of source voltage, such a variation of source voltage Vs must be considered, as well as variation of load R_L or/and reference Vref (f_O or V_m).

Case 1: VS variation

Assume that Vs is normally at DC 12V, and then it has an instant voltage jump of 12V→10V on 300ms (V_{ref}: f_O=60Hz, V_m=170V). The waveform of Vout is shown as in Fig. 5(a). Obviously, Vout has a slight decrease into about 130V (i.e. 91.93V(RMS)).

Case 2: R_L variation

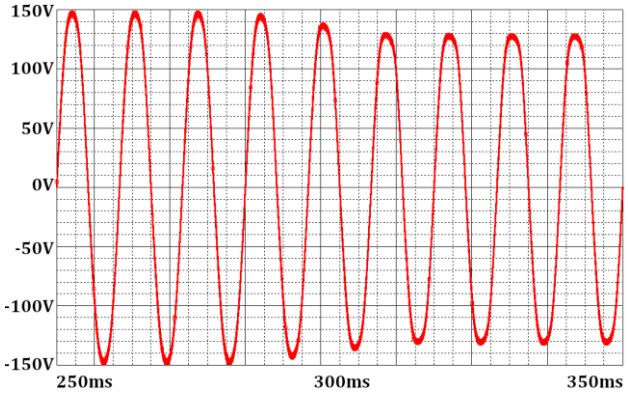
Assume that R_L is 500Ω normally, and it suddenly changes from 500Ω to 250Ω on 300ms (Vref: f_O =60Hz, V_m =170V). Fig. 5(b) shows the transient waveform of Vout at the moment of loading variation. Obviously, Vout has a small drop but Vout can still be following Vref.

Case 3: f_O variation

Assume that the frequency f_O of V_{ref} is 60Hz normally, After a period of 300ms, and it suddenly changes from 60Hz to 40Hz. Fig. 5(c) shows the transient waveform of Vout at the moment of variation: f_O =60Hz→40Hz. Obviously, Vout is still able to follow Vref even the frequency of Vref changes.

Case 4: V_m variation

Assume that V_m is 170V normally, After a period of 300ms, and it changes from 170V to 150V. Fig. 5(d) shows the transient waveform of Vout at the moment of variation: Vm=170V→150V. Obviously, Vout is still able to follow Vref even the amplitude of the desired Vref changes.



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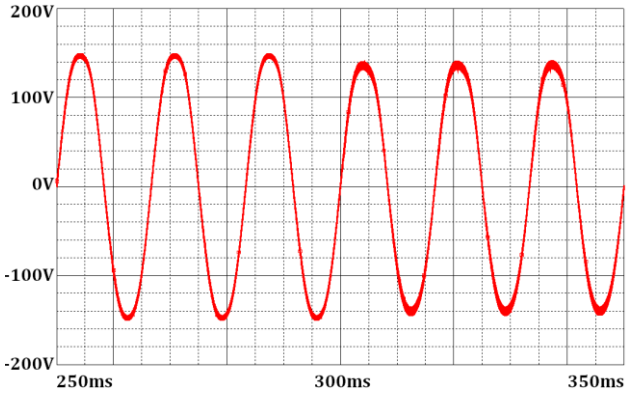

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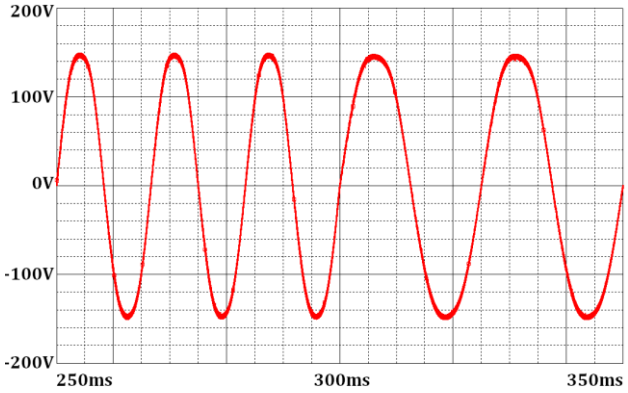

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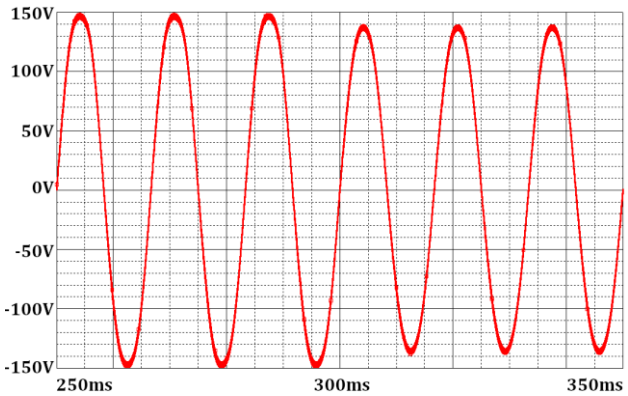

(d)

Fig. 5. Output Vout for the variation of (a) Vs; (b) R_L; (c) fo; (d) Vm.

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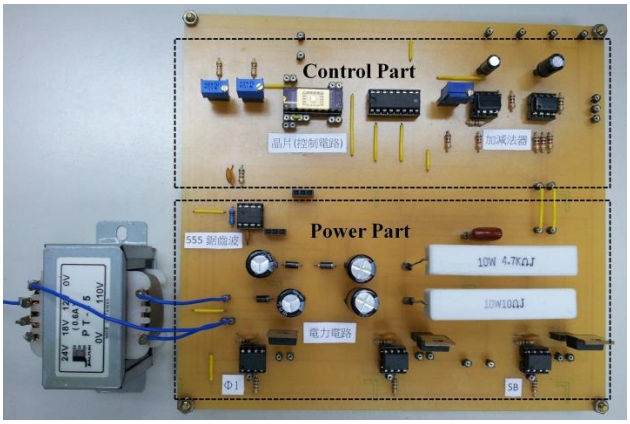

Fig. 6. Prototype circuit of the proposed inverter.

According to the above results, it is obvious that Vout is following Vref for the cases, including Vs source variation, RL loading variation, fo frequency variation, Vm amplitude variation. These results show that this proposed inverter has a good closed-loop dynamic performance.

IV. Conclusion

A novel coupled-inductor switched-capacitor inverter (CISCI) is proposed by combining a non-overlapping circuit and sinusoidal pulse-width-modulation (SPWM) controller for the high-gain boost DC-AC conversion and closed-loop regulation. Finally, the CISCI is designed and simulated, and all results are illustrated to show the efficacy of the proposed scheme. The advantages of the scheme are listed as follows. (i) This CISCI needs just one coupled-inductor element (inductor). Except this, other components (i.e. SC) will be able to be made in IC fabrication future. (ii) This proposed inverter can provide the voltage gain of (2+n+nD)/2(1-D) at most just with 4 pumping capacitors plus one coupled-inductor. (iii) For a higher gain, it can be realized with extending the number of pumping capacitors or increasing the turn ratio of coupled-inductor. (iv) The SPWM technique is adopted not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against source/loading variation. At present, the prototype circuit of this inverter is implemented in the laboratory as shown in the photo of Fig. 6. Some experimental results will be obtained and measured for the verification of the proposed inverter.

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