FDNC Realization and Its Application to FDNR and Filter Realizations

Sasitaporn Theingjit, Tattaya Pukkalanun, Worapong Tangsrirat, *Member, IAENG*

***Abstract*— A simple circuit for the realization of the frequency-dependent negative conductance (FDNC) using active transconductance (G_m) elements is discussed. Based on the realized FDNC as fundamental circuit element, the frequency-dependent negative resistances (FDNR) can also be obtained. The equivalent value of the realized *D* element can be adjusted electronically by means of the transconductance parameters. Both simulator circuits do not require the component-matching condition , and enjoy employing only G_m-cells together with two grounded capacitors; accordingly, they are canonical structures and convenient for integration. Simulation results with TSMC 0.35-μm CMOS technology are presented to validate the characteristics of the realized simulator circuits and application.**

***Keywords*— transconductance cell (G_m-cell), Frequency-Dependent Negative Conductance (FDNC), Frequency-Dependent Negative Resistance (FDNR), immittance function**

I. Introduction

FREQUENCY-dependent negative conductance (FDNC) and frequency-dependent negative resistances (FDNR) are useful active elements in the synthesis and design active ladder filters [1]. They can also be used in the realization of chaotic oscillator circuits [2]. Several realizations of FDNC and FDNR simulators using various types of active building blocks were proposed in the literature [3]-[8]. The circuit of [4] uses three current conveyors, and requires component matching condition. The FDNR simulators in [5]-[6] require at least four passive components. Moreover, they also require matching component. In [7]-[8], floating resistors and capacitors were employed that are not preferable for integrated circuit (IC) implementation point of view.

In literature, it is widely accepted that the transconductances cell or G_m-cells are fundamental circuit elements for the realization of many analog active circuits and systems, especially in the design of modern electronic circuit building blocks, such as CDTA (current differencing transconductance amplifier), CFTA (current follower transconductance amplifier), VDTA (voltage differencing transconductance amplifier), and CCTA (current conveyor transconductance amplifier). They are used in interface circuits, instrumentation amplifiers, and continuous-time-filters. Since the transconductance gain is electronically variable, they can also be applied in automatic, gain control circuits, and analog multipliers. Considering these facts, the realizations of FDNC and FDNR based on the use of only G_m-cells as basic circuit elements has been described in this study. The circuits are realizable by using only G_m-cells and grounded capacitors, without needing passive resistors. It has been shown that the *D*-element values of the realized simulators are controllable electronically through the external biasing currents. In addition, the simulator is tested in an active realization of the third-order Butterworth lowpass ladder filter. To demonstrate the practical workability of the proposed circuits and its applications, simulation results based on TSMC 0.35-μm CMOS process parameters have been provided.

Manuscript received August 28, 2015; revised January 19, 2016.

Sasitaporn Theingjit, Tattaya Pukkalanun, Worapong Tangsrirat, are with the Faculty of Engineering, King Mongkut's Institute of TechnologyLadkrabang (KMITL), Chalongkrung road, Ladkrabang, Bangkok 10520, Thailand. (e-mail : sasitaporn.t@gmail.com , tattap@yahoo.com , worapong.ta@kmitl.ac.th)

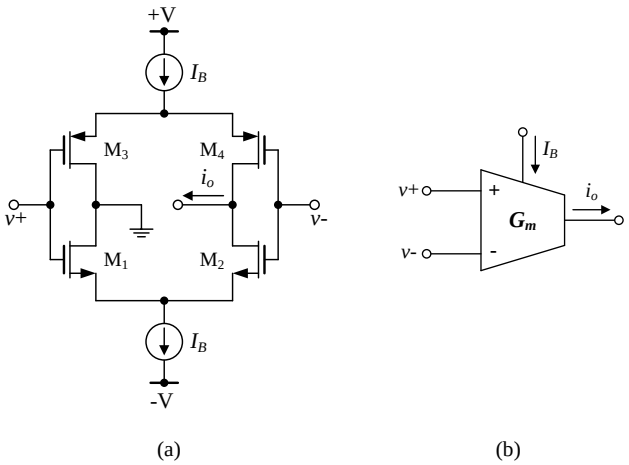


Fig.1 Basic G_m cell.

(a) circuit implementation (b) circuit symbol.

II. Basic G_M-Cell Realization

A particularly simple CMOS realization and the symbol of the tunable G_m-cell, which will be used as a fundamental circuit for implementing the proposed circuit, are shown in Fig.1(a) and 1(b), respectively. The circuit is mainly composed of two Arbel-Goldminz transconductances [9]. For this element, the transconductance value can be determined by the output transistor transconductance, which can be approximated as:

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

$$G_m \cong \left(\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}}\right)+\left(\frac{g_{m3}g_{m4}}{g_{m3}+g_{m4}}\right) \qquad (1)$$

where $g_{mi} = [K_{n(p)}I_B]^{1/2}$ (i = 1, 2, 3, 4) and $K_{n(p)}$ is the transconductance parameter of NMOS (PMOS) transistor and I_B is an external DC bias current of this element, respectively. Note that in eq.(1), the value of G_m is electronically tunable by changing the bias current I_B.

III. FDNC Realization

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{s^2C_1C_2}{G_{m1}G_{m2}G_{m3}} = s^2D \qquad (2)$$

where the D-element value is given by :

$$D = \frac{C_1C_2}{G_{m1}G_{m2}G_{m3}} \qquad (3)$$

From above relation, it is evident that the FDNC is realized, which is electronically controllable by adjusting G_{m1}, G_{m2} and G_{m3}. The circuit comprises only G_m-cell and grounded capacitors; hence, it is suitable for IC fabrication. Moreover, no component matching constraint is required in this realization.

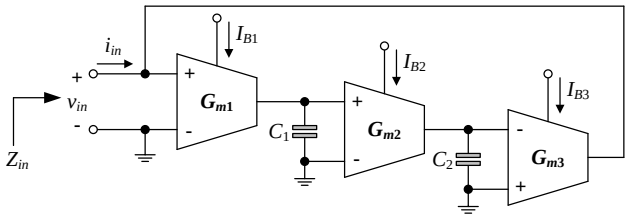


Fig.2 FDNC realization with G_m-cells.

The active and passive sensitivities of the FDNC are obtained as :

$$S^D_{G_{m1}} = S^D_{G_{m2}} = S^D_{G_{m3}} = -1 \qquad (4)$$

and

$$S^D_{C_1} = S^D_{C_2} = 1 \qquad (5)$$

All sensitivity figures are not higher than unity in magnitude. Therefore, the FDNC of Fig.2 exhibits low active and passive sensitivities.

IV. Simulation Results

To evaluate the behavior of the FDNC circuit in Fig.2, PSPICE simulation has been performed using TSMC 0.35-μm CMOS process model parameters. In simulations, the dimensions W(μm)/L(μm) of the MOS transistors are set to be 16.1/0.7 for M_1-M_2, and 28/0.7 for M_3-M_4. The supply voltages used for the proposed simulator circuit are +V = -V = 1.5 V. According to Fig.1, the bias currents (I_Bs) used in simulations are realized by the simple current mirrors.

The impedance-frequency characteristics of the proposed FDNC circuit of Fig.2 for various bias currents are shown in Fig.3. The results were obtained by setting the following passive and active components : $C_1 = C_2$ = 1 nF and $I_B = I_{B1} = I_{B2} = I_{B3}$ ($G_m = G_{m1} = G_{m2} = G_{m3}$). By tuning I_B = 40 μA, 100 μA, and 200 μA, thus the FDNC with D = 18.2 nF/s, 4.7 nF/s and 1.9 nF/s are obtained respectively. It confirms from Fig.3 that the impedance values can be adjusted precisely by changing the biasing current I_B. Also, from Fig.3, the circuit works correctly along the range 20 kHz to 300 kHz, approximately.

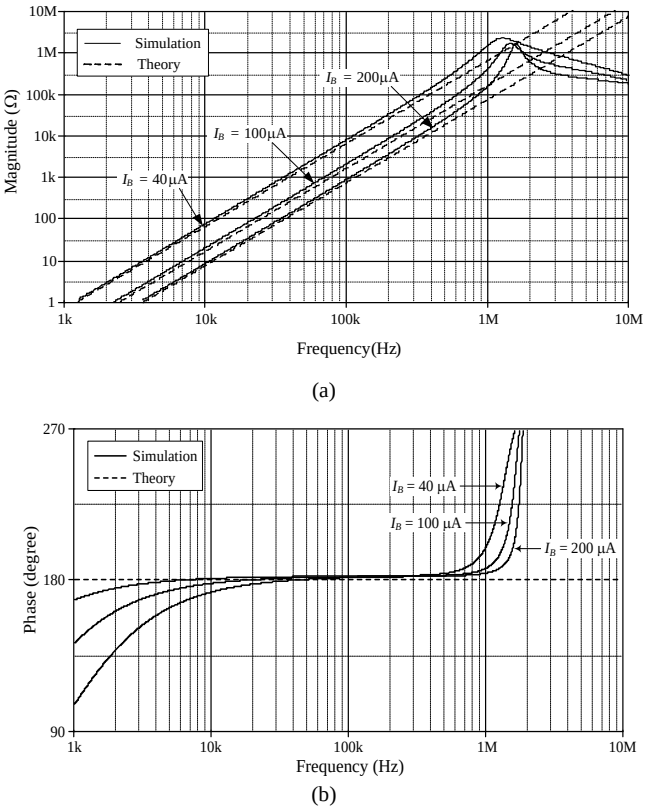


Fig.3 Theory and simulated frequency characteristics for the FDNC circuit of Fig.2.

(a) magnitude responses (b) phase responses

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

V. Application to FDNR Realization

In this section, the generalized circuit topology suitable for grounded FDNR realization is introduced. The introduced topology is depicted in Fig.4. It is based on the FDNC realization shown in Fig.2, where the G_{m4} and G_{m5} behave the variable impedance converter. The circuit has the advantage of using all-grounded capacitors, which enables easy implementation in IC form. The input admittance (Y_{in}) of the circuit is expressed by :

$$Y_{in} = \frac{i_{in}}{v_{in}} = \frac{s^2 C_1 C_2 G_{m4} G_{m5}}{G_{m1} G_{m2} G_{m3}} \tag{6}$$

Thus, the circuit of Fig.4 simulates a grounded FDNR whose its value is obtained as :

$$D = \frac{C_1 C_2 G_{m4} G_{m5}}{G_{m1} G_{m2} G_{m3}} \tag{7}$$

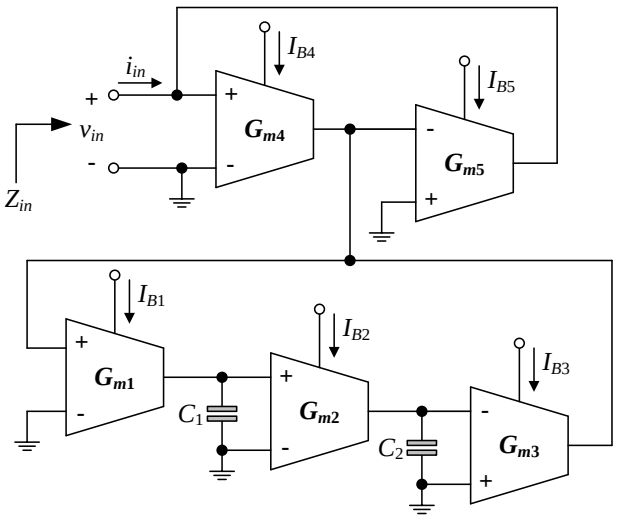
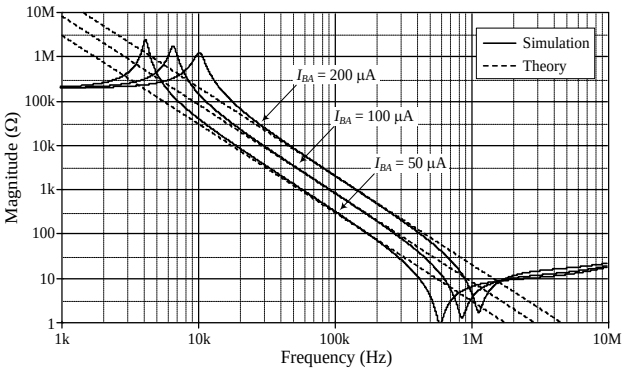
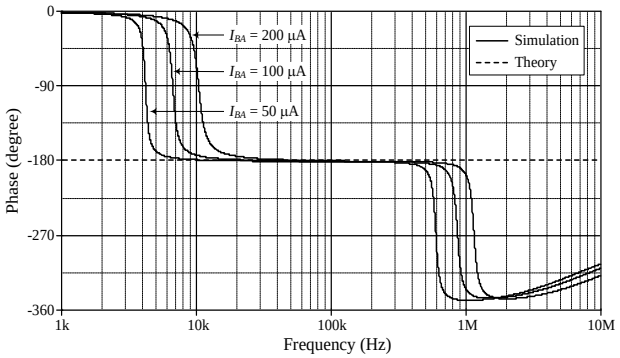


Fig.4 FDNR realization based on FDNC of Fig.2.

In order to demonstrate the performance of the FDNR in Fig.4, it was designed with $C_1 = C_2 = 1$ nF, $I_{BA} = I_{B1} = I_{B2} = I_{B3}$ ($G_{mA} = G_{m1} = G_{m2} = G_{m3}$) and $I_{BB} = I_{B4} = I_{B5}$ ($G_{mB} = G_{m4} = G_{m5}$). In simulations, the circuit was simulated by keeping $I_{BB} = 200$ μA and varying $I_{BA} = 50$ μA, 100 μA, and 200 μA, resulting in $D_{eq} = 8.34$ fF/s, 3.05 fF/s, and 1.24 fF/s, respectively. Fig.5 shows the theory and simulated frequency characteristics of the FDNR simulator of Fig.4 for various I_{BA} values. As demonstrated in both figures, the realized FDNR works perfectly between 20 kHz and 300 kHz. Also note that the simulation results are in close agreement with the prediction values, and confirm that the *D*–element value can be adjusted electronically by the G_m biasing currents.



(a)



(b)

Fig.5 Theory and simulated frequency characteristics for the FDNR circuit of Fig.4.

(a) magnitude responses (b) phase responses

VI. Application to Filter Realization

To illustrate another application of the FDNC realization, the third-order Butterworth lowpass filter was designed and simulated. The normalized RLC passive prototype is shown in Fig.6(a), where $R_s = R_L = 3.18$ kΩ, $L_1 = L_3 = 5$ mH, and $C_2 = 1$ nF [10]. The voltage transfer function of the circuit in Fig.6(a) is given by :

$$\frac{V_L(s)}{V_S(s)} = \frac{1}{s^3\left(\frac{L_1 L_3 C_2}{R_L}\right) + s^2\left(\frac{R_S L_3 C_2}{R_L} + L_1 C_2\right) + s\left(R_S C_2 + \frac{L_1 + L_3}{R_L}\right) + \frac{R_S}{R_L} + 1} \tag{8}$$

By applying Bruton transformation [1] and using variable impedance scaling method with magnitude scaling constant ($k_m = 1.59\times10^3$) and frequency scaling constant ($k_f = 628\times10^3$), the *RLC* passive filter of Fig.6(a) then will have a cutoff frequency of $f_c = 100$ kHz. As a results, the filter is converted into *CRD* filter as shown in Fig.6(b), where the FDNR is realized using the realized circuit of Fig.4. In Fig.6(b), the resulting circuit components are obtained as : $C_{RS} = C_{RL} = 1$ nF, $R_{L1} = R_{L3} = 1.59$ kΩ and $D_2 = 3.18$ fFs. The results of PSPICE simulation of the example filters are also given, verifying the porper operation. Fig.7 shows the magnitude and phase characteristics of the filters in Fig.6. It is seen from Fig.7 that simulation results agree very well with the expectation ones.

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

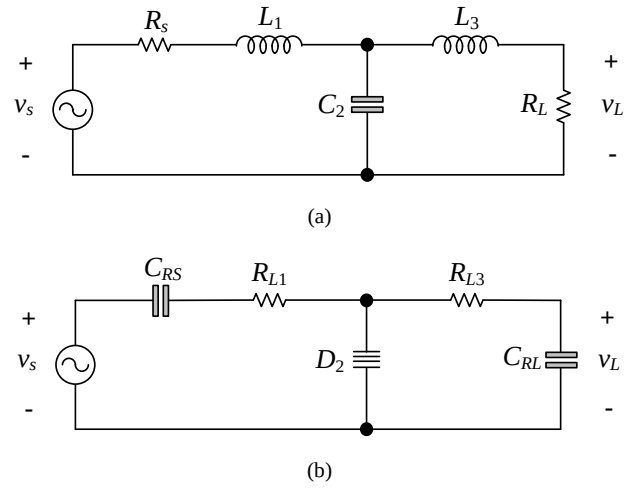


Fig.6 Third-order Butterworth lowpass filter.

(a) RLC passive prototype (b) equivalent CDR circuit with FDNR.

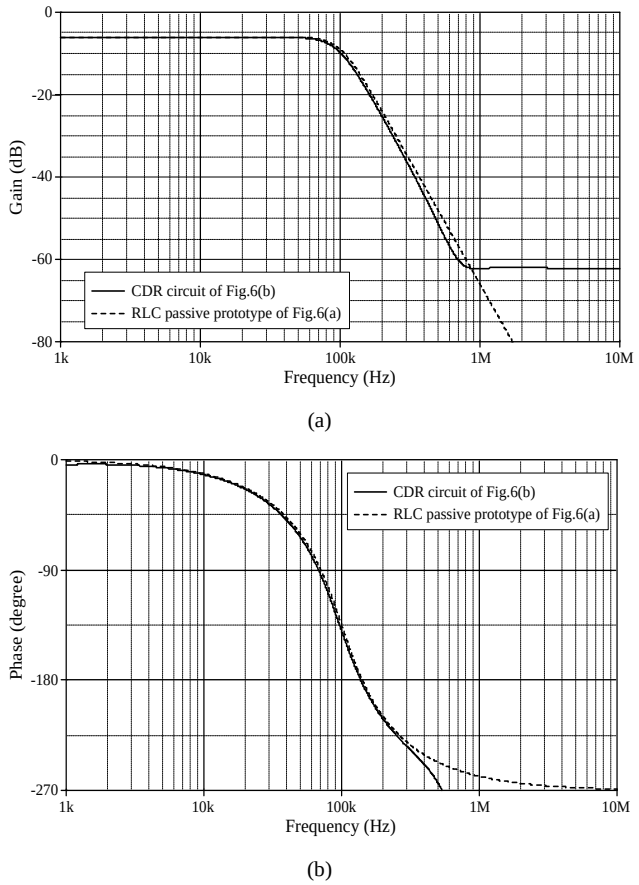


Fig.7 Simulated frequency responses of the filters in Fig.6.

(a) gain responses (b) phase responses.

VII. Conclusions

The simple realization scheme of an electronically tunable FDNC based on G_m-cell technique has been described. The FDNC realization circuit is constructed by only two grounded capacitors as passive elements, resulting in a resistorless structure and suitable for integration. No component matching is needed for its realization. The *D*-element value of the realized FDNC can be tuned electronically through the external bias currents. The described FDNC circuit has been shown to be useful in realizing a FDNR and active ladder filter, respectively. The workability of the realized FDNR is demonstrated on the third-order Butterworth lowpass filter. Simulation results with TSMC 0.35-μm CMOS technology have been provided and the obtained results confirm well the theory.

Acknowledgment

This research work is supported by Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Thailand.

References

[1] L. T. Bruton, "Network transfer functions using the concept of frequency dependent negative resistance", *IEEE Trans. Circuit Theory*, vol.CT-16, pp.406-408, 1969.

[2] A. S. Elwakil, M. P. Kennedy, "Chaotic oscillator configuration using a frequency dependent negative resistor", *J. Circuits Syst. Comp*., vol.9, no.3-4, pp.229-242, 1999.

[3] A. Toker, O. Cicekoglu, H. Kuntman, "New active gyrator circuit suiable for frequency-dependent negative resistor implementation", *Microelectron. J.*, vol.30, pp.59-62, 1999.

[4] M. T. Abuelma'atti, N. A. Tasadduq, "Electronically tunable capacitance multiplier and frequency dependent negative resistance simulator using the current-controlled current conveyor", *Microelectron. J.*, vol.30, pp.869-873, 1999.

[5] E. Yuce, "Floating inductance, FDNR and capacitance simulation circuit employing only grounded passive elements", *Int. J. Electron*., vol93, no.10, pp.679-688, 2006.

[6] C. Psychalinosa, K. Pal, S. Vlassisa, "A floating generalized impedance converter with current feedback operational amplifiers", *Int. J. Electron. Commun. (AEU)*, vol. 62, pp.81-85, 2008.

[7] A. M. Soliman, R. A. Saad, "Two new families of floating FDNR circuits", *J. Electrical Comp. Eng*., vol.2010, Article ID 563761, 7 pages, 2010.

[8] A. Gupta, R. Senani, D. R. Bhaskar, A. K. Singh, "OTRA-based grounded-FDNR and grounded-inductance simulators and their applications", *Circuits Syst. Signal Process.*, vol.31, pp.489-499, 2012.

[9] A. F. Arbel, L. Goldminz, "Output stage for current-mode feedback amplifiers, theory and applications", *Analog Integr. Circ. Sig. Process.*, vol.2, no.3, pp.243–255, 1992.

[10] L. P. Huelman, P. E. Allen, *Introduction to the Theory and Design of Active Filters*, McGraw-Hill, New York, 1980.