Head Loading Control for Hard Disk Drive Process MRAC Technique

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***Abstract*—Head to disk striking is an essential problem in the servo track writing process caused by less dynamic response control. This paper describes head loading control for the hard disk drive process using model reference adaptive (MRAC) technique, in order to decrease the occurrences of the head striking. The introduced technique, discrete time model reference adaptive has an adjustable control mechanism to decrease the deviation of a system output from the output of the reference model so that increase reference tracking performance. The experiment results implemented in self-servo track writer illustrated that the proposed controller design can achieve the effective control performance comparing with the conventional PID control.**

***Index Terms*— Hard Disk Drive, Head loading Control, MRAC**

I. INTRODUCTION

RAMP Ramp load/ unload (L/UL) technology was first introduced in the early 1990's in mobile drives made by PrairieTek and Integral [1], and has been used in a variety of removable disk drives ever since, including all IBM 2.5" drives since 1997. Continuing research and development on L/UL mechanisms has added further benefits, including increased areal density and drive capacity, more efficient power utilization, and superior shock resistance [2, 3]. Unfortunately, during the load/unload process, the effect of various operating parameters, such as load/unload speed, VCM oscillation, ramp height, and friction, continue to hold back Ramp L/UL performance [4–6]. back Ramp L/UL performance [4–6].

In this paper, we concentrate on problems with the VCM velocity profile, particularly the response of the head loading process, which varies according to the non-linear characteristics of the system under control. Improper VCM velocity affects slider attitude, reducing its flying height (FH) and causing head-disk interface (HDI) problems in servo track writing, which in turn impacts production cost and time.

To address this problem, we propose a design scheme for discrete-time model reference adaptive control of the ramp loading process.

The model reference adaptive control technique was first introduced by Whitacker in 1958. The structure of adaptive systems and the mechanisms used for the adaptation of unknown or variable parameters create a degree of nonlinearity in the controlled system. Since the 1960s, MRAC theory has been developed extensively, with several continuous-time and discrete-time [7–21] MRAC algorithms applied to control systems, including Mechatronics And Automation Control [22–24], Process Control [25], Power system Control [26], etc. A number of schemes for designing adaptive laws for such systems have also been introduced, including the sensitivity model [27], stability theory of Lyapunov [28, 29] and PoPov's hyperstability concepts [30].

This paper describes head loading control for the hard disk drive process using model reference adaptive (MRAC) technique, in order to decrease the occurrences of the head striking. The introduced technique, discrete time model reference adaptive has an adjustable control mechanism to decrease the deviation of a system output from the output of the reference model so that increase reference tracking performance. The experiment results implemented in self-servo track writer illustrated that the proposed controller design can achieve the effective control performance comparing with the conventional PID control.

This paper is organized as follows: in section II, we describe an overview of L/UL control systems; in section III, we present our methodology for our DTMRAC discrete-time model reference adaptive control; in section IV, we detail the setup and results of our performance evaluation; and in section V, we offer concluding remarks.

II. LOAD/UNLOAD CONTROL SYSTEM

A. Hardware

The hard drive head's L/UL control system diagrammed in Fig. 1 includes VCM and Load/Unload mechanical structures, a VCM power driver, velocity control processor, signal converter and embedded firmware. The input of the control system is the voltage to the VCM driver and the output is an L/UL head velocity. For our research, we used voltage generated by the VCM back electromotive force (Vbemf), which is proportional to the VCM rotating velocity, as the measurement signal to control the load/unload head velocity.

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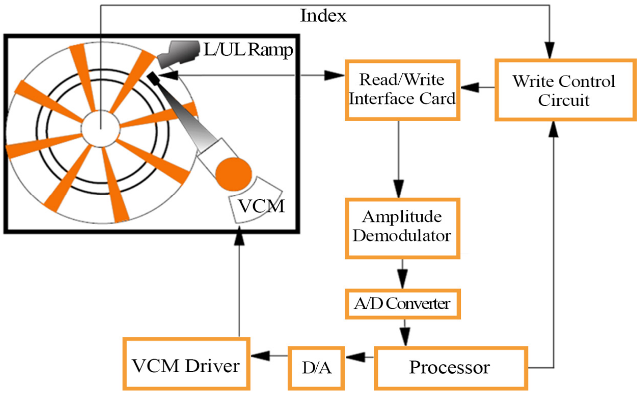

Fig. 1. Head Loading in SSTW Proces Diagram.

B. System Model

The ramp load disk drive actuator can be described by a combination of mechanical and electrical dynamic equations. The mechanical dynamics are given by

$$J\ddot{x} = K_t i, \tag{1}$$

where x is the actuator arm position (mm), J is the actuator inertia (g-mm^2), and i the current applied in the coil (amp). K_t is a torque factor (N-mm/amp). The electrical dynamics are represented by

$$V_s = Ri + L\frac{di}{dt} + V_b, \tag{2}$$

where R and L are specified as the coil resistance (ohm) and inductance (mH), respectively, V_s is the supply voltage control signal available as input to the system, and $V_b = K_t\dot{x}$ is the back electro-motive force.

For hard disk drive ramp loading control, the process transfer function is obtained by choosing the state $x_1 = x, x_2 = \dot{x}, x_3 = i$ and providing the control input as $u = V_s$. The system can be illustrated in state-space form as

$$\begin{aligned} \dot{x} &= Ax + Bu, \\ y &= Cx, \end{aligned} \tag{3}$$

where

$$A = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & K_t / J \\ 0 & -K_t / L & -R / L \end{bmatrix}, B = \begin{bmatrix} 0 \\ 0 \\ 1/L \end{bmatrix}, C = \begin{bmatrix} 0 & 1 & 0 \end{bmatrix}$$

III. METHODOLOGY FOR DISCRETE TIME MODEL REFERENCE ADAPTIVE CONTROL (DTMRAC)

A. Controller Design

The MRAC may be regarded as an adaptive servo system in which the desired performance is expressed in terms of a reference model, which creates the required response to the input signal. A block diagram of the MRAC control system is depicted in Fig. 2.

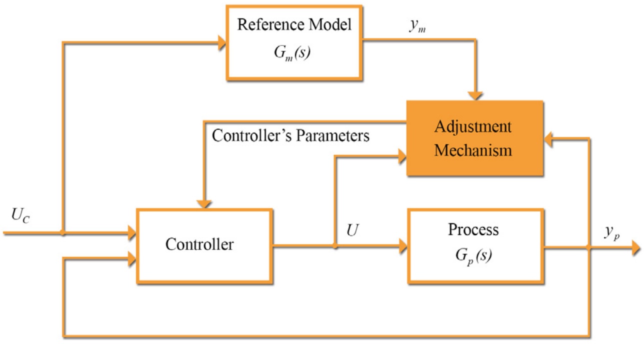

Fig. 2. Model Reference Adaptive Control (MRAC) Control System.

MRAC control system is the feedback loop composed of the controller, the process and additional feedback loop which adjusts the controller parameters. The parameters of controller are adjusted on the basis of feedback from the error, which is the deviation between the output of the system and the output of the reference model.

$$J(kT,\theta) = \frac{1}{2}e^2(kT,\theta) \tag{4}$$

where $e(kT,\theta) = y(kT,\theta) - y_m(kT)$ is the error between the system output and the output of reference model. So as to minimize the performance index, the parameter vector θ of the adjustable controller has to change in the direction opposite the gradient $\frac{\partial J}{\partial \theta}$. Thus, the adaptation law in discrete form is

$$\begin{aligned} \theta(kT+T) &= \theta(kT) - \gamma\frac{\partial J(kT,\theta)}{\partial \theta} \\ &= \theta(kT) - \gamma e(kT,\theta)\frac{\partial e(kT,\theta)}{\partial \theta} \end{aligned} \tag{5}$$

where the components of $\frac{\partial e(kT,\theta)}{\partial \theta}$ are the sensitivity derivatives of the error with respect to θ, and the γ parameter is an adaptation gain.

For the transfer function of the third order process described by

$$\begin{aligned} y_p(k) = &-a_2 y(k-1) - a_1 y(k-2) - a_0 y(k-3) \\ &+ b_2 u(k-1) + b_1 u(k-2) + b_0 u(k-3) \end{aligned} \tag{6}$$

We first perform the z-transform of both sides of the difference equation.

$$\mathrm{Z}\{y(k)\} = \mathrm{Z}\begin{bmatrix} -a_2 y(k-1) - a_1 y(k-2) - a_0 y(k-3) \\ +b_2 u(k-1) + b_1 u(k-2) + b_0 u(k-3) \end{bmatrix} \tag{7}$$

$$H(z) = \frac{y_p(z)}{u(z)} = \frac{b_2 z^2 + b_1 z^1 + b_0}{z^3 + a_2 z^2 + a_1 z^1 + a_0} \tag{8}$$

where $H(z)$ is the z-transfer function from u to y_p.

A block diagram for this adaptive system based on MIT rule is illustrated in Fig. 2. The closed loop transfer function becomes

$$\frac{y_p(z)}{u_c(z)} = \frac{b_{c4}z^4 + b_{c3}z^3 + b_{c2}z^2 + b_{c1}z + b_{c0}}{z^5 + a_{c4}z^4 + a_{c3}z^3 + a_{c2}z^2 + a_{c1}z + a_{c0}} \quad (9)$$

where

$$b_{c4} = b_2\left(K_p + K_i + K_d\right)$$
$$b_{c3} = b_1K_d - 2b_2K_d + b_1K_i + b_1K_p - b_2K_p$$
$$b_{c2} = b_0K_d - 2b_1K_d + b_2K_d + b_0K_i + b_0K_p - b_1K_p$$
$$b_{c1} = b_1K_d - 2b_0K_d - b_0K_p$$
$$b_{c0} = b_0K_d$$
$$a_{c4} = a_2 + b_2K_d + b_2K_i + b_2K_p - 1$$
$$a_{c3} = a_1 - a_2 + b_1K_d - 2b_2K_d + b_1K_i + b_1K_p - b_2K_p$$
$$a_{c2} = a_0 - a_1 + b_0K_d - 2b_1K_d + b_2K_d + b_0K_i + b_0K_p - b_1K_p,$$
$$a_{c1} = b_1K_d - 2b_0K_d - a_0 - b_0K_p$$
$$a_{c0} = b_0K_d\,.$$

The control aim is for changing value of the plant output y_p according to the output of the reference model y_m. The transfer function of reference model is specified as

$$H_m(z) = \frac{y_m(z)}{u_c(z)} = \frac{b_{m4}z^4 + b_{m3}z^3 + b_{m2}z^2 + b_{m1}z^1 + b_{m0}}{z^5 + a_{m4}z^4 + a_{m3}z^3 + a_{m2}z^2 + a_{m1}z^1 + a_{m0}}\,. \quad (10)$$

According to the procedure of adaptive controller design, we then apply the MIT gradient rules for calculating parameters of PID controller, is given in (11) ~ (16):

$$\begin{aligned} K_p(kT+T) &= K_p(kT) - \gamma_p\frac{\partial J}{\partial K_p} \\ &= K_p(kT) - \gamma_p\left(\frac{\partial J}{\partial \varepsilon}\right)\left(\frac{\partial \varepsilon}{\partial y_p}\right)\left(\frac{\partial y_p}{\partial K_p}\right) \end{aligned} \quad (11)$$

$$\begin{aligned} K_i(kT+T) &= K_i(kT) - \gamma_i\frac{\partial J}{\partial K_i} \\ &= K_i(kT) - \gamma_i\left(\frac{\partial J}{\partial \varepsilon}\right)\left(\frac{\partial \varepsilon}{\partial y_p}\right)\left(\frac{\partial y_p}{\partial K_i}\right) \end{aligned} \quad (12)$$

$$\begin{aligned} K_d(kT+T) &= K_d(kT) - \gamma_d\frac{\partial J}{\partial K_d} \\ &= K_d(kT) - \gamma_d\left(\frac{\partial J}{\partial \varepsilon}\right)\left(\frac{\partial \varepsilon}{\partial y_p}\right)\left(\frac{\partial y_p}{\partial K_d}\right) \end{aligned} \quad (13)$$

where $\partial J/\partial\varepsilon = \varepsilon$, $\partial\varepsilon/\partial y = 1$, and $D = d/dt$

$$\frac{\partial y_p}{\partial K_p} = \left[\begin{array}{c} \dfrac{b_2D^4 + (b_1 - b_2)D^3 + (b_0 - b_1)D^2 - b_0D}{D^5 + a_{c4}D^4 + a_{c3}D^3 + a_{c2}D^2 + a_{c1}D + a_{c0}} \\ \cdot\left[U_c - y_p\right] \end{array}\right] \quad (14)$$

$$\frac{\partial y_p}{\partial K_i} = \left[\begin{array}{c} \dfrac{b_2D^4 + b_1D^3 + b_0D^2}{D^5 + a_{c4}D^4 + a_{c3}D^3 + a_{c2}D^2 + a_{c1}D + a_{c0}} \\ \cdot\left[U_c - y_p\right] \end{array}\right] \quad (15)$$

$$\frac{\partial y_p}{\partial K_d} = \left[\begin{array}{c} \dfrac{b_2D^4 + (b_1 - 2b_2)D^3 + (b_0 - 2b_1 + b_2)D^2 + (b_1 - 2b_0)D + b_0}{D^5 + a_{c4}D^4 + a_{c3}D^3 + a_{c2}D^2 + a_{c1}D + a_{c0}} \\ \cdot\left[U_c - y_p\right] \end{array}\right] \quad (16)$$

From (14), (15) and (16), we obtain $\dfrac{\partial K_p}{\partial t}, \dfrac{\partial K_i}{\partial t}, \dfrac{\partial K_d}{\partial t}$ as given in (17), (18) and (19) respectively:

$$\begin{aligned} K_p(kT+T) - K_p(kT) &= -\gamma_p\frac{\partial J}{\partial K_p} \\ &= -\gamma_p\varepsilon\left[\begin{array}{c} \dfrac{b_2D^4 + (b_1 - b_2)D^3 + (b_0 - b_1)D^2 - b_0D}{D^5 + a_{c4}D^4 + a_{c3}D^3 + a_{c2}D^2 + a_{c1}D + a_{c0}} \\ \cdot\left[U_c - y_p\right] \end{array}\right] \end{aligned} \quad (17)$$

$$\begin{aligned} K_i(kT+T) - K_i(kT) &= -\gamma_i\frac{\partial J}{\partial K_i} \\ &= -\gamma_i\varepsilon\left[\begin{array}{c} \dfrac{b_2D^4 + b_1D^3 + b_0D^2}{D^5 + a_{c4}D^4 + a_{c3}D^3 + a_{c2}D^2 + a_{c1}D + a_{c0}} \\ \cdot\left[U_c - y_p\right] \end{array}\right] \end{aligned} \quad (18)$$

$$\begin{aligned} K_d(kT+T) - K_d(kT) &= -\gamma_i\frac{\partial J}{\partial K_d} \\ &= -\gamma_d\varepsilon\left[\begin{array}{c} \dfrac{b_2D^4 + (b_1 - 2b_2)D^3 + (b_0 - 2b_1 + b_2)D^2 + (b_1 - 2b_0)D + b_0}{D^5 + a_{c4}D^4 + a_{c3}D^3 + a_{c2}D^2 + a_{c1}D + a_{c0}} \\ \cdot\left[U_c - y_p\right] \end{array}\right] \end{aligned} \quad (19)$$

IV. EXPERIMENTAL RESULTS AND ANALYSIS

A. Servo Track Writer

To validate the performance of the proposed controller design, the experimental system composes of

--Hard drive self-servo track writer with a ramp L/UL mechanism.

--PH4LC card, Altera Cyclone II FPGA, running version EP2C15 to control the system.

--Master PC for programming FPGA and analysis of signal data. The programming is an applied OOP language compiled and run with an STWHost program and using an ethernet connection between the computer and the PH4LC card.

--Golden unit 2.5" hard drive.

Head U/UL processes were executed by commands from the STWHost and STW Console program on the Master PC. The excitation signal and the measured signal from unloading control were saved in *.dat file for further analysis using MATLAB.

B. Results and Analysis

Refering to performance requirements, head loading velocities must be effectively controlled to prevent head to disk interaction. The desired head loading velocities must track the reference input amplitude at 350mm/sec, which can be achieved without head-disk interaction. The ramp loading maneuver must also execute within the 11V saturation voltage of the amplifier. Thus, the reference model took the following form:

$$\frac{y_m(z)}{u_c(z)} = \frac{6.70\text{e-}005z^4 - 7.29\text{e-}005z^3 - 6.11\text{e-}005z^2 + 5.69\text{e-}006z^1 - 1.26\text{e-}007}{z^5 - 3.99z^4 + 5.99z^3 - 3.99z^2 + 0.99z^1 - 1.26\text{e-}007} \tag{20}$$

The structure of the adaptive control system has already been provided in Fig. 3, and the experimental parameters are shown in Table I. Finally, the compiled codes for the new control algorithm were loaded into the Altera Cyclone PH4LC card.

TABLE I
PARAMETER VALUES OF DTMRAC SYSTEM.

Symbol	Quantity	Value
γ_{p1}, γ_{p2}	adaptation gain P	0.002, 0.043
γ_{i1}, γ_{i2}	adaptation gain I	0.035, 0.039
γ_{d1}, γ_{d2}	adaptation gain D	0.041, 0.052

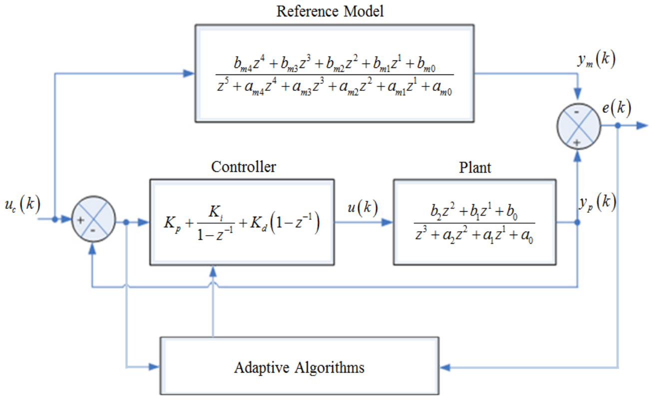

Fig. 3. Block Diagram of Discrete Time Model Reference Adaptive Control System.

The performance of discrete time model reference adaptive control for ramp loading process in hard disk drive is shown in Fig. 6 and 8 compared with conventional PID in Fig. 4. The figures show satisfied value of the loading velocity and VCM voltage saturation. Furthermore, the maximum overshoot of loading velocity was decreased by adaptation gain adjustment.

In the results figures, it is clear that the VCM Velocity response of the proposed ramp load control using the DTMRAC technique. The improved control performance of the DTMRAC control system is especially pronounced when compared to that of conventional PID shown in Fig. 4. Clearly, the controller shows lower VCM oscillation in head to disk interaction prior to head loading.

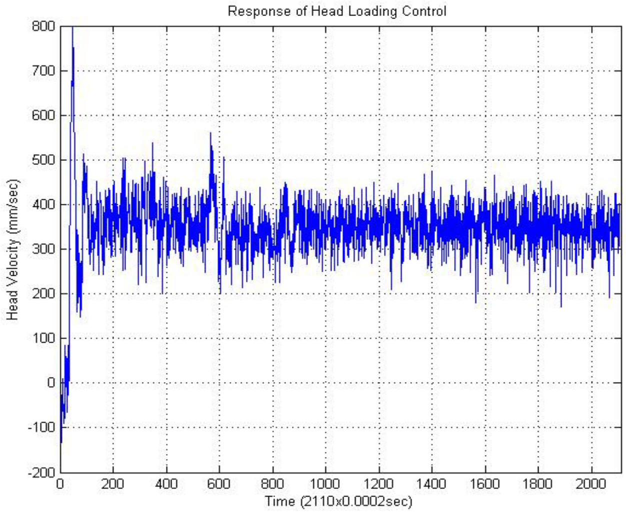

Fig. 4. The Response of Conventional- PID Control for VCM Velocity in SSTW Process.

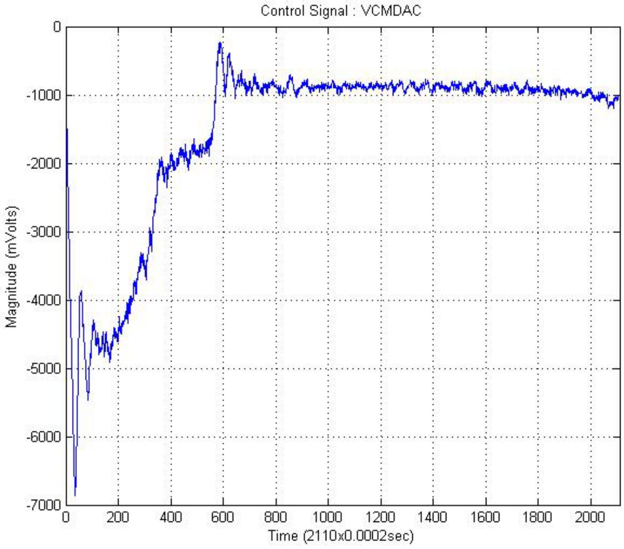

Fig. 5. Conventional- PID Control Signal.

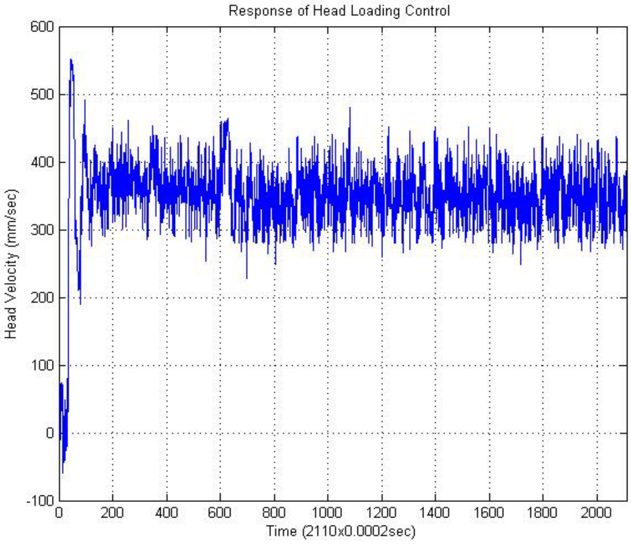

Fig. 6. The Response of DTMRAC $(\gamma_{p1}, \gamma_{i1}, \gamma_{d1}, \varepsilon_1)$ for VCM Velocity in SSTW Process.

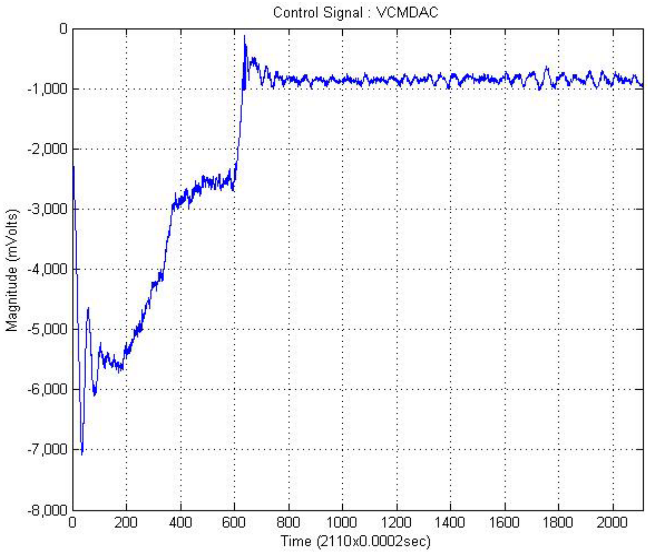

Fig. 7. DTMRAC $\left(\gamma_{p1}, \gamma_{i1}, \gamma_{d1}, \varepsilon_1\right)$ Control Signal.

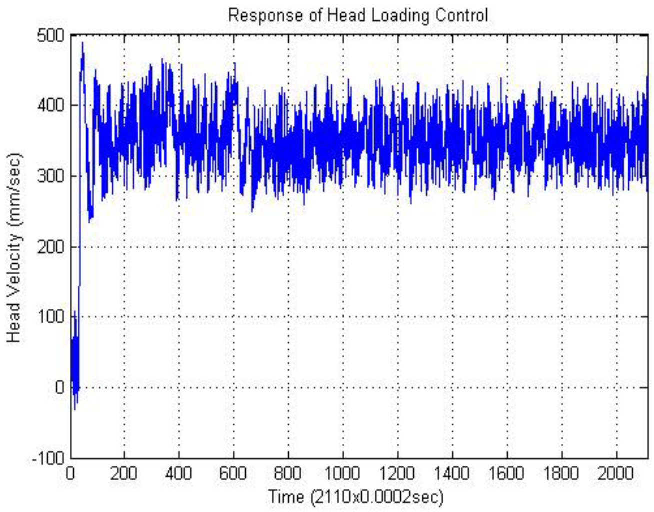

Fig. 8. The Response of DTMRAC $\left(\gamma_{p2}, \gamma_{i2}, \gamma_{d2}, \varepsilon_2\right)$ for VCM Velocity in SSTW Process.

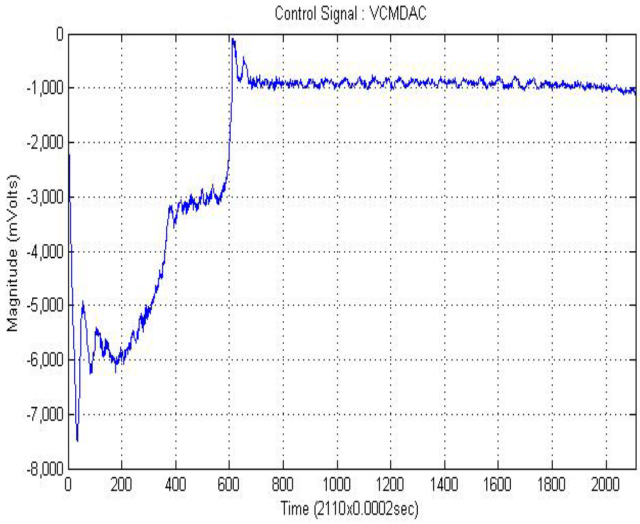

Fig. 9. DTMRAC $\left(\gamma_{p2}, \gamma_{i2}, \gamma_{d2}, \varepsilon_2\right)$ Control Signal.

The reference tracking performance exhibited in Figures 8 and 9 reflects the adaptive control strategy. The velocity error decreased as expected while large overshoot at the beginning of the velocity profile has been decreased. Figure 10 shows that the ramp loading control are executed within the acceptable range of 11V saturation voltage of the amplifier. Repeatability was investigated by completing 50 consecutive loading cycles without failure.

V. CONCLUSION

We successfully implemented the model reference adaptive control system for hard disk drive head loading processes using MIT rule adaptive mechanism. We then conducted experiments on the self-servo track writer PH4LC unit to verify the performance of the proposed ramp loading controller. The results demonstrated the clear superiority of our controller to conventional PID controls. With the MRAC control strategy, the VCM velocity profile remained within 500 mm/sec, while the maximum overshoot of transient response was decreased. The repeatability of these results was verified by completing 50 consecutive loading cycles without failure. Our preliminary conclusion is that the proposed control scheme is fully sufficient to solving unwanted head-to-disk contact problem while the servo track writing process.

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