A Simple Switched-Coupled-Inductor Inverter for Boost DC-AC Conversion and Closed-Loop Regulation

Yuen-Haw Chang, Kai-Lin Hsu, and Dian-Lin Ou

***Abstract*—This paper presents a simple configuration of a closed-loop switched-coupled-inductor inverter (SCII) by combining a non-overlapping phase generator and a sinusoidal pulse-width-modulation (SPWM) controller in order to realize boost DC-AC conversion and low-power regulation. The power part is composed of two sub-circuits between supply V_S and output V_{OUT}, including: (i) a switched-copuled-inductor booster (one coupled inductor, two pumping capacitors, and one switch regulated by the phase generator circuit), and (ii) a half-bridge DC-link inverter (one filter capacitor, a load resistor, and two switches controlled by the SPWM controller), so as to obtain the maximum range of AC output: $+[(1+nD)/(1-D)]V_S \sim -nV_S$, where n is the turn ratio of the coupled inductor and D is duty cycle of charging this inductor. Practically, while D=0.42 and n=6, a symmetrical sinusoidal output: AC 100V_{RMS}, 60Hz can be obtained at the supply of DC 24V. Besdies, the SPWM is employed to enhance regulation capability for the different output amplitude and frequency, as well as robustness to source or loading variation. Finally, the closed-loop SCII is designed and simulated by SPICE for some cases of steady-state and dynamic responses. All results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*—switched-coupled-inductor inverter, boost DC-AC conversion, cloased-loop regulation, sinusoidal pulse-width-modulation.**

I. Introduction

Last several years, boost power converters for DC-DC or DC-AC are widely applied when a circuit or module has just a low-voltage source available, such as lighting device, smart phone, and medical equipment… etc. They are always required to be with some good characteristics, including small volume, light weight, high conversion efficiency, and robust regulation capability. Generally, the conventional converters have a larger volume and a heavier weight due to magnetic elements. Therefore, more manufactures and researchers pay attention to this topic, and ultimately aiming for DC-DC/ DC-AC step-up converters realized on a compact chip by mixed-mode VLSI technology.

This kind of switched-capacitor (SC) power converters, including only capacitors and MOSFET switches, is one of the good solutions to provide a high voltage gain for realizing the boost DC-DC/DC-AC conversion in the non-magnetic circuit. Up to now, the various SC types have been suggested. In 1976, Dickson charge pumping was proposed based on a diode-capacitor chain structure [1]. In 1990s, Ioinovici *et al*. proposed some SC schems with two capacitor cells working in anti-phase by voltage/current mode [2-3]. In 2007, Chang proposed a CPLD-based implementation of SC step-down DC-DC converter for multiple output choices [4]. In 2011-2013, Chang *et al*. proposed a series of multistage/ multiphase SC step-up/down DC-DC converter or DC-AC inverter [5-8]. In 2014, Chang *et al*. proposed a two-stage four-phase SC-based boost DC-AC inverter with sinusoidal PFM [9]. In 2015, Chang *et al*. proposed a closed-loop high-gain switched-capacitor-inductor-based boost DC-AC inverter [10].

For a higher voltage gain, it is one of the good ways to take advantage of turn ratio and/or extra winding stage of coupled inductor. But, the stress on transistors and the volume of magnetic device must be considered. In 2015, Chen *et al*. proposed a high-gain and input-current-ripple-free boost integrated flyback converter including coupled inductor [11]. Bahrami *et al*. suggested a modified step-up boost converter with coupled-inductor and super-lift techniques [12]. Chen *et al*. proposed a novel switched-coupled-inductor DC-DC step-up converter and its derivatives [13]. Wu *et al*. proposed a nonisolated high step-up DC-DC converter via adopting switched-capacitor cell [14]. Nouri *et al*. proposed an interleaved high-gain step-up DC-DC converter based on three-winding coupled-inductor and voltage-multiplier cell [15]. In 2016-2017, Chang *et al*. proposed a novel coupled-inductor switched-capacitor boost DC-AC inverter, and then plus a four-stage SC, presented a high-gain serial-parallel-switched-capacitor coupled-inductor inverter [16-17]. Here, under the consideration of circuit complexity reduction, the authors attempt to propose a simple SCII scheme for boost DC-AC conversion and closed-loop regulation.

II. Configuration of SCII

Fig. 1 shows the simple closed-loop switched-coupled-inductor inverter (SCII) proposed, and it contains two major parts: power and control part for achieving the boost DC-AC conversion and closed-loop regulation. These two parts are discussed as follows.

A. Power Part

The power part of this inverter as in the upper half of Fig. 1 contains two sub-circuits: (i) a switched-coupled-inductor booster and (ii) a half-bridge DC-link inverter, which are in

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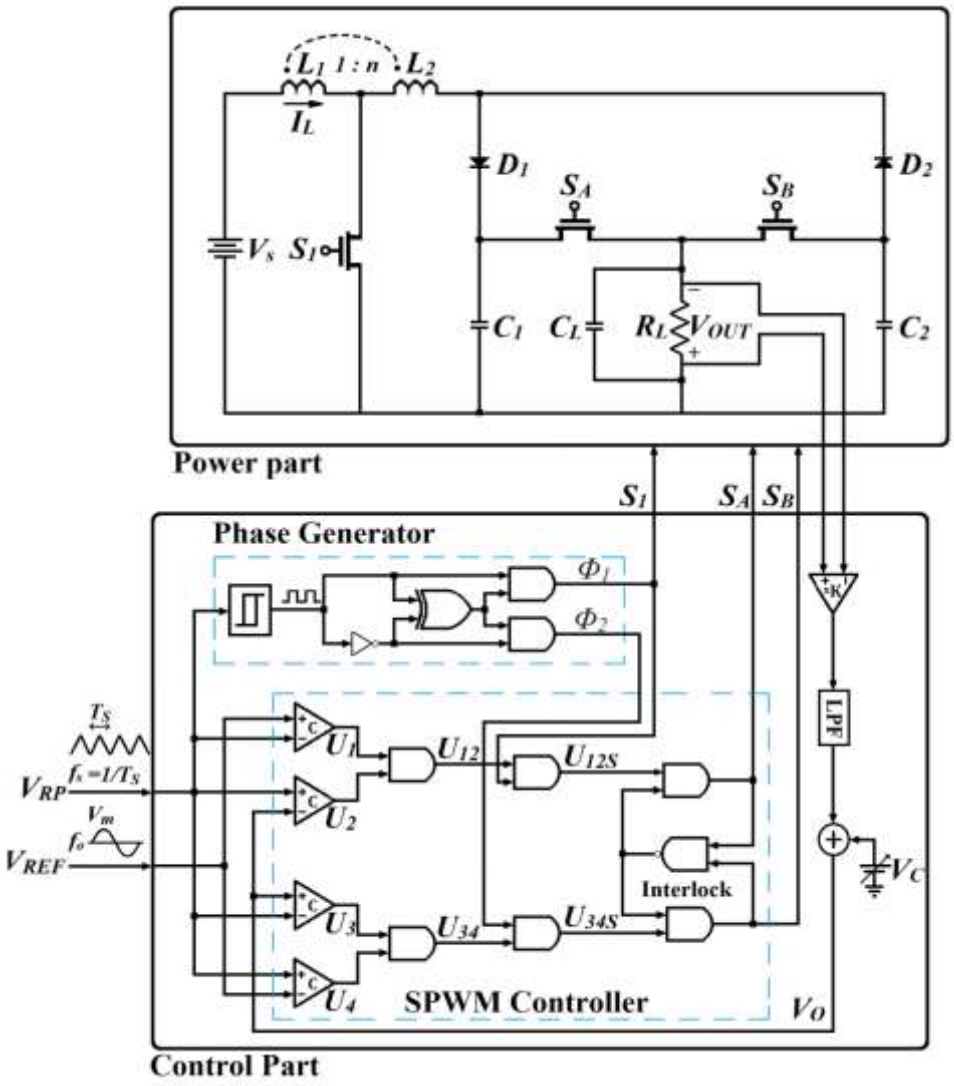

Fig. 1. Configuration of closed-loop SCII.

cascaded connection between supply V_S and output V_{OUT} . Firstly, the front-stage booster circuit is mainly in charge of step-up DC-DC conversion, including a MOSFET switch S_1, a coupled inductor L_1, L_2, diodes D_1-D_2, pumping capacitors C_1, C_2, where the same capacitance C (C_1=C_2=C) is assumed. This coupled inductor (L_1 and L_2) is modeled as an ideal transformer with a turn ratio of n (n=N_2/N_1). The main function of this front stage is to lift the values of voltage across C_1, C_2 up to $[(1+nD)/(1-D)]V_S$ and nV_S respectively, where D ($0<D<1$) is the duty cycle and DT_S is the period of charging this coupled inductor in one switching cycle T_S (T_S=1/f_S, f_S: switching frequency). Secondly, the rear-stage circuit: half-bridge DC-link is to handle DC-AC invertsion. It includes two switches S_A, S_B of SWPM control, a filter capacitor C_L, and a load resistor R_L, and additionally half-bridge pumping capacitors C_1, C_2. With the help of S_A and S_B in the half-bridge, the maximum range of the AC output V_{OUT} can reach to: $+[(1+nD)/(1-D)]V_S \sim -nV_S$. Fig. 2 shows the theoretical waveforms within an output cycle T_O (T_O=1/f_O, f_O: output frequency). Here, for the convenience of explanation, one T_O contains 11 (or above actually) switching cycle T_S. Each T_S has two phases: Phases I and II with the different periods DT_S and $(1-D)T_S$. The detailed operations are discussed as follows.

1) Phase I:

During this time interval, turn ON S_1, turn SPWM-ON S_A, and turn OFF S_B. Then, diode D_2 is turned ON, and D_1 is turned OFF. The relevant topology is shown in Fig. 3(a). The inductor L_1 is charged by supply V_S, and the energy is transferred from the primary winding of this coupled inductor to the secondary one for making the voltage as: V_{L1}=V_S, V_{L2}=nV_S. And then, the energy stored in the secondary winding is transferred into C_2 via S_1 and D_2 for making capacitor voltage V_{C2} towards $-nV_S$. At the same time, the siagnal from SPWM controller can control switch S_A ON or not, so as to make C_1 discharging the energy into C_L and R_L, and then V_{OUT} is heading towards the direction of the positive output.

2) Phase II:

During this time interval, turn OFF S_1 and S_A, and turn SPWM-ON S_B. Then, diode D_1 is turned ON, and D_2 is turned OFF. The relevant topology is shown in Fig. 3(b). According to the theory of the booster, the steady-state voltage V_{L1} across L_1 is going towards the value of $-DV_S/(1-D)$ via the operation of duty cycle D, and thus the voltage V_{L2} across L_2 in the secondary side is approaching the value of $-nDV_S/(1-D)$. Then, C_1 is

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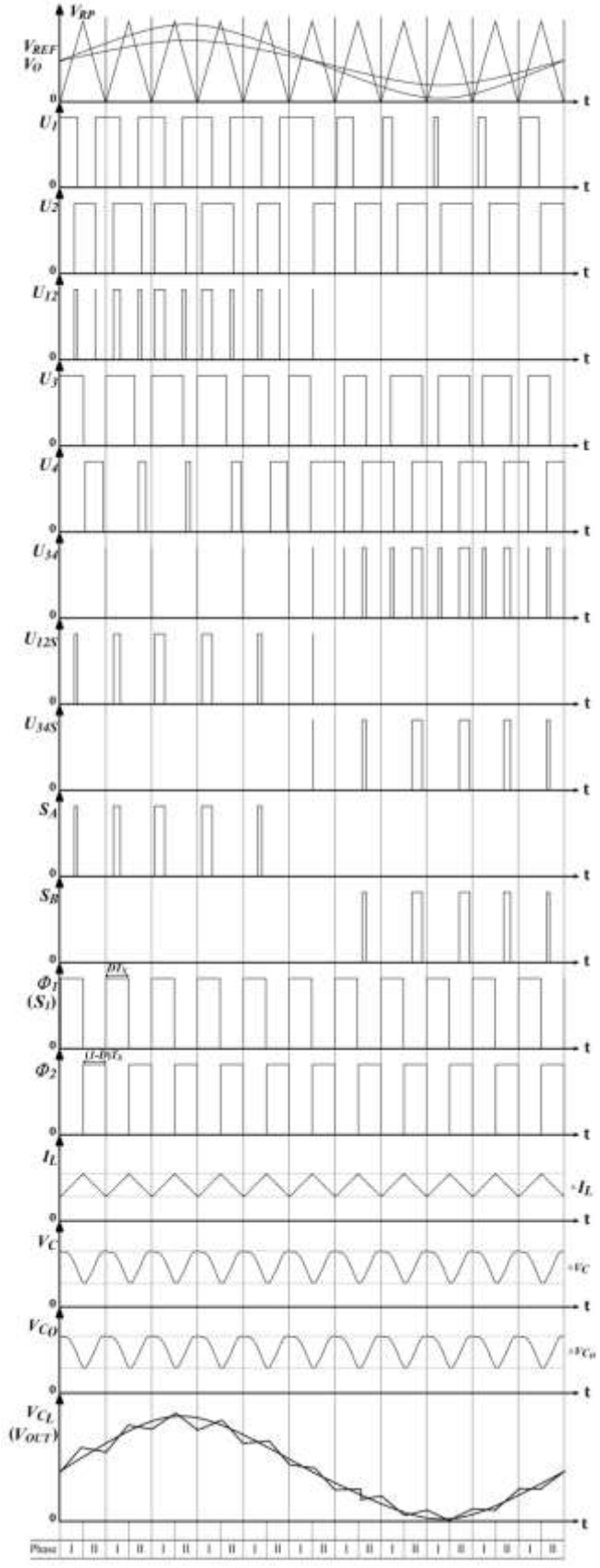

Fig. 2. Theoretical waveforms of closed-loop SCII.

charged by V_S, V_{L1}, V_{L2} in series via D_1 (V_S+|V_{L1}|+|V_{L2}| $\rightarrow V_{C1}$), and so V_{C1} is charged towards V_S +DV_S/(1-D)+ nDV_S/(1-D)= +[(1+nD)/(1-D)]V_S. At the same time, the siagnal from SPWM controller can control switch S_B ON or not, so as to make C_2 discharging the energy into

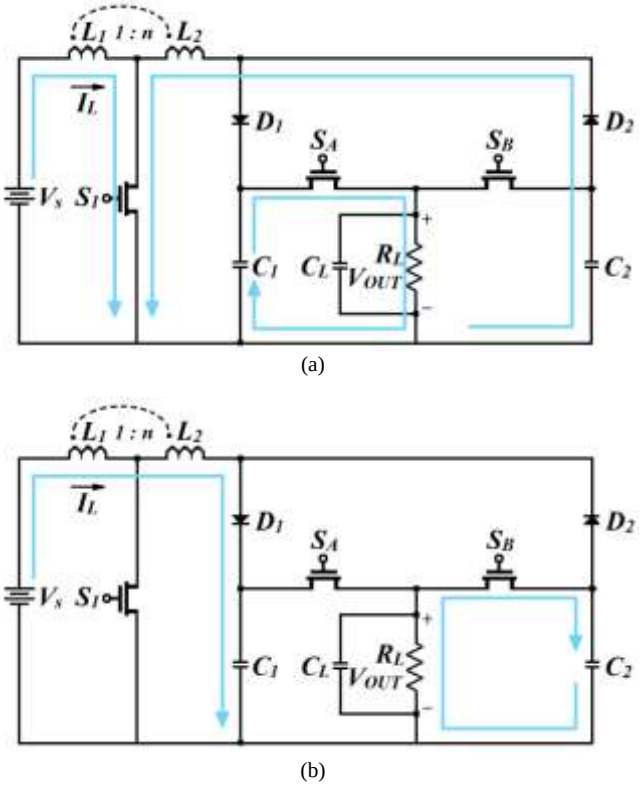

Fig. 3. Topologies for Phase (a) I and S_A: SPWM-ON, (b) II and S_B: SPWM-ON.

C_L and R_L, and then V_{OUT} is heading towards the direction of the negative output.

Based on the cyclical operations of Phase I and II, the overall step-up output V_{OUT} can reach to the AC output range as: +[(1+nD)/(1-D)]V_S ~ $-nV_S$. Here, the voltage gain is at about 5.89 (supply DC 24V, output AC 100V, 60Hz, AC peak: 142V), and so turn ratio n is taken by the nearest integer 6. For the symmetry of positive and negative output, let (1+nD)/(1-D) equal to n, and then the duty cycle D can be obtained at about 0.42. Thus, by using D=0.42 and n=6, it is reasonable that a symmetrical sinusoidal output can be attained from DC 24V to AC 100V_{RMS}, 60Hz.

B. Control Part

The control part of SCII is composed of a non- overlapping phase generator and a SPWM controller as in the lower half of Fig. 1. The operations of these two blocks are discussed as follows. Firstly, an external ramp function V_{RP} is sent into Schmitt trigger (i.e. Hysteresis comparator), and is compared with an adjustable upper/lower trigger level to produce a non-symmetrical clock signal, in which the duty cycle D (0<D<1) can be set or regulated by these levels. And then, this clock is sent to the non-overlapping circuit so as to obtain a set of phase signals Φ_1, Φ_2. Here, Φ_1 is taken as the driver signal of S_1. Exactly, DT_S is the period of Phase I for charging the coupled inductor. Secondly, from the view of controller signal flow, the output voltage V_{OUT} is attenuated and fed back into the OP-amp-based low-pass filter (LPF) for high-frequency noise rejection. Next, by adding an extra DC-shift of V_C, the output signal V_O can be obtained, and also be compared with the desired output V_{REF} via 4 comparators (U_1,

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U_2, U_3 and U_4), and following by using logic-AND to produce a set of control signals U_{12}, U_{34} for realizing SPWM. When e>0 and |e| is raising (e=V_{REF} -V_O), the pulse width of U_{12} is getting bigger. When e<0 and |e| is raising, the pulse width of U_{34} is getting bigger. And then, via the interlock circuit (avoid S_A and S_B being 1 simultaneously) plus coming into the phase of Φ_2, S_A and S_B can be obtained for the SPWM control. The main goal is to keep V_O on following V_{REF} (sinusoidal reference) to enhance the regulation capability of this proposed inverter. To summarize, based on V_O and V_{REF}, the relevant rules of producing the control/driver signals are listed as below.

1) Φ_1, Φ_2: non-overlapping antiphase signals;
   S_1=Φ_1.
2) If $V_{REF} > V_{RP}$, then U_1=1;
   If $V_{REF} < V_{RP}$, then U_1=0.
   If $V_{RP} > V_O$, then U_2=1;
   If $V_{RP} < V_O$, then U_2=0.
   If $V_O > V_{RP}$, then U_3=1;
   If $V_O < V_{RP}$, then U_3=0.
   If $V_{RP} > V_{REF}$, then U_4=1;
   If $V_{RP} < V_{REF}$, then U_4=0.
3) If U_1=1 and U_2=1, then U_{12}=1;
   If not, then U_{12}=0.
   If U_3=1 and U_4=1, then U_{34}=1;
   If not, then U_{34}=0.
4) If U_{12}=1 and Φ_2=1, then U_{12S}=1;
   If not, then U_{12S}=0.
   If U_{34}=1 and Φ_2=1, then U_{34S}=1;
   If not, then U_{34S}=0.
5) SPWM control signals: (^: logic-AND)
   S_A= U_{12S}, for $V_{REF} > V_O$.
   S_B= U_{34S}, for $V_{REF} < V_O$.
   (Interlock : S_A ^$S_B \neq$ 1)

III. Examples of SCII

In this paper, the proposed SCII is simulated by SPICE, and all the parameters are listed in TABLE I. Based on these parameters, we have three cases for steady-state responses and four cases for dynamic responses in total. Then, these results are illustrated to verify the efficacy of the proposed inverter.

1) Steady-State Responses:
   Case 1: f_O=60 Hz, V_m=145V
   Let the supply source V_S be DC 24V, load R_L be 800Ω, and the peak value and output frequency of V_{REF} are V_m=145V, f_O=60Hz. The waveform of V_{OUT} is obtained as in Fig. 4(a). V_{OUT} has the practical peak value of 140V (i.e. 99V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 68.2% and THD is 2.023%.

TABLE I
Circuit parameters of SCII.

Supply source (V_S)	24V
Pumping capacitor (C_1, C_2)	220μF
Coupled inductor(L_1, L_2)	70μH, 2520μH (n=6)
Filter capacitor (C_L)	1.2μF
On-state resistor of MOSFET (S_1)	50μΩ
On-state resistor of MOSFETs (S_A, S_B)	2.2Ω
Diode (D_1, D_2)	D1N5822
Load resistor (R_L)	800Ω
Switching frequency (f_S)	50kHz
Output frequency (f_O)	60Hz

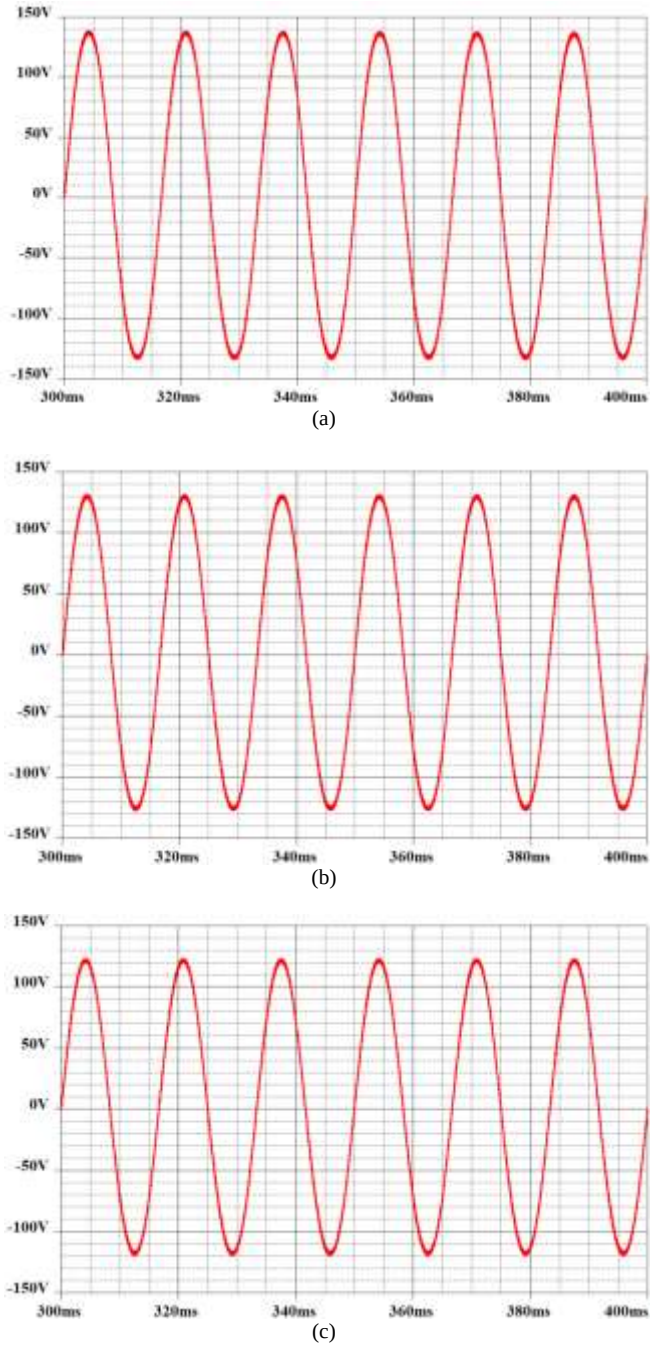

Fig. 4. Output V_{OUT} for V_{REF}: (a) f_O =60Hz, V_m =145V; (b) f_O=60Hz, V_m=135V; (c) f_O =60Hz, V_m=125V.

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Case 2: f_O=60 Hz, V_m=135V

Let the supply source V_S be DC 24V, load R_L be 800Ω, and the peak value and output frequency of V_{REF} are V_m=135V, f_O=60Hz. The waveform of V_{OUT} is obtained as in Fig. 4(b). V_{OUT} has the practical peak value of 131V (i.e. 92.6V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 66.7% and THD is 1.449%.

Case 3: f_O=60 Hz, V_m=125V

Let the supply source V_S be DC 24V, load R_L be 800Ω, and the peak value and output frequency of V_{REF} are V_m=125V, f_O=60Hz. The waveform of V_{OUT} is obtained as in Fig. 4(c). V_{OUT} has the practical peak value of 123V (i.e. 86.9V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 61.2% and THD is 1.161%.

2) Dynamic Responses:

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of supply voltage, such a variation of supply voltage V_S must be considered, as well as variation of load R_L and/or sinusoidal reference V_{REF} (f_O or V_m).

Case 1: V_S variation

Assume that V_S is normally at DC 24V, and then it has an instant voltage drop: 24V→23V on 350ms (V_{REF}: f_O=60Hz, V_m=145V). The waveform of V_{OUT} is shown as in Fig. 5(a). Obviously, V_{OUT} has a slight decrease into about 138V.

Case 2: R_L variation

Assume that R_L is 800Ω normally, and suddenly it changes from 800Ω to 400Ω on 350ms (V_{REF}: f_O= 60Hz, V_m=145V). Fig. 5(b) shows the transient waveform of V_{OUT} at the moment of loading variation. Obviously, V_{OUT} has a small drop but can still be following V_{REF}.

Case 3: f_O variation

Assume that the frequency f_O of V_{REF} is 60Hz normally. After a period of 350ms, and it suddenly changes from 60Hz to 120Hz. Fig. 5(c) shows the transient waveform of V_{OUT} at the moment of variation as V_{REF}: f_O=60Hz→120Hz, V_m=145V. Obviously, V_{OUT} is still able to follow V_{REF} even the frequency of V_{REF} changes.

Case 4: V_m variation

Assume that V_m is 125V normally, After a period of 350ms, and it changes from 125V to 145V. Fig. 5(d) shows the transient waveform of V_{OUT} at the moment of variation as V_{REF}: f_O=60Hz, V_m=125V →145V. Obviously, V_{OUT} is still able to follow V_{REF} even the amplitude of V_{REF} changes.

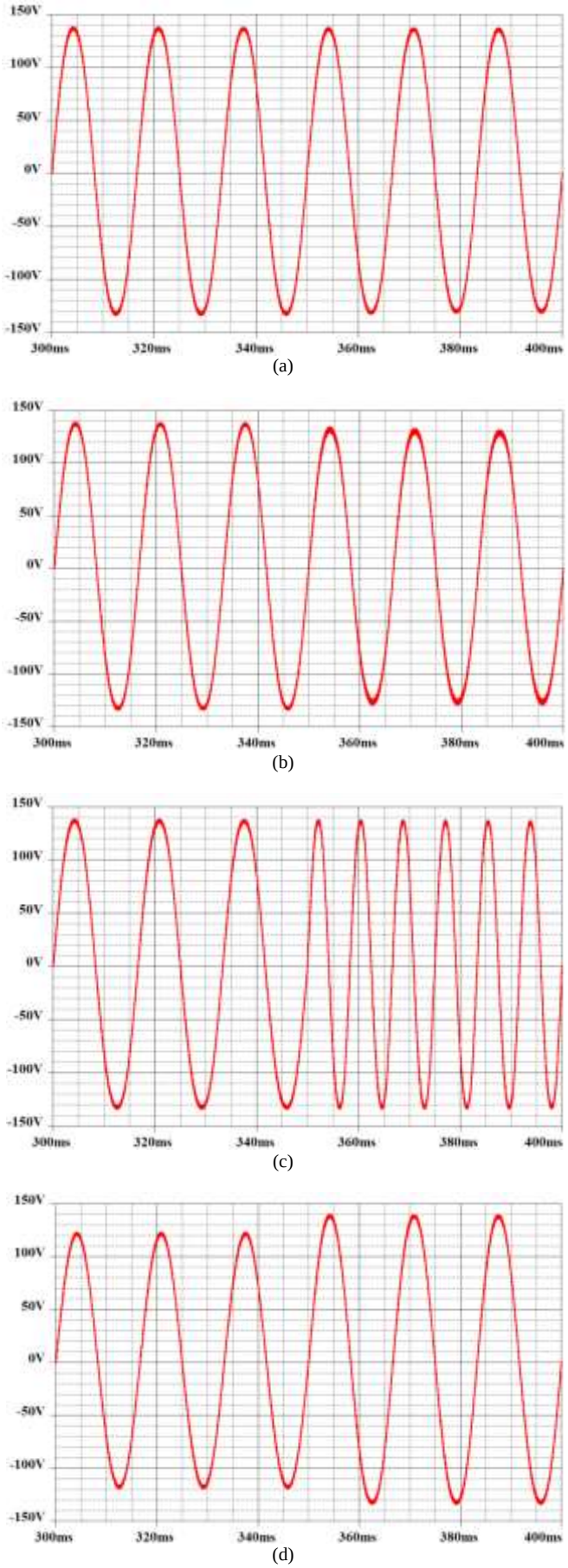

Fig. 5. Output V_{OUT} for the variation of (a) V_S; (b) R_L; (c) f_O; (d) V_m.

According to the above results, it is obvious that V_{OUT} is following V_{REF} for the cases, including V_S source variation, R_L loading variation, f_O frequency variation, V_m amplitude variation. These results show that this proposed inverter has good closed-loop dynamic performances.

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Fig. 6. Prototype circuit of closed-loop SCII.

IV. Conclusions

This papae presnts a simple SCII scheme with combining a phase generator and a SPWM controller for boost DC-AC conversion and closed-loop regulation. The power part is composed of a switched-copuled-inductor booster and a half-bridge DC-link inverter between V_S and V_{OUT}, so as to obtain the boost output range: $+[(1+nD)/(1-D)]V_S \sim -nV_S$, where n is the turn ratio of the coupled inductor and D is duty cycle of charging this inductor. Practically, while D=0.42 and n=6, a symmetrical sinusoidal output: AC $100V_{RMS}$, 60Hz can be obtained at the supply of DC 24V. Finally, the closed-loop SCII is designed and simulated by SPICE for some cases: steady-state and dynamic responses. The advantages of the proposed scheme are listed as follows. (i) This SCII needs just one coupled-inductor device. Except this, other components (including switches, diodes, and capacitors) can be made in IC fabrication promisingly. (ii) This proposed inverter sure is to present a simple configuration for boost DC-AC conversion via using fewer component count here. It is beneficial to circuit complexity decrease as well as coat reduction. (iii) For a higher gain, it can be realized with increasing the turn ratio of coupled inductor or extending the number of pumping capacitors. (iv) The SPWM technique is adopted not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against source and loading variation. At present, the prototype circuit of this inverter is implemented in the laboratory as in the photo of Fig. 6. Some experimental results will be obtained and measured for the verification of the proposed inverter.

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