A Closed-Loop Coupled-Inductor Cockcroft-Walton-Switched-Capacitor Inverter for Boost DC-AC Conversion

Yuen-Haw Chang and Kai-Lin Hsu

***Abstract*—A coupled-inductor Cockcroft-Walton-switched-capacitor (CICWSC) inverter is proposed by combining a non-overlapping circuit and sinusoidal pulse-width-modulation (SPWM) controller for boost DC-AC conversion and closed-loop regulation. The power part between source V_S and of V_O is composed of three sub-circuits, including: (i) coupled-inductor booster (CI booster), (ii) Cockcroft-Walton-switched-capacitor doubler (CWSC doubler), and (iii) half-bridge DC-link, so as to obtain an AC output range: $+[(n+1)/(1-D)]V_S \sim -[(n+1)/(1-D)]V_S$, where D is the duty cycle and n is the turn ratio of coupled inductor. While D=0.5, n=2, the practical range of V_O can be obtained as: $+6V_S \sim -6V_S$. Here, the SPWM is employed not only to enhance regulation capability for the different amplitude and frequency of V_O, but also to reinforce robustness to source or loading variation. Finally, the closed-loop CICWSC is designed and simulated by SPICE for cases of steady-state and dynamic responses. All results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*—coupled-inductor, Cockcroft-Walton-switched-capacitor, sinusoidal pulse-width-modulation, boost DC-AC conversion.**

I. Introduction

In recent years, step-up power converters are widely used as power modules in the portable electronic equipments, e.g. notebooks, smart phones, and pads…etc. The power modules of those products are always asked for some good features: small volume, light weight, high conversion efficiency, and strong regulation capability. Due to magnetic elements used, traditional converters always have a large volume and heavy weight. Thus, more manufactures and researchers pay much attention to this topic, especially for requiring step-up DC-DC/DC-AC converters realized on a compact chip by mixed-mode VLSI technology.

The switched-capacitor (SC) converter is one of the good solutions for high-gain DC-DC/DC-AC conversion. Up to now, the various SC types have been suggested. In 1976, Dickson charge pumping was proposed based on a diode-capacitor chain structure [1]. In 1990s, Ioinovici proposed a SC with two capacitor cells working complementarily [2-3]. In 2007, Chang presented a CPLD-based implementation of SC step-down DC-DC converter for the multiple output choices [4]. In 2011-2013, Chang *et al*. proposed a series of multistage multiphase SC step-up/down DC-DC/DC-AC converter/inverter [5-8]. In 2014, Chang *et al*. proposed a 2-stage 4-phase SC-based boost DC-AC inverter by using sinusoidal PFM control [9]. In 2015, Chang *et al*. proposed a closed-loop high-gain switched-capacitor-inductor-based boost DC-AC inverter [10].

To obtain a higher voltage gain, it is one of the good ways by using the turn ratio and/or extra winding stage of the coupled inductor. Nevertheless, the stress on transistors and the volume of magnetic device must be considered. In 2015, Chen *et al*. proposed a coupled-inductor boost integrated flyback converter including high-voltage gain and ripple-free input current [11]. Bahrami *et al*. suggested a modified step-up boost converter with coupled-inductor and super-lift techniques [12]. Chen *et al*. proposed a novel switched-coupled-inductor step-up converter and its derivatives [13]. Wu *et al*. proposed a nonisolated high step-up DC-DC converter adopting switched-capacitor cell [14]. Nouri *et al*. proposed an interleaved high-gain step-up DC-DC converter based on three-winding high-frequency coupled-inductor and voltage-multiplier cell [15]. In 2016, Chang *et al*. proposed a novel coupled-inductor switched- capacitor inverter for high-gain boost DC-AC conversion [16]. In 2017, Chang *et al*. proposed a novel coupled-inductor switched-capacitor inverter for high-gain boost DC-AC conversion [17]. In this paper, the authors make an attempt on combining Cockcroft-Walton SC circuit with one coupled inductor to propose a closed-loop CICWSC inverter for boost DC-AC conversion and regulation.

II. Configuration of CICWSC Inverter

Fig. 1 shows the coupled-inductor Cockcroft-Walton-switched-capacitor (CICWSC) inverter proposed, and it contains two major parts: power and control part for achieving the boost DC-AC conversion and closed-loop regulation. These two parts are discussed as follows.

A. Power Part

The power part of this inverter as in the upper half of Fig. 1 contains a coupled-inductor booster (CI booster), a Cockcroft -Walton-switched-capacitor doubler (CWSC doubler), and a half-bridge DC-link, in cascaded connection between supply V_S and output V_{OUT}. Firstly, the front-stage circuit composed of CI booster and CWSC doubler is in charge of step-up DC-DC conversion. It includes switch S_1, diodes D_1-D_4, coupled-inductor L_1, L_2, clamping capacitor C_1, pumping capacitors C_2, C_3, and C_4, where it is assumed that same capacitance C (C_2=C_3=C_4=C). The coupled-inductor L_1 and

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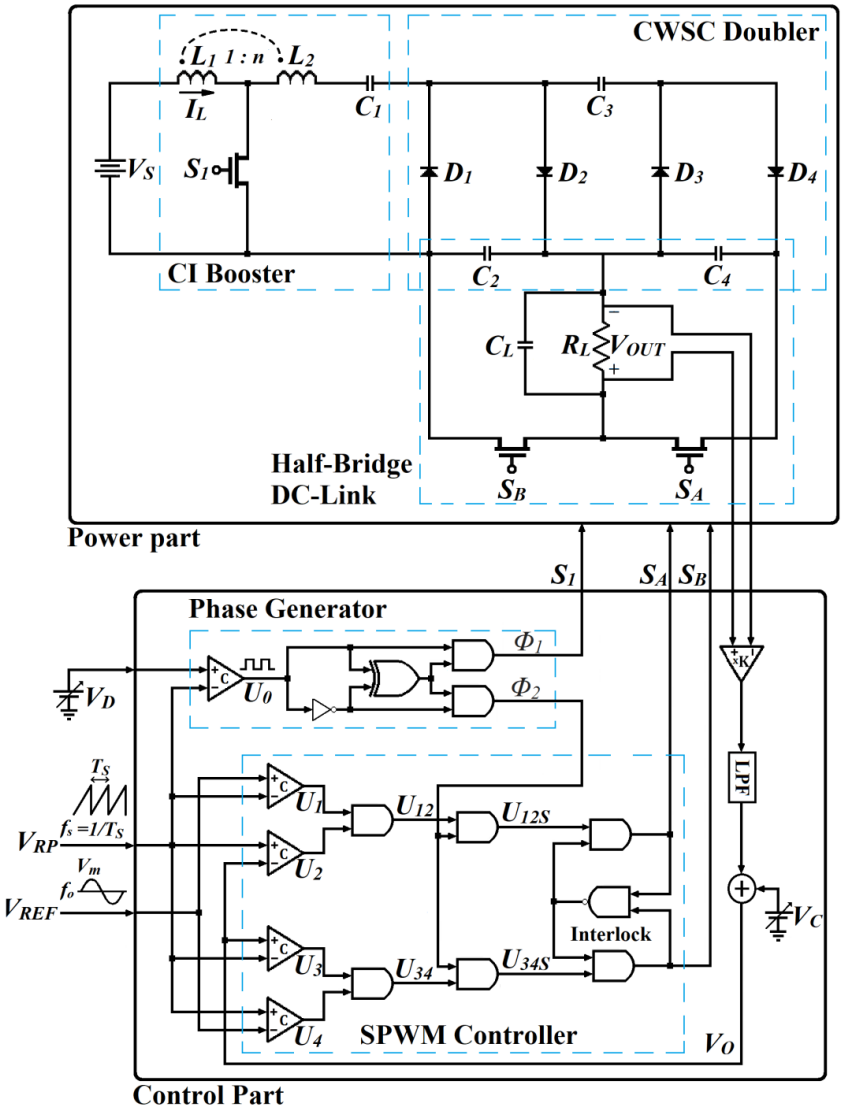

Fig. 1. Configuration of closed-loop CICWSC inverter.

L_2 is modeled as an ideal transformer with a turn ratio of n (n=N_2/N_1). The main function of this front stage is to raise the voltage gain up to [2(n+1)/(1-D)] at most from supply V_S to capacitor voltage (V_{C2}+V_{C4}), where D (0<D<1) is the duty cycle and DT_S is the period of charging this coupled inductor in a switching cycle T_S (T_S=1/f_S, f_S is the switching frequency). Secondly, the rear-stage circuit: half-bridge DC-link is to handle DC-AC inverter. It include switches S_A, S_B, half-bridge capacitors C_2, C_4, filter capacitor C_L, and load R_L. With the help of S_A and S_B in the half-bridge, the maximum range of the AC output V_{OUT} can reach: +[(n+1)/(1-D)]V_S ~ −[(n+1)/(1-D)]V_S. Fig. 2 shows the theoretical waveforms within an output cycle T_O (T_O=1/f_O, f_O is the output frequency). Here, for the convenience of explanation, one T_O contains 11 (or above actually) switching cycle T_S. Each T_S has two phases: Phases I and II with the different periods DT_S and (1-D)T_S. The detailed operations are discussed as follows.

1) Phase I:

During this time interval, turn ON S_1 and turn OFF S_A, S_B. Then, diodes D_1, D_3 are turned ON, and D_2, D_4 are OFF. The relevant topology is shown in Fig. 3(a). The inductor L_1 is charged by supply V_S, and simultaneously the energy is transferred from the primary side of this coupled inductor to the secondary side for making the inductor voltages as: V_{L1}=+V_S, V_{L2}=−nV_S. And then, the clamping capacitor C_1 is charged by V_{L2} so as to lift V_{C1} towards the value of nV_S. Also, the pumping capacitor C_3 is charged with the total loop volatge of V_{L2}, V_{C1}, V_{C2} so as to boost V_{C3} towards [(n +1)/(1- D)]V_S.

2) Phase II:

During this time interval, S_A or S_B is turned ON and S_1 is turned OFF. Then, diodes D_2, D_4 are turned ON, and D_1, D_3 are turned OFF. According to the theory of the booster, the steady-state voltage V_{L1} across L_1 is going towards the value of −[D/(1-D)]V_S based on duty cycle D, and thus the voltage V_{L2} across L_2 in the secondary side is approaching the value of +[nD/(1-D)] V_S.

(i) While S_A is ON:

The relevant topology is shown in Fig. 3(b). The capacitors C_2 and C_4 are charged by V_S, V_{L1}, V_{L2}, V_{C1} in series, and together plus V_{C3} and V_{C2}, respectively. At the same time, C_4 is discharged to supply the energy to C_L and R_L.

(Output range of V_{OUT}: 0~+ $\frac{n+1}{1-D}$ V_S)

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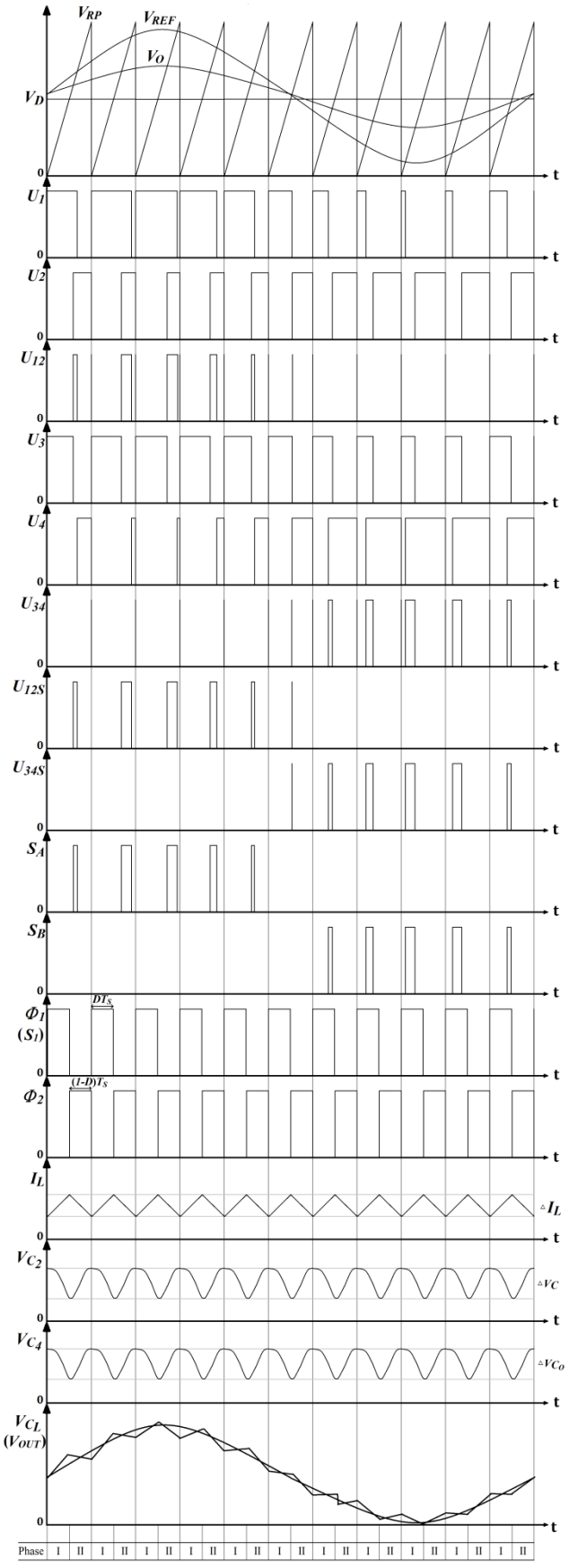

Fig. 2. Theoretical waveforms of closed-loop CICWSC Inverter.

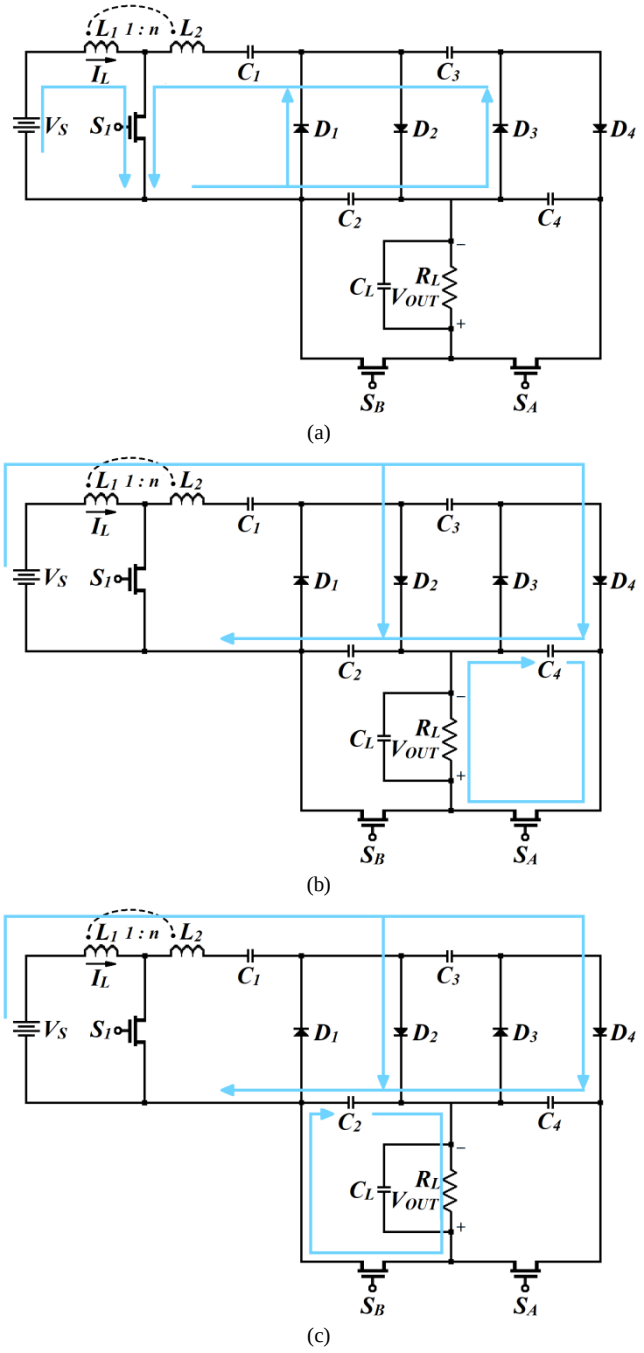

Fig. 3. Topologies for Phase (a) I, (b) II (S_A:ON), and (c) II (S_B:ON).

(ii) While S_B is ON:

The relevant topology is shown in Fig. 3(c). The capacitors C_2 and C_4 are charged by V_S, V_{L1}, V_{L2}, V_{C1} in series, and together plue V_{C3} and V_{C2}, respectively. At the same time, C_2 is discharged to supply the energy to C_L and R_L.

(Output range of V_{OUT}: $0 \sim -\frac{n+1}{1-D} V_S$)

Based on the cyclical operations of Phase I and II, the overall step-up gain can reach to the value of $(n+1)/(1-D)$ (from V_S to V_{C2} or V_{C4}). Further, with the help of the half-bridge DC-link, the AC output can be realized for the range as: $+[(n+1)/(1-D)]V_S \sim -[(n+1)/(1-D)]V_S$.

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B. *Control Part*

The control part of CICWSC inverter is composed of a phase generator and a SPWM controller as in the lower half of Fig. 1. The operations of these two blocks are discussed as follows. Firstly, an adjustable voltage V_D is compared with a ramp function V_{RP} to produce a non-symmetrical clock signal U_0. And then, this clock is sent to the non-overlapping circuit so as to obtain a set of phase signals Φ_1 and Φ_2. Here, Φ_1 is taken as the driver signal of S_1. Thus, D is exactly the ON-time ratio (duty cycle) of S_1, and DT_S (period of Phase I) can be regulated by the value of V_D. Secondly, from the controller signal flow, the output voltage V_{OUT} is attenuated and fed back into the OP-amp low-pass filter (LPF) for high-frequency noise rejection. Next, by using an extra DC-shift of V_C, the output signal V_O is obtained and compared with the desired output V_{REF} via 4 comparators U_1, U_2, U_3 and U_4, and following by using logic-AND to produce a set of control signals U_{12}, U_{34} for realizing SPWM. When e>0 and |e| is raising (e=V_{REF}-V_O), the pulse width of U_{12} is getting bigger. When e<0 and |e| is raising, the pulse width of U_{34} is getting bigger. And then, via the interlock circuit (avoid S_A and S_B being 1 simultaneously) plus coming into the phase of Φ_2, S_A and S_B can be obtained for the SPWM control. The main goal is to keep V_O on following V_{REF} (sinusoidal reference) to enhance the regulation capability of this proposed inverter. To summarize, based on V_O and V_{REF}, the relevant rules of producing the control/driver signals are listed as below.

1) Φ_1, Φ_2: non-overlapping antiphase signals from U_0;
   $S_1=\Phi_1$.
2) If $V_D>V_{RP}$, then $U_0=1$; If $V_D<V_{RP}$, then $U_0=0$.
3) If $V_{REF}>V_{RP}$, then $U_1=1$; If $V_{REF}<V_{RP}$, then $U_1=0$;
   If $V_{RP}>V_O$, then $U_2=1$; If $V_{RP}<V_O$, then $U_2=0$;
   If $V_O>V_{RP}$, then $U_3=1$; If $V_O<V_{RP}$, then $U_3=0$;
   If $V_{RP}>V_{REF}$, then $U_4=1$;If $V_{RP}<V_{REF}$, then $U_4=0$.
4) If $U_1=1$ and $U_2=1$, then $U_{12}=1$ (otherwise $U_{12}=0$);
   If $U_3=1$ and $U_4=1$, then $U_{34}=1$ (otherwise $U_{34}=0$).
5) If $U_{12}=1$ and $\Phi_2=1$, then $U_{12S}=1$ (otherwise $U_{12S}=0$);
   If $U_{34}=1$ and $\Phi_2=1$, then $U_{34S}=1$ (otherwise $U_{34S}=0$).
6) SPWM control signals: (^: logic-AND)
   $S_A=U_{12S}$, for $V_{REF}>V_O$;
   $S_B=U_{34S}$, for $V_{REF}<V_O$.
   (Interlock : $S_A \wedge S_B \neq 1$)

III. Examples of CICWSC Inverter

In this paper, the proposed CICWSC is simulated by SPICE, and all the circuit parameters are listed in TABLE I. There are 3 cases for steady-state responses and 4 cases for dynamic responses in total. Then, these results are illustrated to verify the efficacy of the proposed inverter.

1) Steady-State Responses:
   Case 1: f_O=60 Hz, V_m=125V
   Let the supply source V_S be DC 24V, load R_L be 600Ω, and the peak value and output frequency of V_{REF} are V_m=125V, f_O=60Hz. The waveform of V_{OUT} is obtained as in Fig. 4(a). V_{OUT} has the practical peak value of 125V (i.e. 88.4V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 60.9% and THD is 1.726%..

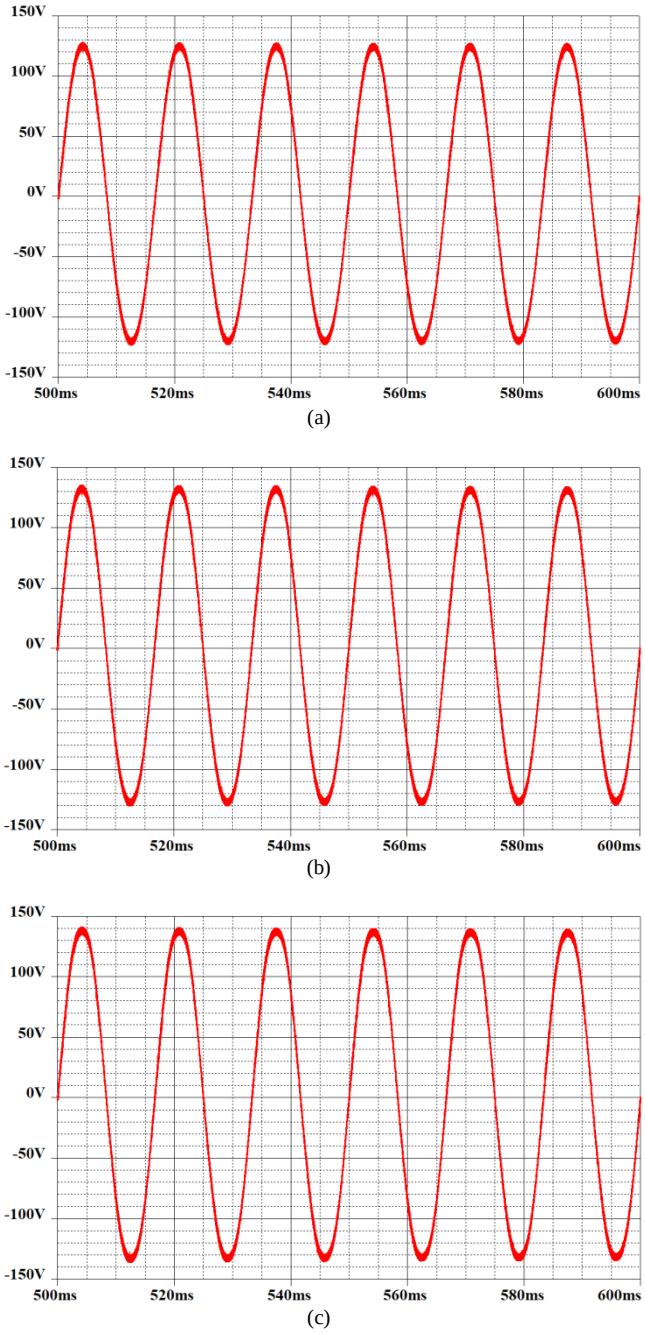

Fig. 4. Output V_{OUT} for V_{REF}: (a) f_O =60Hz, V_m =125V; (b) f_O=60Hz, V_m=135V; (c) f_O =60Hz, V_m=145V.

Case 2: f_O=60 Hz, V_m=135V
Let the supply source V_S be DC 24V, load R_L be 600Ω, and the peak value and output frequency of V_{REF} are V_m=135V, f_O=60Hz. The waveform of V_{OUT} is obtained as in Fig. 4(b). V_{OUT} has the practical peak value of 134V (i.e. 94.7V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 68.3% and THD is 2.183%.

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Case 3: f_O=60 Hz, V_m=145V

Let the supply source V_S be DC 24V, load R_L be 600Ω, and the peak value and output frequency of V_{REF} are V_m=145V, f_O=60Hz. The waveform of V_{OUT} is obtained as in Fig. 4(c). V_{OUT} has the practical peak value of 140V (i.e. 99V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 74.8% and THD is 3.072%.

2) Dynamic Responses:

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of source voltage, such a variation of source voltage V_S must be considered, as well as variation of load R_L and/or reference V_{REF} (f_O or V_m).

Case 1: V_S variation

Assume that V_S is normally at DC 24V, and then it has an instant voltage drop: 24V→23V on 550ms (V_{REF} : f_O=60Hz, V_m=145V). The waveform of V_{OUT} is shown as in Fig. 5(a). Obviously, V_{OUT} has a slight decrease into about 138V.

Case 2: R_L variation

Assume that R_L is 600Ω normally, and it suddenly changes from 600Ω to 300Ω on 550ms (V_{REF} : f_O= 60Hz, V_m=145V). Fig. 5(b) shows the transient waveform of V_{OUT} at the moment of loading variation. Obviously, V_{OUT} has a small drop but can still be following V_{REF}.

Case 3: f_O variation

Assume that the frequency f_O of V_{REF} is 60Hz normally. After a period of 550ms, and it suddenly changes from 60Hz to 120Hz. Fig. 5(c) shows the transient waveform of V_{OUT} at the moment of variation: f_O =60Hz→120Hz (V_m=145V). Obviously, V_{OUT} is still able to follow V_{REF} even the frequency of V_{REF} changes.

Case 4: V_m variation

Assume that V_m is 125V normally, After a period of 550ms, and it changes from 125V to 145V. Fig. 5(d) shows the transient waveform of V_{OUT} at the moment of variation: V_m=125V→145V. Obviously, V_{OUT} is still able to follow V_{REF} even the amplitude of the desired V_{REF} changes.

According to the above results, it is obvious that V_{OUT} is following V_{REF} for the cases, including V_S source variation, R_L loading variation, f_O frequency variation, V_m amplitude variation. These results show that this proposed inverter has good closed-loop dynamic performances.

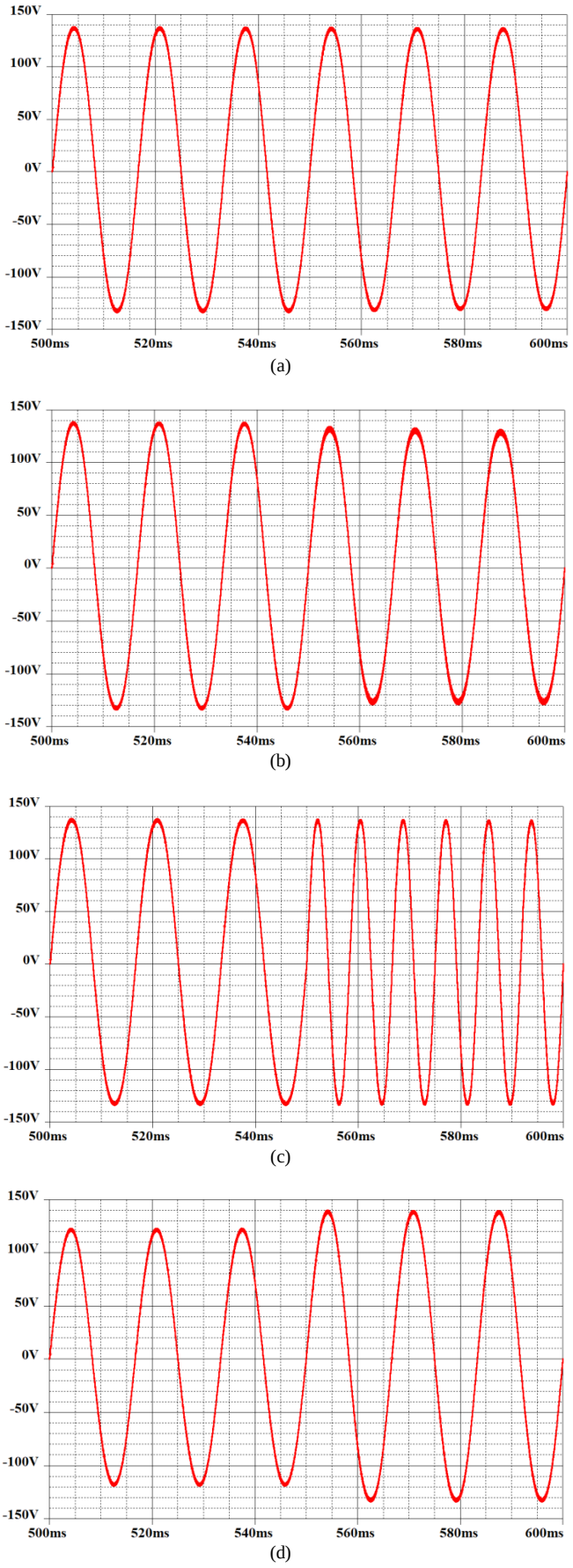

Fig. 5. Output V_{OUT} for the variation of (a) V_S; (b) R_L; (c) f_O; (d) V_m.

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TABLE I
Circuit parameters of CICWSC inverter.

Supply source (V_S)	24V
Clamping capacitor (C_1)	47μF
Pumping capacitor (C_2-C_4)	47uF
Coupled-inductor (L_1, L_2)	150μH, 600μH (n=2)
Output capacitor (C_L)	1μF
Power MOSFETs (S_1, S_A, S_B)	ASW
On-state resistor of MOSFET (S_1)	50μΩ
On-state resistor of MOSFETs (S_A, S_B)	2Ω
Diodes (D_1-D_4)	D1N5822
Load resistor (R_L)	600Ω
Switching frequency (f_S)	40kHz
Output frequency (f_O)	60Hz

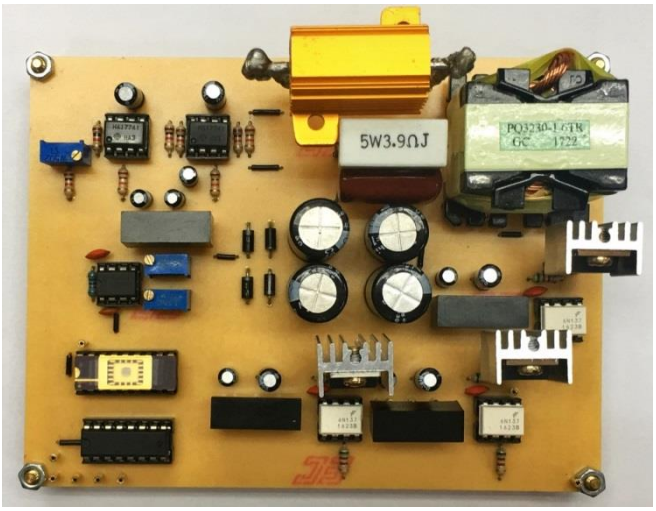

Fig. 6. Prototype circuit of CICWSC inverter.

IV. Conclusions

A novel CICWSC inverter is proposed by combining a non-overlapping circuit and SPWM controller for the high-gain boost DC-AC conversion and closed-loop regulation. Finally, the CICWSC is designed and simulated, and all results are illustrated to show the efficacy of the proposed scheme. The advantages of the scheme are listed as follows. (i) This CICWSC needs just one coupled-inductor element (inductor). Except this, other components (i.e. SC) will be able to be made in IC fabrication future. (ii) This proposed inverter can provide a high voltage gain (from V_S to half-bridge total capacitor voltage) of [2(n+1)/(1-D)] at most. (iii) For a higher gain, it can be realized with increasing the turn ratio of coupled inductor and/or extending the number of pumping capacitors. (iv) The SPWM technique is adopted not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against source/loading variation. At present, the prototype circuit of this inverter is implemented in the laboratory as shown in the photo of Fig. 6. Some experimental results will be obtained and measured for the verification of the proposed inverter.

References

[1] John F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374-378, Jun. 1976.

[2] On-Cheong Mak, Yue-Chung Wong and Adrian Ioinovici, "Step-up DC power supply based on a switched-capacitor circuit," *IEEE Transactions on Industrial Electronics*, vol. 42, no. 1, pp. 90-97, Feb. 1995.

[3] Guangyong Zhu and Adrian Ioinovici, "Steady-state characteristics of switched-capacitor electronic converters," *Journal of Circuits, Systems and Computers*, vol. 7 , no. 2, pp. 69-91, 1997.

[4] Yuen-Haw Chang, "CPLD-based closed-loop implementation of switched-capacitor step-down DC-DC converter for multiple output choices," *IET Electric Power Applications*, vol. 1, issue 6, pp. 926-935, Nov. 2007.

[5] Yuen-Haw Chang, "Design and analysis of multistage multiphase switched-capacitor boost DC-AC inverter," *IEEE Transactions on Circuits and Systems I: Regular paper*, vol. 58, no. 1, pp. 205-218, Jan. 2011.

[6] Yuen-Haw Chang, "Variable-conversion-ratio multistage switched-capacitor-voltage-multiplier/divider DC-DC converter," *IEEE Transactions on Circuits and Systems I: Regular paper*, vol. 58, no. 8, pp. 1944-1957, Aug. 2011.

[7] Yuen-Haw Chang and Ming-Zong Wu, "Generalized *mc x nc* -stage switched-capacitor-voltage-multiplier-based boost DC-AC inverter," *International Journal of Electronics*, vol. 99, no. 1, pp. 29-53, Jan. 2012.

[8] Yuen-Haw Chang and Yun-Jie Huang, "Closed-loop 7-Level switched-capacitor boost DC-AC inverter with sinusoidal PFM control," *International MultiConference of Engineers and Computer Scientists 2013 (IMECS'2013)*, vol. 2, Hong Kong, pp. 641-646, Mar. 13-15, 2013.

[9] Yuen-Haw Chang, Chin-Ling Chen and Po-Chien Lo, "2-Stage 4-Phase Switched-Capacitor Boost DC-AC Inverter with Sinusoidal PFM Control," *International MultiConference of Engineers and Computer Scientists 2014 (IMECS'2014)*, vol. 2, Hong Kong, pp. 673-678, Mar. 12-14, 2014.

[10] Yuen-Haw Chang, Yu-Kai Lin, "A closed-loop high-gain switched-capacitor-inductor-based boost DC-AC inverter," *International MultiConference of Engineers and Computer Scientists 2015 (IMECS'2015)*, vol. 2, Hong Kong, pp. 694-699, Mar. 18-20, 2015.

[11] Zhangyong Chen, Qun Zhou and Jianping Xu, "Coupled-inductor boost integrated flyback converter with high-voltage gain and ripple-free input current," *IET power Electronics*, vol. 8, pp. 213-220, Feb. 2015.

[12] Hamid Bahrami, Hossein Iman-Eini, Babak Kazemi, Alireza Taheri, "Modified step-up boost converter with coupled-inductor and super-lift techniques," *IET power Electronics*, vol. 8, pp. 898-905, Jun. 2015.

[13] Shih-Ming Chen, Man-Long Lao, Yi-Hsun Hsieh, Tsorng-Juu Liang, Kai-Hui Chen, "A novel switched-coupled-inductor DC-DC step-up converter and its derivatives," *IEEE Transactions on Industry Applications*, vol. 51, no. 1, pp. 309-314, Jan. 2015.

[14] Gang Wu, Xinbo Ruan, Zhihong Ye, "Nonisolated high step-up DC-DC converters adopting switched-capacitor cell," *IEEE Transactions on Industrial Electronics*, vol. 32, no. 1, pp. 383-393, Jan. 2015.

[15] Tohid Nouri, Seyed Hossein Hosseini, Ebrahim Babaei and Jaber Ebrahimi, "Interleaved high step-up DC-DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell," *IET Power Electronics*, vol. 8, no. 2, pp. 175-189, Feb. 2015.

[16] Yuen-Haw Chang, Jyun-Jia Liao, "A novel coupled-inductor switched-capacitor inverter for high-gain boost DC-AC conversion," *International MultiConference of Engineers and Computer Scientists 2016 (IMECS'2016)*, vol. 2, Hong Kong, pp. 603-608, Mar. 16-18, 2016.

[17] Yuen-Haw Chang, Zheng-Bin Li, "A high-gain serial-parallel–switched-capacitor coupled-inductor boost DC-AC inverter," *International MultiConference of Engineers and Computer Scientists 2017 (IMECS'2017)*, vol. 2, Hong Kong, pp. 688-693, Mar. 15-17, 2017.

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