Mathematical Modeling and Analysis of Coupled-Inductor Cockcroft-Walton-Switched-Capacitor Inverter

Yuen-Haw Chang and Kai-Lin Hsu

***Abstract*—The main purpose of this research is to present the detailed mathematical derivation of system modeling and steady-state analysis of coupled-inductor Cockcroft-Walton-switched-capacitor (CICWSC) inverter for the boost DC-AC conversion. The part of CICWSC for power conversion, built up by three: CI booster, CWSC doubler, and half-bridge DC-link in cascade between supply *Vs* and output *Vo*, is capable of boosting the DC-AC gain into: +(*n*+1)/(1-*D*) ~ -(*n*+1)/(1-*D*), where *n* is the turn ratio of coupled inductor, and *D* is the ratio cycle of inductor-charging. For example, when *n*=2, *D*=0.5, the conversion from DC 24V to AC 100Vrms, 60Hz can be attained. With the help of the proposed modeling, this boosting gain is proven through steady-state analytic discussions. Moreover, it is much helpful to future analysis and design. At the end, some simulation/experiment cases are discussed, and all results are illustrated/verified on the prototype to confirm the efficacy of CICWSC's modeling.**

***Index Terms*—boost DC-AC conversion, coupled-inductor (CI), Cockcroft-Walton-switched-capacitor (CWSC), steady-state analysis, mathematical derivation.**

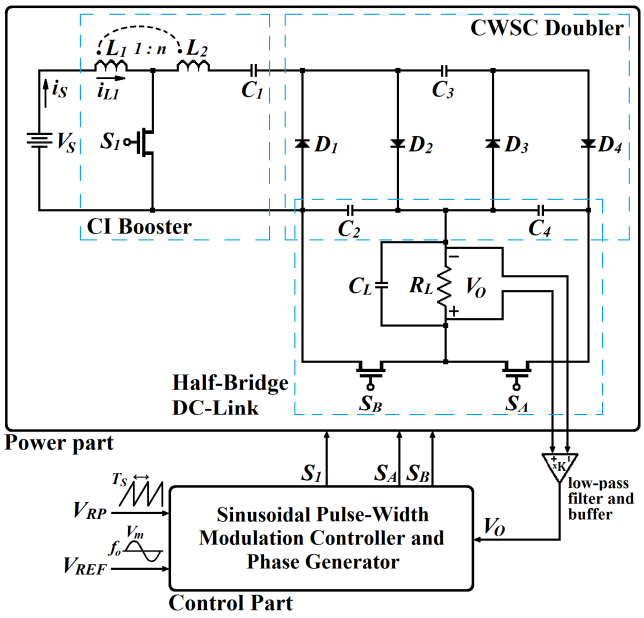

Fig. 1. Configuration of CICWSC.

I. Introduction

Over the past decades, a large number of engineers have devoted great efforts and many resources to developing switched-capacitor (SC) power converters on account of the inherent advantages in adopting device simplification, i.e., semi-switches and capacitors are just needed. Because of no magnetic device used, the SC-based power converters have two features: light weight and compact size. This kind of SC allows for a wide range of applications, e.g., driver of WLED, LCD, EEPROM, etc. So far, many well-structured SCs have been developed. About 45 years ago, a famous charge pump based on a diode-capacitor chain structure was proposed by Dickson [1]. However, both large area and rigid gain are its weaknesses. In the early 1990s, Ioinovici *et al.* suggested a series of SC converters by the cell-interleaved structure, and discussed issues related to some characteristics in a steady state [2-3]. In recent years, Chang *et al.* developed several novel SC-based converters aiming for high-gain DC-DC/ DC-AC conversion [4-6]. Further, many researchers adopted the coupled-inductor idea in combination with SC scheme for building higher gain converters [7-9]. Here, we are trying to present the detailed derivation of mathematical modeling of CICWSC as a solid foundation for future system analysis and parameter design.

Manuscript received June 28, 2021. This work is supported by Ministry of Science and Technology of Taiwan, under Grant MOST 109-2221-E- 324-027.
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II. Configuration

Fig. 1 demonstrates the closed-loop CICWSC inverter as presented in [8], consisting of power part and control part for realizing the boost DC-AC conversion/regulation. As in the top-half one, the power part includes three circuit blocks: (i) CI booster, (ii) CWSC doubler, and (iii) half-bridge DC-link (HBDL), linked in cascade from DC supply V_S to AC output V_o. This part is responsible for power conversion of boosting and inverting. As in the bottom-half one, the control part has two blocks: SPWM controller and phase generator, to be in charge of timing control (to different phases) and regulation enhancement (to different references V_{REF}). In other words, the main goal is to keep V_o on following V_{REF} (i.e., desired output). For details, refer to control part of [9].

Firstly, details of the power circuit are introduced. The CI booster is built with one switch (S_1), a clamping capacitor (C_1), and one coupled inductor (L_1,L_2), aimed at boosting gain to: $(n+1)/(1-D)$ ($0<D<1$: ON-time ratio cycle of S_1; $n\geq 1$: turn ratio of the coupled inductor, i.e., L_1:$L_2=1$:n^2). The CWSC doubler is contained by three pumping capacitors

ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

(C_2-C_4) and four diodes (D_1-D_4), aimed at doubling the value of gain. The HBDL circuit is made of two switches (S_A,S_B), two bridge capacitors (C_2,C_4), a filter capacitor (C_L), and a load resistor (R_L), aimed at performing DC-AC inversion, so as to obtain the complete gain: $+(n+1)/(1-D)\sim -(n+1)/(1-D)$. Next, the operations of the power circuit are introduced. Fig. 2 shows the relevant theoretical waveforms. Let each of switching cycle T_S ($T_S=1/f_S$) be partitioned into Phase I & Phase II, and their respective periods are DT_S and $(1-D)T_S$ (f_S : switching frequency of ramp V_{RP}). In the following, let's look at the details of these phases.

(i) Phase I:

S_1 be ON and S_A, S_B be both OFF. Now, D_1,D_3 are biased ON, and D_2,D_4 are OFF. The related topology is obtained as in Fig. 3(a). L_1 is being on charge by V_S via S_1. The energy is being transferred from the primary coil to the secondary (i.e., aiming for $V_{L1}=V_S$, $V_{L2}=nV_S$). Then, C_1 is on charge by V_{L2} via D_1 (i.e., $V_{L2}\rightarrow V_{C1}$) to clamp V_{C1} up to nV_S. At the same time, C_3 is on charge in the loop of V_{L2},V_{C1},V_{C2} (i.e., $V_{L2}+V_{C2}\rightarrow V_{C1}+V_{C3}$). From the steady-state standpoint, it means that the charge transfers from C_2 to C_3 (i.e., $V_{C2}\rightarrow V_{C3}$). In addition, C_L is solely responsible for R_L concurrently.

(ii) Phase II:

S_1 be OFF and either S_A or S_B be SPWM-ON/OFF. Then, D_1,D_3 are OFF and D_2,D_4 are biased ON. The related topologies are obtained as in Fig. 3(b)-3(d). At this moment, C_2 is being on charge by V_S,V_{L1},V_{L2},V_{C1} in series via D_2 (i.e., $V_S+V_{L1}+V_{L2}+V_{C1}\rightarrow V_{C2}$). On the basis of voltage-second balance, the steady-state value of V_{L1}, V_{L2} will be $[D/(1-D)]\cdot V_S$ and $[nD/(1-D)]\cdot V_S$. So, the steady-state voltage of V_{C2} will be $[(n+1)/(1-D)]\cdot V_S$ (i.e., $V_S+DV_S/(1-D)+nDV_S/(1-D)+nV_S=[(n+1)/(1-D)]\cdot V_S$). At the same time, C_4 is on charge in the loop of V_S,V_{L1},V_{L2}, V_{C1},V_{C2},V_{C3} (i.e., $V_S+V_{L1}+V_{L2}+V_{C1}+V_{C3}\rightarrow V_{C2}+V_{C4}$). From the steady-state standpoint, it means that the charge transfers from C_3 to C_4 (i.e., $V_{C3}\rightarrow V_{C4}$). Similarly, V_{C3},V_{C4} have the same steady-state voltage as V_{C2}, i.e., $[(n+1)/(1-D)]\cdot V_S$. Besides, there are two operations of SPWM considered as follows: (a) When either S_A or S_B is SPWM-ON, C_4 or C_2 is on discharge to supply energy for C_L, R_L. The related topology is shown in Fig. 3(b) or 3(c) so as to keep V_o moving towards positive/negative output. (b) When S_A and/or S_B is SPWM-OFF, C_L shall supply energy for R_L alone. The topology is shown in Fig. 3(d) so as to keep V_o holding there temporarily.

By making use of Phase I and II in cyclical operation, it is reasonably expected that the AC voltage range of V_o can be converted into $+[(n+1)/(1-D)]\cdot V_S\sim -[(n+1)/(1-D)]\cdot V_S$. For instance, when $V_S=24\text{V}$, $n=2$, $D=0.5$, V_o will be boosted into $+144\text{V}\sim -144\text{V}$ (100Vrms).

III. Modeling and Analysis

In this section, the CICWSC's modeling is discussed. Let the whole derivation be partitioned into two discussions as: modeling heading for negative output/heading for positive output, and then let them be merged together for the complete formulation. Before it begins, let's adopt an equivalence to be as the modeling of the coupled-inductor device, including

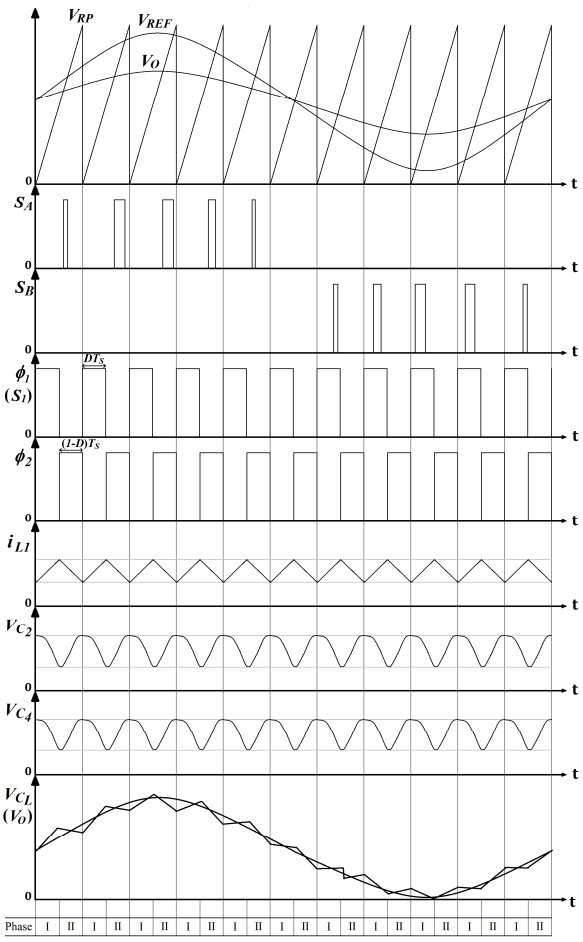

Fig. 2. Theoretical waveforms of CICWSC.

magnetizing inductor L_m and leakage inductor L_k, where $L_m=k\sqrt{L_1L_2}/n$ and $L_k=2(1-k)\cdot L_1$ (k : coupling coefficient, $0\le k\le 1$). For simplifying the complexity, almost perfectly coupling is assumed here, that is to say at $k\approx 1$, this device is with a negligibly small leakage L_k.

Firstly, the modeling heading for negative output will be discussed, i.e., C_1,C_2 are playing active roles. Based on Fig. 3(a),3(c),3(d), the effective circuits can be obtained as in Fig. 4(a)-4(c), and the related equations are formulated below.

(i) Phase I: Fig. 4(a)

$$\frac{\mathrm{d}[V_{C_1}(t)]}{\mathrm{d}t}=\frac{nV_S-V_{C_1}(t)-nR_A\cdot i_L(t)}{pR_BC}, \tag{1a}$$

$$\frac{\mathrm{d}[V_{C_L}(t)]}{\mathrm{d}t}=-\frac{V_{C_L}(t)}{R_LC_L}, \tag{1b}$$

$$\frac{\mathrm{d}[i_L(t)]}{\mathrm{d}t}=\frac{nR_A}{pR_BL_m}\cdot V_{C_1}(t)+\frac{V_S-R_A\cdot i_L(t)}{pL_m}, \tag{1c}$$

$$\frac{\mathrm{d}[V_{C_2}(t)]}{\mathrm{d}t}=0, \tag{1d}$$

$$V_o(t)=V_{C_L}(t), \tag{1e}$$

(ii) Phase II when S_B is SPWN-ON: Fig. 4(b)

$$\frac{\mathrm{d}[V_{C_1}(t)]}{\mathrm{d}t}=-\frac{i_L(t)}{(n+1)C}, \tag{2a}$$

$$\frac{\mathrm{d}[V_{C_L}(t)]}{\mathrm{d}t}=-\left(\frac{1}{R_L}+\frac{1}{R_D}\right)\cdot\frac{V_{C_L}(t)}{C_L}-\frac{V_{C_2}(t)}{R_DC_L}, \tag{2b}$$

$$\frac{\mathrm{d}[i_L(t)]}{\mathrm{d}t}=\frac{V_{C_1}(t)-V_{C_2}(t)+V_S}{(n+1)L_m}-\frac{R_{Cn}\cdot i_L(t)}{(n+1)^2L_m}, \tag{2c}$$

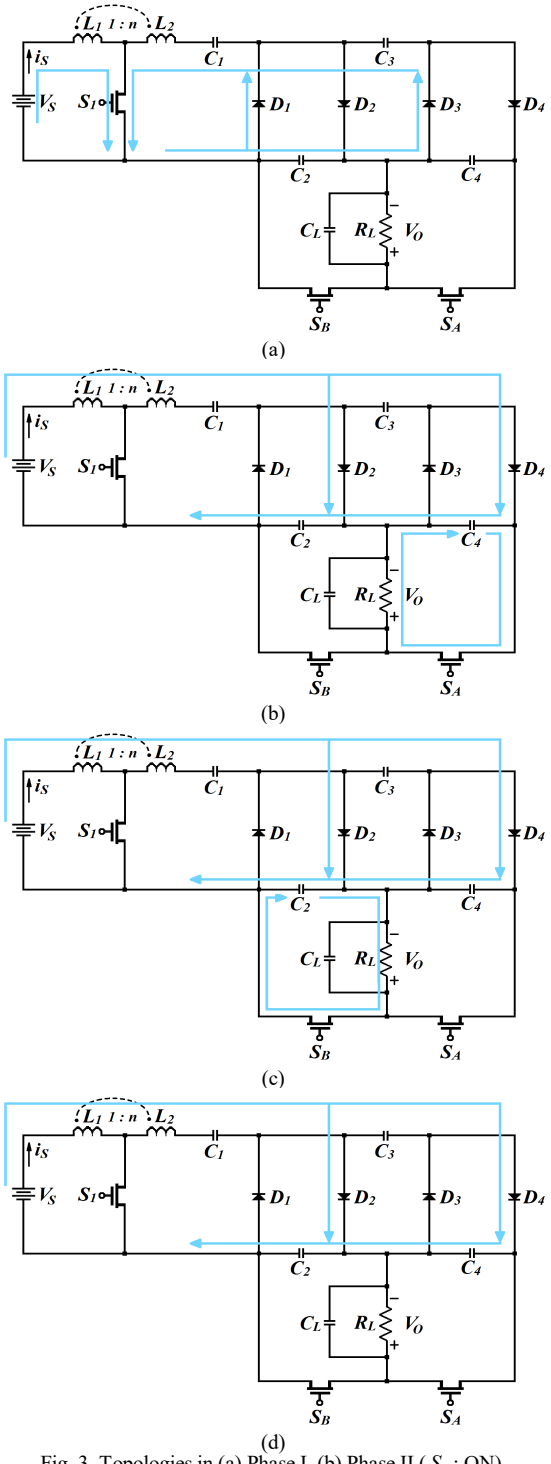

Fig. 3. Topologies in (a) Phase I, (b) Phase II (S_A : ON), (c) Phase II (S_B : ON), (d) Phase II (S_A, S_B : OFF).

$$\frac{\mathrm{d}[V_{C_2}(t)]}{\mathrm{d}t} = -\frac{V_{C_L}(t)+V_{C_2}(t)}{R_D C} + \frac{i_L(t)}{(n+1)C}, \tag{2d}$$

$$V_o(t) = V_{C_L}(t), \tag{2e}$$

(iii) Phase II when S_B is SPWN-OFF: Fig. 4(c)

$$\frac{\mathrm{d}[V_{C_1}(t)]}{\mathrm{d}t} = -\frac{i_L(t)}{(n+1)C}, \tag{3a}$$

$$\frac{\mathrm{d}[V_{C_L}(t)]}{\mathrm{d}t} = -\frac{V_{C_L}(t)}{R_L C_L}, \tag{3b}$$

$$\frac{\mathrm{d}[i_L(t)]}{\mathrm{d}t} = \frac{V_{C_1}(t)-V_{C_2}(t)+V_S}{(n+1)L_m} - \frac{R_{Cn}\cdot i_L(t)}{(n+1)^2 L_m}, \tag{3c}$$

$$\frac{\mathrm{d}[V_{C_2}(t)]}{\mathrm{d}t} = \frac{i_L(t)}{(n+1)C}, \tag{3d}$$

$$V_o(t) = V_{C_L}(t), \tag{3e}$$

where $R_A = r_T + r_1$, $R_B = r_C + r_D + r_T + r_2$, $R_{Cn} = 2r_C + r_D + r_1 + r_2$, $R_D = r_C + r_T$, $p = 1 + n^2 R_A / R_B$. V_{C_1}, V_{C_2}, V_{C_L}, V_o, i_L, i_S means the voltage across C_1, C_2, voltage across C_L, voltage across R_L, current through L_m, and current at the supply terminal, respectively. And then, by using state-space averaging (SSA), (i.e., $[DT_S\times(1) + x_n(1-D)T_S\times(2) + (1-x_n)(1-D)T_S\times(3)]/T_S$), the state equation heading for negative output can be derived as in (4), where x_n ($0 \le x_n \le 1$) is the duty cycle of S_B.

$$\frac{\mathrm{d}[x_N(t)]}{\mathrm{d}t} = A_N \cdot x_N(t) + B_N \cdot u(t), \tag{4a}$$

$$y(t) = C_N \cdot x_N(t), \tag{4b}$$

where

$$x_N(t) = [V_{C_1}(t) \quad V_{C_L}(t) \quad i_L(t) \quad V_{C_2}(t)]^T, \tag{5a}$$

$$u(t) = [V_S], \quad y(t) = [V_o(t)], \tag{5b,c}$$

$$A_N = \begin{bmatrix} -\frac{D}{pR_B C} & 0 & -\frac{K_F}{C} & 0 \\ 0 & -\frac{1}{C_L}\left(\frac{1}{R_L} + \frac{(1-D)x_n}{R_D}\right) & 0 & -\frac{(1-D)x_n}{R_D C_L} \\ \frac{K_F}{L_m} & 0 & -\frac{R_{En}}{L_m} & -\frac{1-D}{(n+1)L_m} \\ 0 & -\frac{(1-D)x_n}{R_D C} & \frac{1-D}{(n+1)C} & -\frac{(1-D)x_n}{R_D C} \end{bmatrix}, \tag{5d}$$

$$B_N = \begin{bmatrix} \frac{nD}{pR_B C} & 0 & \frac{K_G}{L_m} & 0 \end{bmatrix}^T, \tag{5e}$$

$$C_N = [0 \quad 1 \quad 0 \quad 0], \tag{5f}$$

$$R_{En} = D\cdot\frac{R_A}{p} + (1-D)\cdot\frac{R_{Cn}}{(n+1)^2}, \tag{5g}$$

$$K_F = D\cdot\frac{nR_A}{pR_B} + (1-D)\cdot\frac{1}{n+1}, \tag{5h}$$

$$K_G = D\cdot\frac{1}{p} + (1-D)\cdot\frac{1}{n+1}. \tag{5i}$$

Next, the modeling heading for positive output will be discussed, i.e., C_1, C_4 are playing active roles and C_2, C_3 are treated as energy buffers. Based on Fig. 3(a),3(b),3(d), the effective circuits are simplified as in Fig. 4(d)-4(f), and the related equations can also be formulated below.

(i) Phase I: Fig. 4(d)

$$\frac{\mathrm{d}[V_{C_1}(t)]}{\mathrm{d}t} = \frac{nV_S - V_{C_1}(t) - nR_A\cdot i_L(t)}{pR_B C}, \tag{6a}$$

$$\frac{\mathrm{d}[V_{C_L}(t)]}{\mathrm{d}t} = -\frac{V_{C_L}(t)}{R_L C_L}, \tag{6b}$$

$$\frac{\mathrm{d}[i_L(t)]}{\mathrm{d}t} = \frac{nR_A}{pR_B L_m}\cdot V_{C_1}(t) + \frac{V_S - R_A\cdot i_L(t)}{pL_m}, \tag{6c}$$

$$\frac{\mathrm{d}[V_{C_4}(t)]}{\mathrm{d}t} = 0, \tag{6d}$$

$$V_o(t) = V_{C_L}(t), \tag{6e}$$

(ii) Phase II when S_A is SPWN-ON: Fig. 4(e)

$$\frac{\mathrm{d}[V_{C_1}(t)]}{\mathrm{d}t} = -\frac{i_L(t)}{(n+1)C}, \tag{7a}$$

$$\frac{\mathrm{d}[V_{C_L}(t)]}{\mathrm{d}t} = -\left(\frac{1}{R_L} + \frac{1}{R_D}\right)\cdot\frac{V_{C_L}(t)}{C_L} + \frac{V_{C_4}(t)}{R_D C_L}, \tag{7b}$$

ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

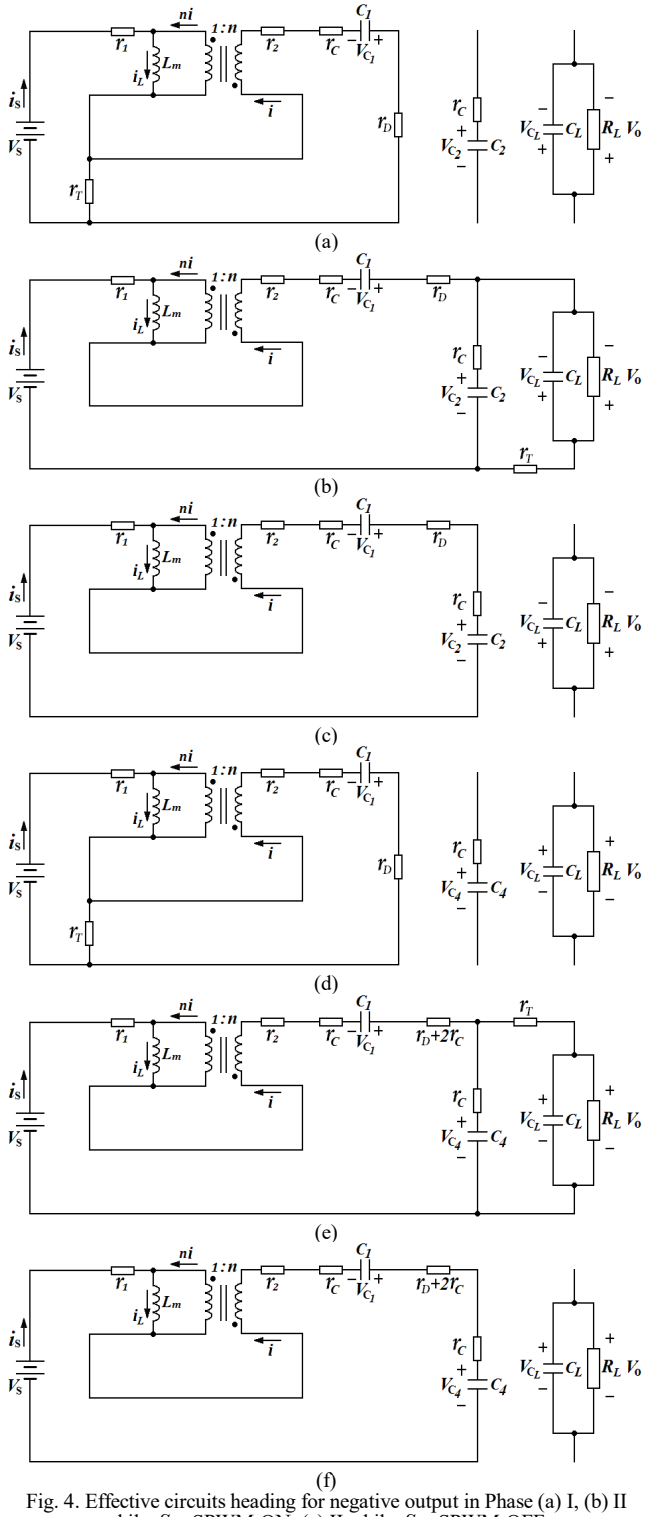

Fig. 4. Effective circuits heading for negative output in Phase (a) I, (b) II while S_B: SPWM-ON, (c) II while S_B: SPWM-OFF; Effective circuits heading for positive output in Phase (d) I, (e) II while S_A: SPWM-ON, (f) II while S_A: SPWM-OFF.

$$\frac{\mathrm{d}[i_L(t)]}{\mathrm{d}t}=\frac{V_{C_1}(t)-V_{C_4}(t)+V_S}{(n+1)L_m}-\frac{R_{Cp}\cdot i_L(t)}{(n+1)^2L_m}, \tag{7c}$$

$$\frac{\mathrm{d}[V_{C_4}(t)]}{\mathrm{d}t}=\frac{V_{C_L}(t)-V_{C_4}(t)}{R_DC}+\frac{i_L(t)}{(n+1)C}, \tag{7d}$$

$$V_o(t)=V_{C_L}(t), \tag{7e}$$

(iii) Phase II when S_A is SPWN-OFF: Fig. 4(f)

$$\frac{\mathrm{d}[V_{C_1}(t)]}{\mathrm{d}t}=-\frac{i_L(t)}{(n+1)C}, \tag{8a}$$

$$\frac{\mathrm{d}[V_{C_L}(t)]}{\mathrm{d}t}=-\frac{V_{C_L}(t)}{R_LC_L}, \tag{8b}$$

$$\frac{\mathrm{d}[i_L(t)]}{\mathrm{d}t}=\frac{V_{C_1}(t)-V_{C_4}(t)+V_S}{(n+1)L_m}-\frac{R_{Cp}\cdot i_L(t)}{(n+1)^2L_m}, \tag{8c}$$

$$\frac{\mathrm{d}[V_{C_4}(t)]}{\mathrm{d}t}=\frac{i_L(t)}{(n+1)C}, \tag{8d}$$

$$V_o(t)=V_{C_L}(t), \tag{8e}$$

where $R_{Cp}=4r_C+r_D+r_1+r_2$ and V_{C_4} is the voltage across C_4. Similarly, by using SSA skill (i.e., $[DT_S\times(6)+x_p(1-D)T_S\times(7)+(1-x_p)(1-D)T_S\times(8)]/T_S$), the state equation heading for positive output is also derived as in (9), where x_p ($0\le x_p\le 1$) is the duty cycle of S_A.

$$\frac{\mathrm{d}[x_P(t)]}{\mathrm{d}t}=A_P\cdot x_P(t)+B_P\cdot u(t), \tag{9a}$$

$$y(t)=C_P\cdot x_P(t), \tag{9b}$$

where

$$x_P(t)=[V_{C_1}(t)\quad V_{C_L}(t)\quad i_L(t)\quad V_{C_4}(t)]^T, \tag{10a}$$

$$A_P=\begin{bmatrix}-\frac{D}{pR_BC} & 0 & -\frac{K_F}{C} & 0\\ 0 & -\frac{1}{C_L}\left(\frac{1}{R_L}+\frac{(1-D)x_p}{R_D}\right) & 0 & +\frac{(1-D)x_p}{R_DC_L}\\ \frac{K_F}{L_m} & 0 & -\frac{R_{Ep}}{L_m} & -\frac{1-D}{(n+1)L_m}\\ 0 & +\frac{(1-D)x_p}{R_DC} & \frac{1-D}{(n+1)C} & -\frac{(1-D)x_p}{R_DC}\end{bmatrix}, \tag{10b}$$

$$B_P=\begin{bmatrix}\frac{nD}{pR_BC} & 0 & \frac{K_G}{L_m} & 0\end{bmatrix}^T, \tag{10c}$$

$$C_P=[0\quad 1\quad 0\quad 0], \tag{10d}$$

$$R_{Ep}=D\cdot\frac{R_A}{p}+(1-D)\cdot\frac{R_{Cp}}{(n+1)^2}. \tag{10e}$$

Finally, for ease of expression of AC output, define a new integrated duty-cycle variable x_{ac} ($-1\le x_{ac}\le 1$) as follows: (i) $x_{ac}=+x_p$ if $V_{REF}>V_o$ (heading for positive output via use of S_A), and (ii) $x_{ac}=-x_n$ if $V_{REF}<V_o$ (heading for negative output via use of S_B). Based on (4) and (9), plus by the aid of x_{ac}, the complete modeling of CICWSC can be derived as in (11), where V_{C_B} is the average of voltages across bridge capacitors C_2 and C_4 (i.e., $V_{C_B}(t)=[V_{C_2}(t)+V_{C_4}(t)]/2$). This modeling can help solving future questions of theoretical analysis and control design.

$$\frac{\mathrm{d}[x_{INV}(t)]}{\mathrm{d}t}=A_{INV}\cdot x_{INV}(t)+B_{INV}\cdot u(t), \tag{11a}$$

$$y(t)=C_{INV}\cdot x_{INV}(t), \tag{11b}$$

where

$$x_{INV}(t)=[V_{C_1}(t)\quad V_{C_L}(t)\quad i_L(t)\quad V_{C_B}(t)]^T, \tag{12a}$$

$$A_{INV}=\begin{bmatrix}-\frac{D}{pR_BC} & 0 & -\frac{K_F}{C} & 0\\ 0 & -\frac{1}{C_L}\left(\frac{1}{R_L}+\frac{(1-D)|x_{ac}|}{R_D}\right) & 0 & \frac{(1-D)x_{ac}}{R_DC_L}\\ \frac{K_F}{L_m} & 0 & -\frac{R_E}{L_m} & -\frac{1-D}{(n+1)L_m}\\ 0 & \frac{(1-D)x_{ac}}{R_DC} & \frac{1-D}{(n+1)C} & -\frac{(1-D)|x_{ac}|}{R_DC}\end{bmatrix}, \tag{12b,c}$$

$$B_{INV}=\begin{bmatrix}\frac{nD}{pR_BC} & 0 & \frac{K_G}{L_m} & 0\end{bmatrix}^T,$$

ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

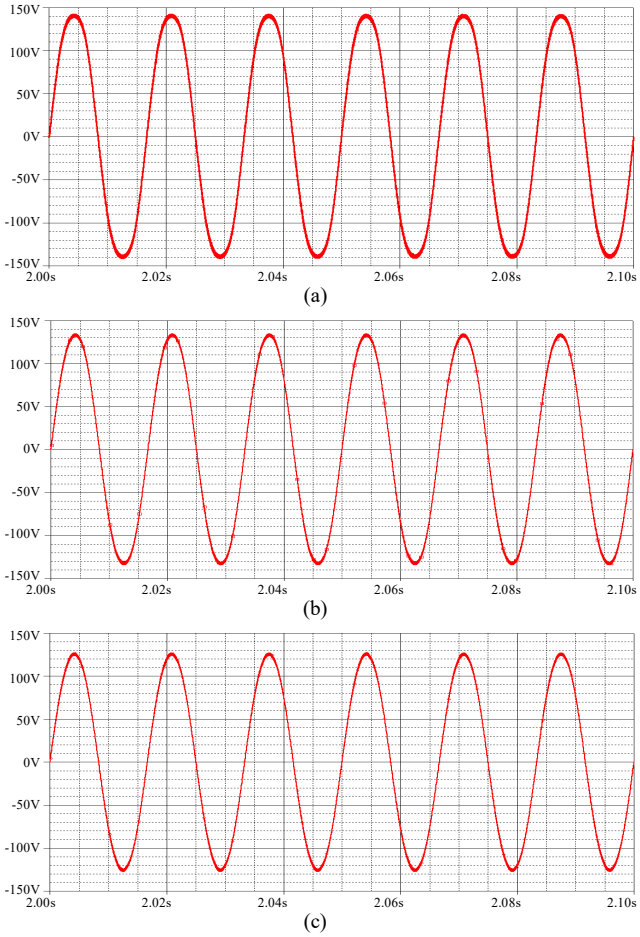

Fig. 5. Simulation: V_o for V_{REF} :
(a) 145Vpeak,60Hz; (b) 135Vpeak,60Hz; (c) 125Vpeak,60Hz.

$$C_{INV} = [0 \quad 1 \quad 0 \quad 0], \tag{12d}$$

$$R_E = (R_{Ep} + R_{En})/2 . \tag{12e}$$

For the steady-state analysis, let $\mathrm{d}[x_{INV}(t)]/\mathrm{d}t = 0$ of (11), and the analytical solution to the steady-state response V_o can be obtained as

$$V_o = (-C_{INV} A_{INV}^{-1} B_{INV}) \cdot u = \frac{n+1}{1-D} \times \frac{x_{ac}}{|x_{ac}|} \cdot V_S \cdot \frac{1}{1+R_o/R_L}, \tag{13a}$$

$$R_o = \frac{R_D}{(1-D)|x_{ac}|} + \frac{(n+1)^2 R_E}{(1-D)^2} + \frac{(n+1)^2 K_F{}^2 p R_B}{D(1-D)^2} . \tag{13b}$$

As (13a) shows, V_o can really be regulated by n and D. If n and/or D increases, V_o will gain a higher output voltage. Here, the voltage conversion ratio (VCR, i.e., boosting gain) can be suggested as

$$M_{INV} = \frac{|V_o|}{V_S} = \frac{n+1}{1-D} \cdot \frac{1}{1+R_o/R_L} . \tag{14}$$

Because r_C, r_D, r_T are generally at the level of mΩ and R_L is about at ten Ω (or bigger), that is to say $R_o << R_L$, there is no doubt that M_{INV} will be close to $(n+1)/(1-D)$. When $x_{ac} = +1 / x_{ac} = -1$, V_o can be converted to the max/min value: $+M_{INV} V_S / -M_{INV} V_S$. Thus, it shows that the output range of CICWSC is $+M_{INV} V_S \sim -M_{INV} V_S$ (i.e., $+[(n+1)/(1-D)] \cdot V_S \sim -[(n+1)/(1-D)] \cdot V_S$).

IV. Examples

In the following examples, the inverter design of CICWSC is performed through Pspice for circuit simulation, and its prototype is implemented for circuit test. Firstly, this inverter is designed in accordance with the structure of Fig. 1. The basic inversion is from DC 24V to AC 100Vrms, 60Hz, and the used parameters are shown below: $f_S = 50\text{kHz}$, $R_L = 500\Omega$, $C = 47\mu F$, $C_L = 1.5\mu F$, $L_m = 80\mu H$, $r_1 = 0.01\Omega$, $r_2 = 0.04\Omega$, $n = 2$, $r_C = 0.03\Omega$, $r_T = r_D = 0.01\Omega$. Via OrCAD Pspice, the circuit simulation is performed for the steady-state response under

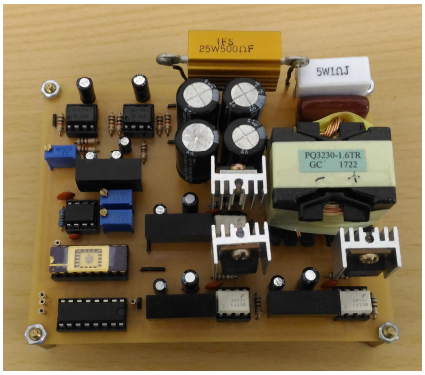

Fig. 6. CICWSC prototype circuit.

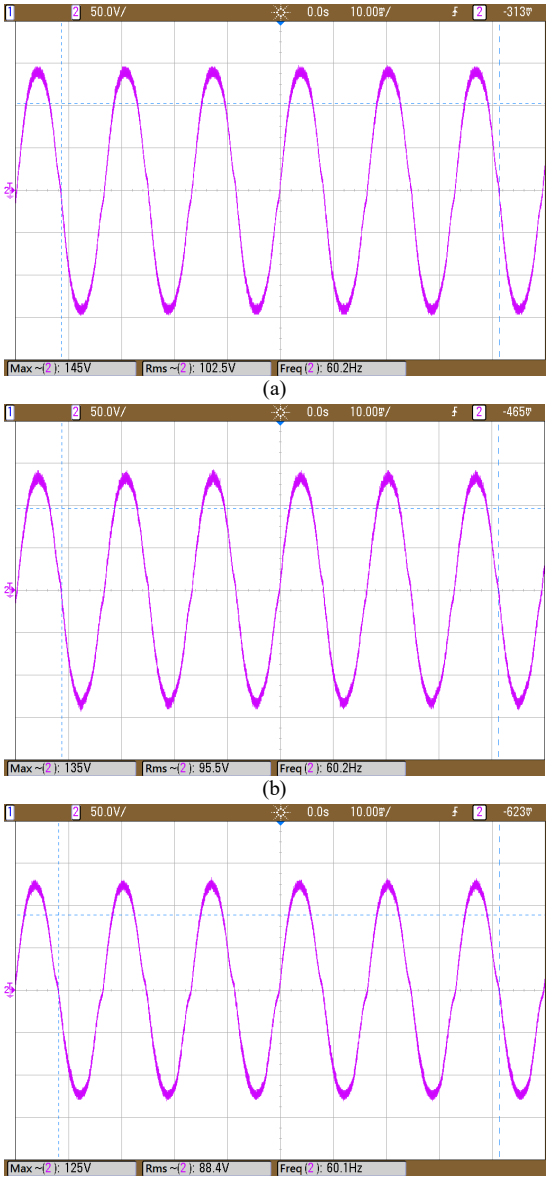

Fig. 7. Experiment: V_o for V_{REF} :
(a) 145Vpeak,60Hz; (b) 135Vpeak,60Hz; (c) 125Vpeak,60Hz.

ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

various references. Fig. 5(a)-5(c) show the waveforms of V_o for V_{REF} : 145Vpeak,60Hz, 135Vpeak,60Hz, 125Vpeak,60Hz, respectively. It is observed that this inverter remains stable to provide a sinusoidal output, and both output amplitude and output frequency of V_o can keep on following V_{REF} indeed. Through the simulation, the validity of the analytic result about VCR of (14) can be verified.

Next, the experiments will be considered. Fig. 6 shows the prototype circuit of CICWSC (board size: $11.5\text{cm} \times 9.5\text{cm}$). The parameters in this circuit are shown below: $V_S = 24\text{V}$, $f_S = 40\text{kHz}$, $R_L = 500\Omega$, $C = 47\mu\text{F}$, $C_L = 1\mu\text{F}$, $L_m = 80m\text{H}$, $n = 2$, IRF840 power MOSFET, 6N137 MOS photocoupled driver (Agilent 54830B oscilloscope). Via test on this prototype, the circuit experiment is performed for the steady-state response under the different references. Fig. 7(a)-7(c) demonstrate the waveforms of V_o for V_{REF} : 145Vpeak,60Hz, 135Vpeak,60Hz, 125Vpeak,60Hz, respectively. It is observed that the prototype circuit of CICWSC remains stable and provides a sinusoidal output. Indeed, both output amplitude and output frequency of V_o can keep on following V_{REF} .

V. Conclusion

This study presents the detailed mathematical derivation of system modeling and steady-state analysis of CICWSC inverter. The power part of CICWSC, including CI booster, CWSC doubler, and HBDL in cascade from supply *Vs* to output *Vo*, is capable of providing a wide range of DC-AC gain as: +(*n*+1)/(1-*D*)~−(*n*+1)/(1-*D*) (*n*: turn ratio of coupled inductor, *D*: ratio cycle of inductor-charging). Firstly, the state equations related to those effective circuits heading for negative/positive output are formulated individually. Next, by merging the two sets of state equations, the complete modeling of CICWSC can be derived. It is much helpful to future analysis and design. With the help of this modeling, the boosting gain (i.e., VCR) is proven through steady-state analytic discussions. Finally, some simulation/experiment cases are discussed, and all results are illustrated/verified on the prototype circuit to confirm the efficacy of CICWSC's modeling. Here, this study has gained some merits as listed below. (i) As section 4 presents, this CICWSC is able to successfully perform the DC-AC conversion from DC 24V to AC 100Vrms, 60Hz. Indeed, it can attain the max/min gain of ± 6 times, as expected in the analytic discussions. (ii) Apart from one coupled inductor, in nature, this CICWSC belongs to the kind of SC circuit. Thus, it is a promising future to implement SC-based power converter on a chip. (iii) As equation (13a) mentioned before, V_o will gain a higher output voltage if n and/or D increases. For lifting the total gain more, it is feasible to increase n , D , or even to extend the stage number of CWSC doubler in this CICWSC.

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ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)