Controller Chip Design of Multiphase Switched-Capacitor Coupled-Inductor Converter

Yuen-Haw Chang and En-Ping Jhao

***Abstract*—This paper presents the controller chip design/ implementation applied to the multiphase switched-capacitor coupled-inductor (MSCCI) converter for the high-gain DC-DC conversion. In this MSCCI, the plant is composed of a three-stage SC booster and an added coupled inductor, aiming at the boost power conversion from DC 5V to DC 220V. Here, using the multiphase operation is much helpful to reduce the number of devices used. In achieving the goal, the controller is designed to include pulse-width-modulation (PWM) compensator, non-overlapping circuit, and phase generator, and its integrated circuit is planned for layout with the tool of Cadence through pre/post-layout design. Then, with technical assistance from Chip Design & Implementation Center (CIC), this controller is implemented on a chip (no.: D35-105C-E0020, TSMC 0.35μm 2P4M, 1500×1500μm^2, 5V, 0.528mW, max frequency 200kHz, 18S/B). At the end, several simulation/experiment examples of MSCCI are considered, and the results are illustrated/verified on the prototype circuit to present the efficacy.**

***Terms*—high-gain DC-DC conversion, multiphase operation, switched-capacitor (SC), coupled-inductor (CI), chip design and implementation.**

I. Introduction

For the sake of the advantage of device simplification, the kind of switched-capacitor (SC) power converter has received more attention from researchers recently. The SC-based circuit, just containing semi-switches and capacitors, always comes with compact size/light weight because there is no need to use bulky magnetic device. Till now, this kind of SC has been applied to many applications of module drivers, e.g., LCD, Flash LED, EEPROM, etc. In 1976, Dickson built up NMOS integrated circuits for high-voltage output based on SC multiplier technique. But, some weaknesses included big area and fixed gain [1]. Since the 1990s, Ioinovici had suggested many novel SC-based converters by using the idea of SC-bank interleaving, and presented some discussions about steady-state characteristics [2-3]. In the same period, a canonical converter of *n*-stage Makowski was proposed, and the gain is limited to the (*n*+1)th Fibonacci number [4]. In 2001, a multiphase-based converter of *n*-stage Starzyk was presented, and the step-up gain is lifted to 2^n at most, i.e., it uses fewer capacitors under some given gain [5]. For the past few years, Chang *et al.* built up several schemes of new SC power converters for the use of DC-DC/DC-AC [6-8]. Going a further step, the idea of the coupled inductor is adopted and combined with SC for a more flexible arrangement of step-up gain [9-11]. In this paper, we try to present the controller chip design/implementation of MSCCI for the success of multiphase operation, so as to achieve the high-gain DC-DC conversion.

Manuscript received June 28, 2021. This work is supported by Ministry of Science and Technology of Taiwan, under Grant MOST 109-2221-E-324-027.
Yuen-Haw Chang is a professor of Dep. of Computer Science and Information Engineering, Chaoyang University of Technology (CYUT), Taichung, Taiwan, post code: 413. (email: cyhfyc@cyut.edu.tw). En-Ping Jhao was a research assistant at CYUT (email: s10427616@gm.cyut.edu.tw).

II. Configuration of MSCCI

Fig. 1 shows the entire scheme of MSCCI, composed of plant and controller, running together for the task of high-gain DC-DC conversion [10]. As in the top half, the plant consists of a three-stage SC booster and one coupled inductor between supply V_S and output V_o, including three pumping capacitors C_1, C_2, C_3, one coupled inductor L_1, L_2 (L_1:L_2=1:n^2, turn ratio $n = N_2/N_1$), five switches $S_1 - S_5$, diodes $D_1 - D_4$, a load resistor R_L, and an output capacitor C_o. As shown in the bottom half, the controller consists of PWM compensator, non-overlapping circuit, and phase generator, in charge of performing multiphase operation (to manipulate switches for various topologies) and enhancing regulation capability (to keep V_o on following various references V_{ref}). Fig. 2 shows the relevant waveforms in a multiphase cycle T_M. Each T_M has four steps (Step I_0, I_1, I_2, I_3), and each step includes two phases (Phase I, II) for the respective periods as: DT_S, $(1-D)T_S$, where $T_M = 4T_S$, $T_S = 1/f_S$ (f_S: switching freq. of ramp V_{rp}), and D is the PWM duty cycle ($0 < D < 1$). Next, the details of the steps/phases are introduced as follows.

(i) Step I_0:
- (a) Phase I: turn on S_1. D_1 is biased on and $D_2 - D_4$ are off. The current is flowing as shown in Fig. 3(a). L_1 is being charged by V_S, and is transferring energy into L_2 for heading towards $V_{L1} \approx V_S$, $V_{L2} \approx nV_S$. About the same time, L_2 is connected in series with V_S for pumping V_{C1} up to $(n+1)V_S$ ($V_S + V_{L2} \rightarrow V_{C1}$). At the endpoint, C_o stands alone to supply R_L.
- (b) Phase II: turn on S_2. D_2 is on and D_1, D_3, D_4 are off. The current is flowing as shown in Fig. 3(b). L_1, L_2 are being discharged in series with V_S, V_{C1} together for charging C_2 ($V_S + V_{L1} + V_{L2} + V_{C1} \rightarrow V_{C2}$). Based on the booster's theory, V_{L1} is reaching $DV_S/(1-D)$ as operating at D, and then V_{L2} is moving towards $nDV_S/(1-D)$. Thus, V_{C2} can be boosted to the value: $[(n+1)+(1+nD)/(1-D)]\cdot V_S$. At the endpoint, C_o still stands alone to supply R_L.

(ii) Step I_1:
- (a) Phase I: the same as Phase I of Step I_0.

ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

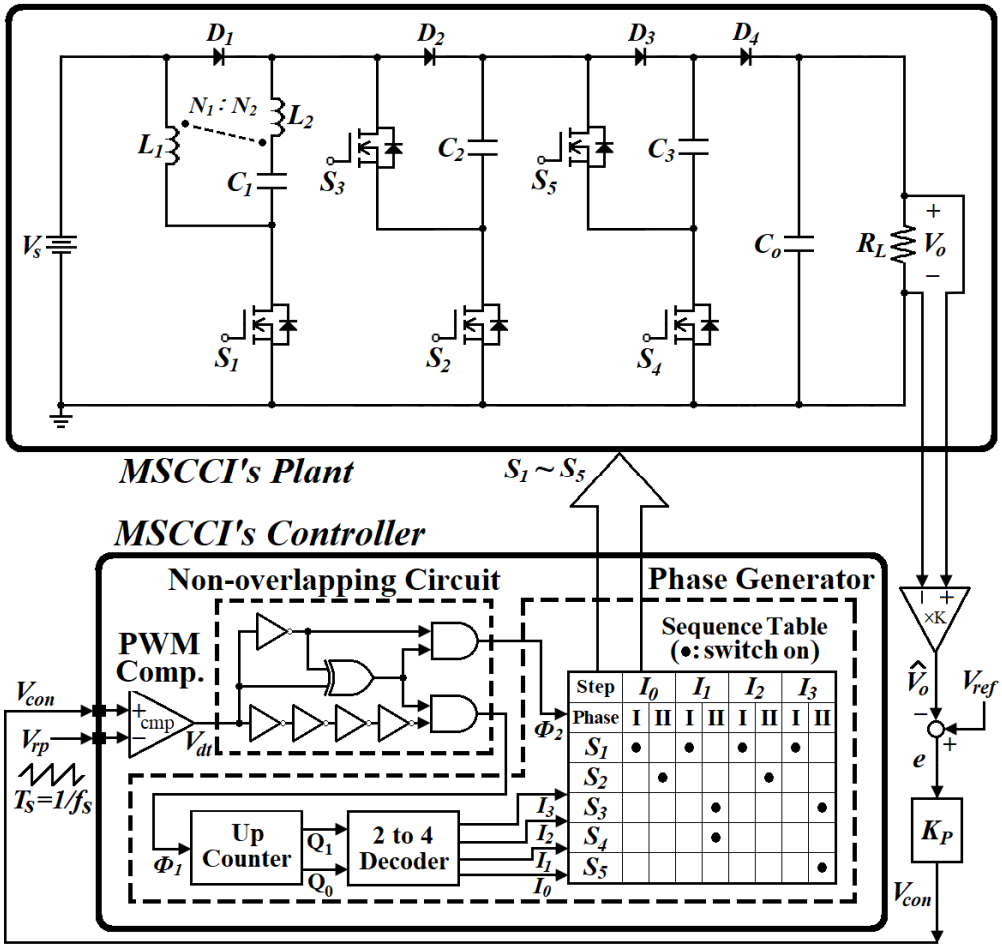


Fig. 1. Configuration of MSCCI.

(b) Phase II: turn on S_3,S_4. D_3 is on and D_1,D_2,D_4 are off. The current is flowing as shown in Fig. 3(c). L_1, L_2 are being discharged in series with V_S, V_{C1}, V_{C2} for charging C_3 ($V_S + V_{L1} + V_{L2} + V_{C1} + V_{C2} \rightarrow V_{C3}$). In other words, V_{C3} can be boosted to two times voltage of V_{C2} as $2\cdot[(n+1)+(1+nD)/(1-D)]\cdot V_S$. At the same time, C_o still stands alone to supply R_L.

(iii) Step I_2:

(a) Phase I: the same as Phase I of Step I_0.

(b) Phase II: the same as Phase II of Step I_0.

(iv) Step I_3:

(a) Phase I: the same as Phase I of Step I_0.

(b) Phase II: turn on S_3,S_5. D_4 is on and $D_1 - D_3$ are off. The current is flowing as in Fig. 3(d). L_1, L_2 are both being discharged in series with V_S, V_{C1}, V_{C2}, V_{C3} for supplying C_o ($V_S + V_{L1} + V_{L2} + V_{C1} + V_{C2} + V_{C3} \rightarrow V_{Co}$) and load R_L. Similarly, V_{Co} can be boosted to two times voltage of V_{C3} as $4\cdot[(n+1)+(1+nD)/(1-D)]\cdot V_S$.

By repeating the multiphase operation cyclically, the total gain of $4\cdot[(n+1)+(1+nD)/(1-D)]$ can be achieved. By the way, the extended gain could be expected to attain the level as: $2^{m-1}\cdot[(n+1)+(1+nD)/(1-D)]$, where m means the number of pumping capacitors.

III. Controller and Chip Design

At the beginning, the details of the MSCCI's controller (composed of PWM compensator, non-overlapping circuit, and phase generator) are introduced as follows.

(i) PWM compensator:

Firstly, let V_o be attenuated/filtered through a low-pass buffer, so as to obtain a signal-level output $\hat{V}_o$. And then, let $\hat{V}_o$ be subtracted with V_{ref} via an OPA-based subtracter, so as to obtain an error signal e. Then, let e be send through a proportional gain K_P, so as to obtain the control signal V_{con}. In the following, this V_{con} is entering the controller chip, and is compared with a ramp V_{rp} via an analog comparator, so as to obtain the pulse signal V_{dt}, possessed of duty cycle D for PWM. The main work is to generate D ($0 < D < 1$) according to the difference between V_{ref} and $\hat{V}_o$.

(ii) Non-overlapping circuit:

The non-overlapping circuit is made up of some logic gates (NOT/AND/XOR) not only to generate a pair of anti-phase signals, but also to avoid any overlapping of being logic-HIGH concurrently. Here, let V_{dt} be send through this circuit, so as to obtain a pair of anti-phase signals Φ_1, Φ_2. As $\Phi_1 = 1, \Phi_2 = 0$, it means Phase I for the duration of DT_S. As $\Phi_1 = 0, \Phi_2 = 1$, it means Phase II

ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

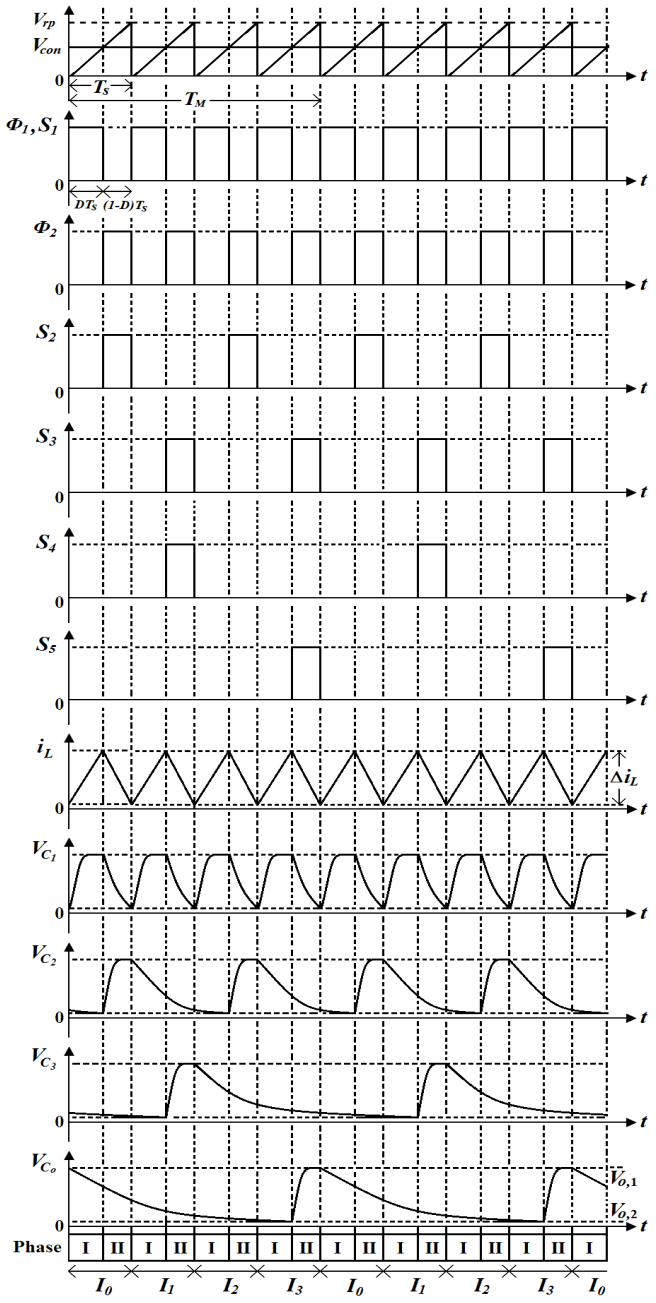


Fig. 2. Theoretical waveforms of MSCCI.

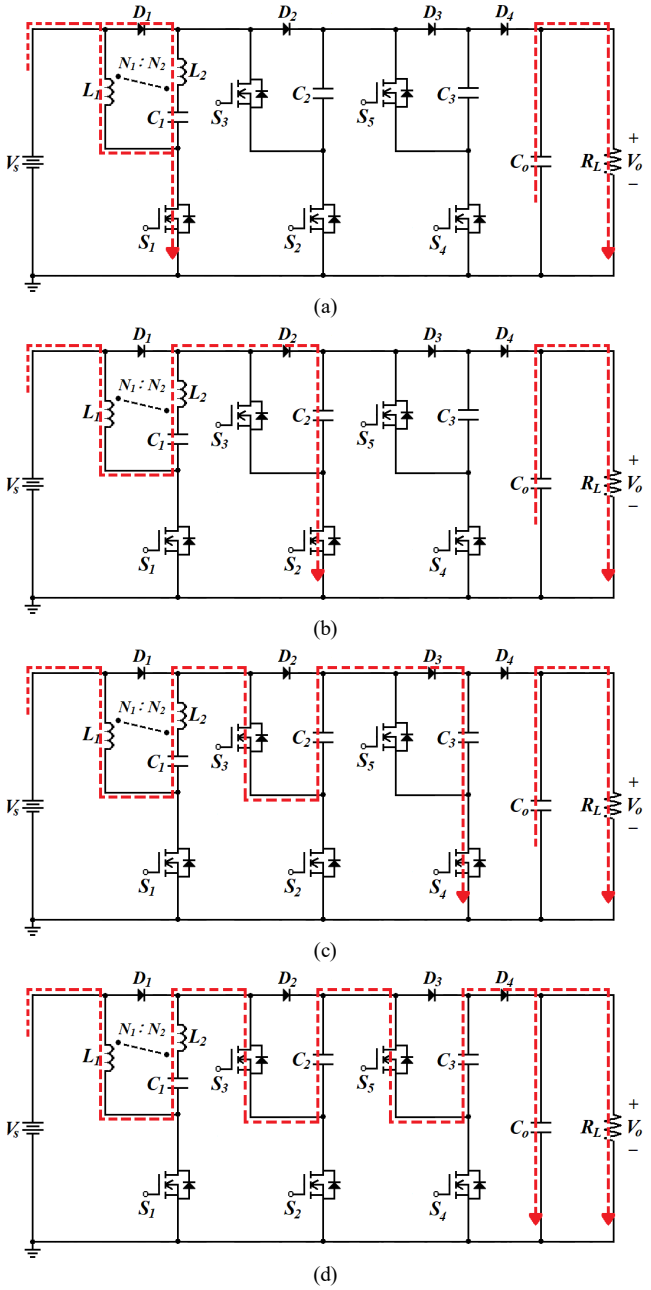


Fig. 3. Topologies for (a) Phase I of Step I_0, I_1, I_2, I_3, (b) Phase II of Step I_0, I_2, (c) Phase II of Step I_1, (d) Phase II of Step I_3.

for the duration of $(1-D)T_S$. These signals Φ_1, Φ_2 can be used for the base of phase control in the next block—phase generator.

(iii) Phase generator:

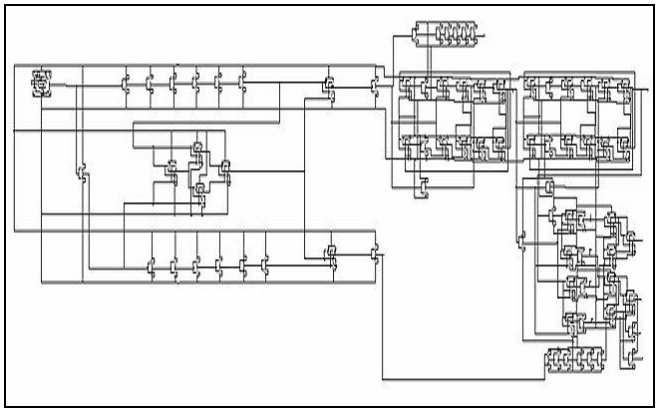
Now, let Φ_1 be used as a trigger signal, and be send through the 2-bit up counter (made of flip flops) so as to obtain $Q_1, Q_0 : 00 \to 01 \to 10 \to 11 \to \cdots$ repeatedly. And then, let Q_1, Q_0 be decoded by the 2 to 4 decoder, so as to obtain a set of step indicators: $I_0, I_1, I_2, I_3 : 1000 \to 0100 \to 0010 \to 0001 \to \ldots$ repeatedly. Then, according to the relationship shown in the sequence table of Fig. 1, the driver signals of switches $S_1 - S_5$ can be integrated by combining these signals Φ_1, Φ_2, I_0, I_1, I_2, I_3, and their related Boolean functions are summarized and listed as: $S_1 = \Phi_1$, $S_2 = (I_0 + I_2) \cdot \Phi_2$, $S_3 = (I_1 + I_3) \cdot \Phi_2$, $S_4 = I_1 \cdot \Phi_2$, $S_5 = I_3 \cdot \Phi_2$. The main work of this block is to generate $S_1 - S_5$, exactly like the waveforms of Fig. 2, for realizing the multiphase operation.

Next, in light of the MSCCI's controller mentioned above, we adopt Cadence software (i.e., Composer/Hspice/Virtuoso/ Calibre) to perform full-custom process for the chip design. In this process, there are two essential items as: pre-layout design and post-layout design. The details of these designs are introduced as follows.

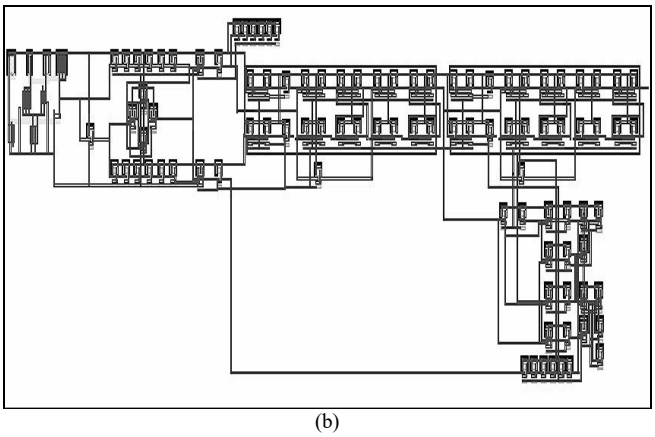
(i) Pre-layout design: (i.e., process before layout)

Based on the structure as in the bottom half of Fig. 1, we use Composer-Schematic to sketch the circuit-level diagram as shown in Fig. 4(a), containing a total of 237 MOSFETs (NOT/AND/XOR/analog comparator). And then, we can use Composer-Export to obtain an original Netlist file (.sp) of this circuit. Then, under the technology document of TSMC 0.35μm, we can add some signals (input/supply/ ground) to this file, so as to obtain a modified Netlist file (.sp). And then, we can use Hspice

ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)



(a)



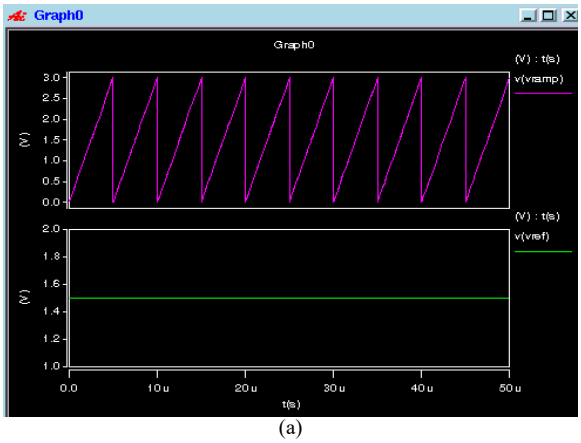
(b)

Fig. 4. Circuit design via (a) Composer-Schematic, (b) Virtuoso-Layout.

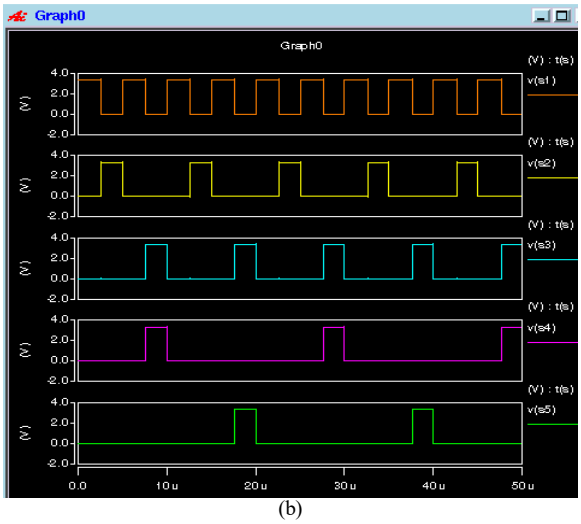
to run this modified Netlist file (.sp) for pre-layout simulation (Pre-Sim). Fig. 5(a)-5(b) show the Pre-Sim results, including the input signals (V_{rp}, V_{con}) and the output signals (S_1, S_2, S_3, S_4, S_5). Apparently, these waveforms are very much similar to those of Fig. 2. Thus, it shows that the pre-layout design is fit for purpose.

(ii) Post-layout design: (i.e., process after layout)

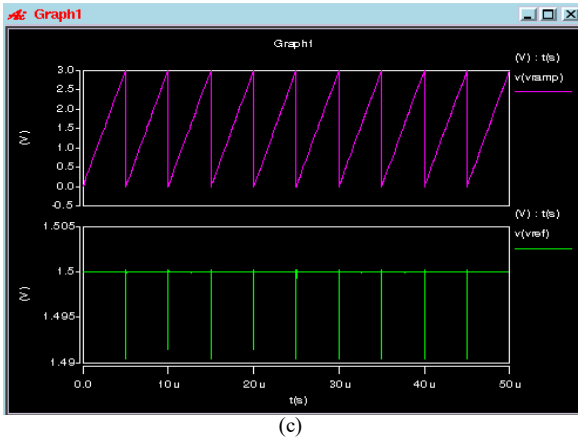
According to the circuit as illustrated in Fig. 4(a), we use Virtuoso-Layout to sketch the physic-level diagram as shown in Fig. 4(b), containing all of the device layouts (NOT/AND/XOR/analog comparator) under the analog CMOS design of TSMC 0.35μm 2P4M. Here, we adopt the multi-fingered layout for the increase in the ratio of width to length of MOS channel, so as to empower the capacity of electrical current, especially for the analog comparator. Then, we can use Virtuoso-Export to obtain a Photomask file (.gds) of the circuit layout. Next, we use Calibre-DRC to check this Photomask file (.gds), use Calibre-LVS to examine the correspondence between this Photomask file (.gds) and the original Netlist file (.sp), and then use Calibre-PEX to extract the parasitic from the circuit layout. After that, a post-layout Netlist file (.sp) can be obtained. Under the technology document of TSMC 0.35μm, we can add some signals (input/supply/ground) to this file, so as to obtain a modified post-layout Netlist file (.sp). Similarly, we use Hspice to run this modified post-layout Netlist file (.sp) for post-layout simulation (Post-Sim). Fig. 5(c)-5(d) show the Post-Sim results, including the input signals (V_{rp}, V_{con}) and the output signals (S_1, S_2, S_3, S_4, S_5). Clearly,



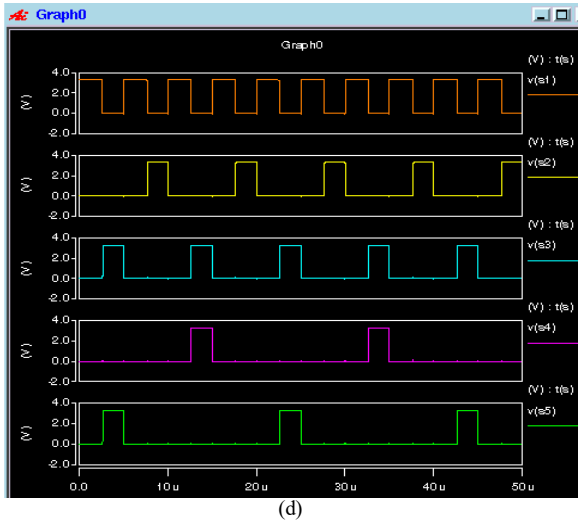
(a)



(b)



(c)



(d)

Fig. 5. Pre-Sim: (a) input signals (V_{rp}, V_{con}), (b) output signals ($S_1 - S_5$); Post-Sim: (c) input signals (V_{rp}, V_{con}), (d) output signals ($S_1 - S_5$).

ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

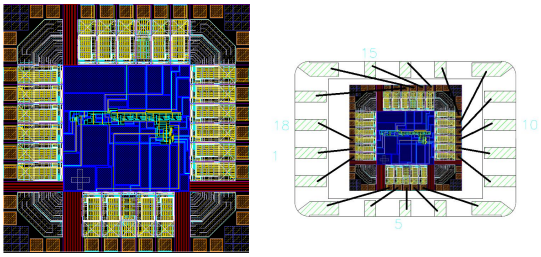
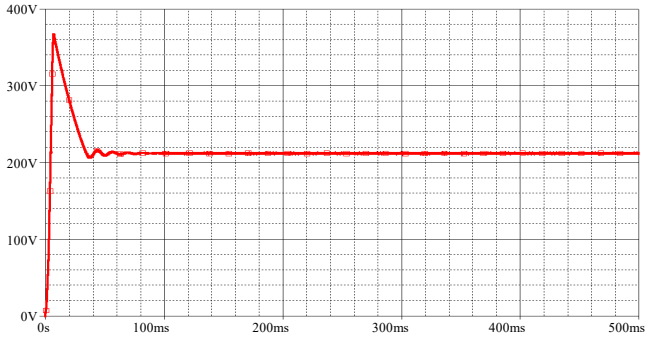
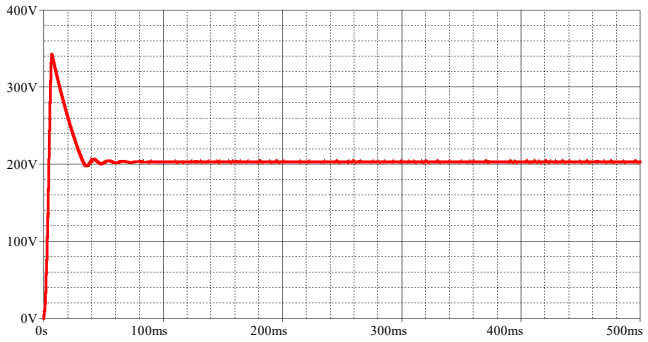


Fig. 6 Layout and wire-bonding package of D35-105C-E0020.



(a)



(b)

Fig. 7. Simulation results: V_o for (a) $V_{ref} = 210\text{V}$, (b) $V_{ref} = 200\text{V}$.

these waveforms are similar to those of Fig. 2. It shows that the post-layout design is fit for purpose. Finally, we shall submit all the required documents of this chip design to Chip Design & Implementation Center (CIC) of Taiwan for the chip fabrication. After examined and accepted by CIC, this chip design will be sent to TSMC foundry for chip tape-out. Fig. 6 shows the layout and wire-bonding package of this controller chip via full-custom fabrication of TSMC (no.: D35-105C-E0020, TSMC 0.35μm 2P4M, 1500×1500μm^2, 5V, 0.528mW, max frequency 200kHz, 18S/B).

IV. Examples of MSCCI

In this section, we will use OrCAD Pspice to complete the design of MSCCI for the circuit simulation and implement the prototype circuit for the circuit experiment, so as to check the steady-state performance. Firstly, based on the structure as demonstrated in Fig. 1, this converter circuit is made via OrCAD for achieving the goal of the rated conversion from DC 5V into DC 220V. After some test via the software, the circuit parameters are selected below: $V_S = 5\text{V}$, $R_L = 0.5\text{k}\Omega$, $f_S = 50\text{kHz}$, $D_o = 0.5$, $C = 100\mu F$, $C_o = 100\mu F$, $L_1 = 40\mu H$, $L_2 = 640\mu H$, $n = 4$, $r_1 = 0.002\Omega$, $r_2 = 0.032\Omega$, $r_D = r_C = 1m\Omega$, $r_T = 0.5m\Omega$. According to these circuit parameters, we can conduct the Pspice simulation to evaluate the steady-state performance of this MSCCI for the different references. Fig. 7 shows the respective waveforms of V_o for $V_{ref} = 210\text{V}$, 200V. It is obvious that the converter is working in the stable status and V_o is keeping on the track of V_{ref}. Further, it is found that the step-up gain is close to 42 times indeed (210/5=42). Secondly, some experiments are discussed in the following. Fig. 8 shows the implemented prototype circuit of MSCCI converter (board size: $18cm \times 22cm$). The circuit parameters are listed as: $V_S = 5\text{V}$, $f_S = 20\text{kHz}$, $R_L = 40\text{k}\Omega$, $C = 10\mu F$, $C_o = 120\mu F$, $L_1 = 78\mu\text{H}$, $L_2 = 1.25m\text{H}$, $n = 4$, MOS IRF840, and MOS photo-coupled driver 6N137. Next, based on these parameters, we can conduct the practical circuit test on this prototype to evaluate the steady-state performance for the different desired outputs. Fig. 9 shows the steady-state results of V_o for $V_{ref} = 200\text{V}, 180\text{V}$. It is obvious that this converter hardware is working in the stable status, and V_o is keeping on following V_{ref} firmly.

V. Conclusion

In this paper, the controller chip design/implementation is presented and aimed at the assisting the closed-loop control of MSCCI for the high-gain DC-DC conversion. As to the structure, this controller consists of PWM compensator, non-overlapping circuit, and phase generator. As to the function, this controller can perform the multiphase operation, which is a cyclical action of four steps and each step has two phases. As to the implementation, this controller chip is successfully designed via Cadence through pre/post-layout design, and then is assisted/fabricated by CIC and TSMC (chip no.: D35-105C-E0020, TSMC 0.35μm 2P4M, 1500×1500 μm^2, 5.0V, 0.528mW, max freq. 200kHz, 18S/B). Then, some examples of the MSCCI are discussed, and the simulation/experiment results are illustrated/verified on the prototype circuit to present the efficacy. Here, some advantages are summarized as follows. (i) As section 4 shows, just using few energy devices (three pumping capacitors and a coupled inductor) can reach the step-up gain of 42 (or higher). Indeed, it is an advantage of adopting multiphase operation here. (ii) This MSCCI essentially belongs to the sort of SC (excluding a coupled inductor). Thus, the related SC converter on chip will be promising. (iii) If required for a higher gain, it will be feasible not only to increase duty cycle/turn ratio of coupled inductor, but also to extend the stage number of SC booster in the MSCCI, as mentioned before. At present, we are working on conducting the function testing of this chip as well as merging this one into the prototype circuit in our laboratory. More experimental results will be obtained/measured for the verification of the overall converter design.

References

[1] J. K. Dickson, "On-chip high voltage generation in NMOS integrated circuits using an improved voltage multiplier technique, *IEEE J. Solid-State Circuits*, vol. 11, pp. 374–378, 1976.
[2] O. C. Mak, Y. C. Wong, A. Ioinovici, "Step-up DC power supply based on a switched-capacitor circuit," *IEEE Trans. on Industrial Electr.*, vol. 42, no. 1, pp. 90–97, 1995.

ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

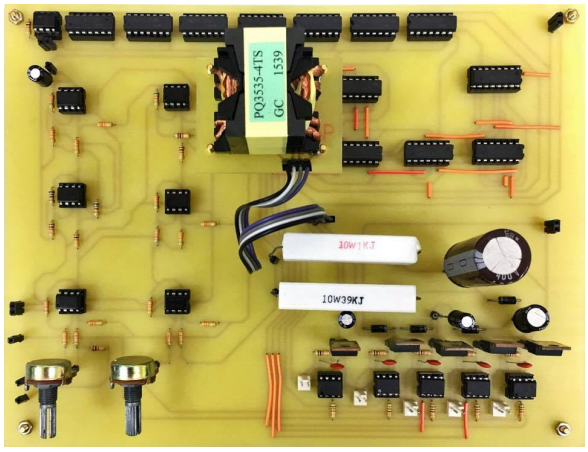
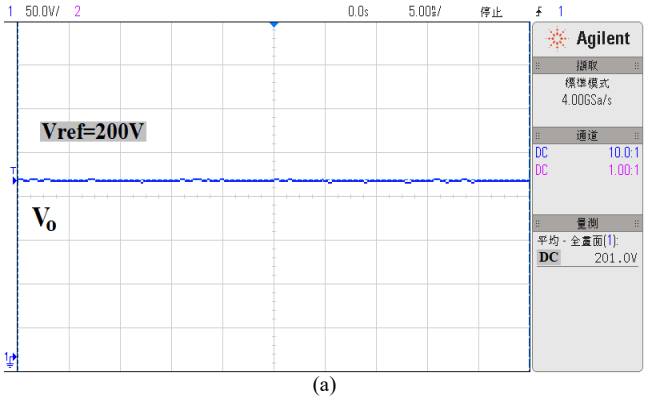
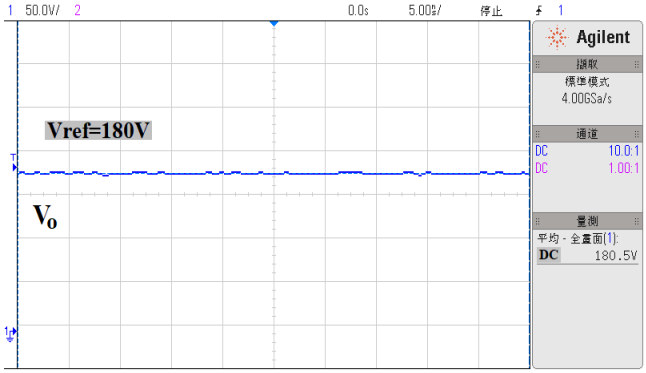


Fig. 8. Hardware implementation of MSCCI.



(a)



(b)

Fig. 9. Experiment results: V_o for (a) $V_{ref} = 200\text{V}$, (b) $V_{ref} = 180\text{V}$.

[3] G. Zhu, A. Ioinovici, "Steady-state characteristics of switched- capacitor electronic converters," *J. of Circuits, Systems and Computers*, vol. 7, no. 2, pp. 69–91, 1997.
[4] M. S. Makowski, "Realizability conditions and bounds on synthesis of switched-capacitor DC-DC voltage multiplier circuits. *IEEE Trans. on Circuits Syst. I, Fundamental Theory and Applications*, vol. 44, no. 8, pp. 684–691, 1997.
[5] J. A. Starzyk, Y.-W. Jan, F. Qiu, "A DC-DC charge pump design based on voltage doublers," *IEEE Trans. on Circuits Syst. I, Fundamental Theory and Applications*, vol. 48, no. 3, pp. 350–359, 2001.
[6] Y.-H. Chang, S.-Y. Kuo, "A gain/efficiency-improved serial-parallel switched-capacitor step-up DC-DC converter," *IEEE Trans. on Circuits Syst. I, Regular Papers*, vol. 60, no. 10, pp. 2799–2809, 2013.
[7] Y.-H. Chang, Y.-J. Chen, "A switch-utilization-improved switched-inductor switched-capacitor converter with adapting stage number," *Int. J. of Circuit Theory and Applications*, vol. 44, issue 3, pp. 709–728, 2016.
[8] Y.-H. Chang, Y.-K. Lin, "Design and analysis of high-gain switched-capacitor-inductor-based inverter for step-up DC-AC conversion," *J. of Circuits, Systems and Computers*, vol. 27, issue 2, pp. 1–23 (1850030), 2018.
[9] S.-M. Chen, M.-L. Lao, Y.-H. Hsieh, T.-J. Liang, and K.-H. Chen, "A novel switched-coupled-inductor DC-DC step-up converter and its derivatives," *IEEE Trans. on Industry Applications*, vol. 51, no.1, pp. 309–314, 2015.
[10] Y.-H. Chang, E.-P. Jhao, "A high-gain multiphase switched-capacitor coupled-inductor step-up DC-DC converter," *International MultiConference of Engineers and Computer Scientists 2017 (IMECS'2017)*, vol. 2, pp. 638–643, March 15-17, 2017.
[11] Y.-H. Chang, J.-S. Lin, "Design and analysis of switched-coupled-inductor SC step-up DC-DC converter," *Int. J. of Electronics (IJE)*, vol. 106, no. 11, pp. 1726–1745, 2019.

ISBN: 978-988-14049-1-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)