Design Considerations for a 20 GHz VCO Using a Cross-Coupled Differential Pair Topology

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***Abstract*—The design and analysis of fully integrated Voltage Controlled Oscillators (VCO) for 20 GHz low cost and low power communication system is presented in this paper. Our work is based mainly on the optimization of phase noise and buffer stage specifications. SiGeC hetero-junction bipolar transistors of f_T=200 GHz have been used and produced with a monolithic BiCMOS technology.**

***Index Terms*—Heterojuntion bipolar transistors, MMICs, phase noise, SiGe BiCMOS, voltage controlled oscillator (VCO).**

I. Introduction

It is well known that full integration in a standard process is a key point for the design of modern telecommunication systems. An important microwave function in transceiver is the millimeter wave generation. However, there is no generic method to design a low phase noise oscillator. Usually people use their home made "know how" and the low phase noise character is only achieved through some prototype that is difficult to reproduce for an industrial implementation. Moreover, oscillator features such as power consumption, output power, tuning range are very important and are optimized, too. It is then very important to research methods to develop a generic method that will permit to obtain a good accuracy of integrated circuit design.

In this paper, we present a full analysis and a design methodology of 20 GHz low phase noise VCO using a 200-GHz-F_{max} BiCMOS SiGeC technology [1]. Possible applications include the broad band optical fibre reception circuits with 20Gb/s and 40Gb/s or the broadband transmissions by satellites and radars in Ka band (20/30GHz).

II. HICUM Model

HICUM [2] (fig. 1) is an advanced model intended for high frequencies applications. The equivalent circuit of HICUM model considers all important physical effects for the current processes of bipolar technologies. The conception of high speed digital and analog circuits requires an exact description of the loads, the capacitances and also of transit time compared to polarization (I_C, V_{CE}).

The transfer current of a homo or hetero-junction vertical transistor can be described by a general form ICCR (Integral Control of Charges Relation):

$$i_T = \frac{c_{10}}{Q_{p,T}}\left[\exp\left(\frac{v_{B'E'}}{V_T}\right) - \exp\left(\frac{v_{B'C'}}{V_T}\right)\right] = i_{Tf} - i_{Tr} \qquad (1)$$

where the constant C_{10} is expressed as

$$c_{10} = (qA_E)^2 V_T \overline{\mu_{nB} n_{iB}^2} \qquad (2)$$

and where $V_{B'E'}$ and $V_{B'C'}$ are the tensions (depending on the time) in the transistor terminals if the flow of charge variation holes $Q_{p,T}$, is carried out between its transmitter and its collector. $\overline{\mu_{nB} n_{iB}^2}$ is the average value of the base area.

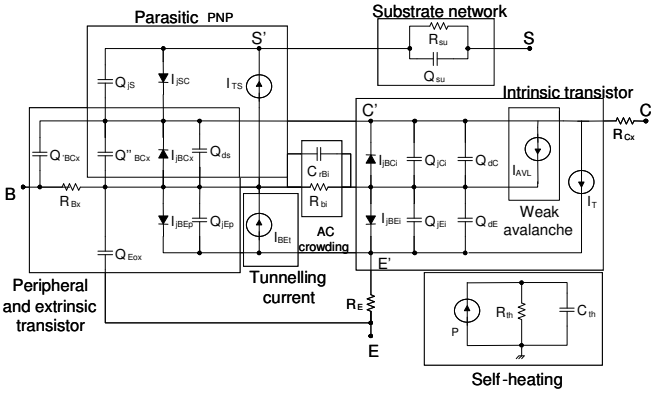


Fig. 1 Electric diagram of HICUM model

The depletion capacities values and the transit time of mobile carriers and of the associated charges, which determine the dynamic behavior, are considered basic quantities in the model. The depletion capacitance base emitter with forward bias consists of a classic part, an average and a strong bias component

$$C_{jEi} = \frac{C_{jEi0}}{\left(1 - v_j / V_{DEi}\right)^{z_{Ei}}} \cdot \frac{e}{1+e} + a_{jEi} C_{jEi0} \frac{1}{1+e} \qquad (3)$$

with

$$e = \exp\left(\frac{V_f - v_{B'E'}}{V_T}\right) \qquad (4)$$

and the auxiliary tension $v_j = V_f - V_T \ln\left[1 + e\right] < V_f$ (5)

where V_f is the voltage in which the capacitance of the classic expression (at strong forward bias) intercepts the maximum constant value. The base collector junction is normally polarized inversely. If the internal tension $v_{B'C}$' exceeds the rupture voltage, the epitaxial region of collector becomes completely exhausted. The depletion capacitance is constituted of three components:

$$C_{jCi} = C_{jCi,cl} + C_{jCi,PT} + C_{jCi,fb} \qquad (6)$$

where $C_{jCi,cl}$ represents the part due to average bias, $C_{jCi,fb}$ is the part due to maximum bias and $C_{jCi,PT}$ represents the strong bias component around and beyond rupture. In addition, all the basic model parameters as the capacitances and the transit time are easily measured with the standard equipment and methods of parameters extraction.

A. Parameter extraction

Reference [1] gives the DC and HF measurements of a HBT SiGeC with cut-off frequencies f_T and f_{max} higher than 200 GHz in 300 K and 65 K. By using Advanced Design System software (ADS), the parameters values of HICUM model are obtained for the transistor used in [1] with an emitter surface A_E = 0.17 µm x 6.2 µm. Fig. 2 shows the Gummel curves:

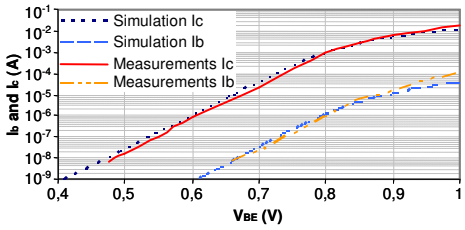


Fig. 2 Gummel curves

A good agreement is observed between simulated and measured data. Therefore, it is affirmed that the HICUM parameters values used in simulation correspond well to those of the hetero-junction bipolar transistor SiGeC to 200 GHz of [1]. Fig. 3 and 4 show f_T-I_C and f_{max}-I_C curves obtained at V_{CB} = 0.5V for the same device.

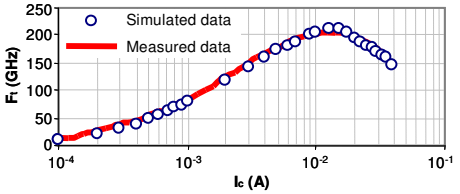


Fig. 3 Cut-off frequency f_T versus collector current I_C

To reiterate, this device exhibits cut-off frequencies f_T and f_{max} around 200 GHz. A very good agreement is observed between measured and simulated data where the best performance is reached for a collector current near 13 mA/µm².

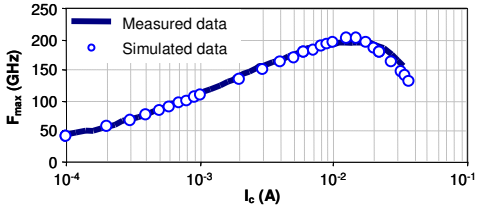
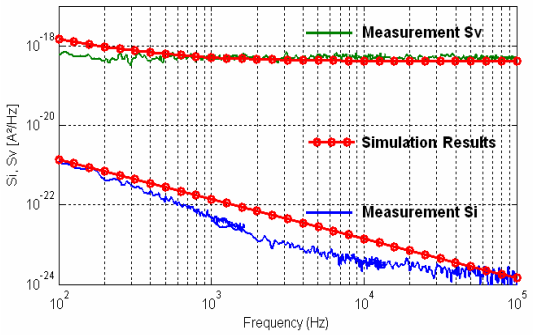
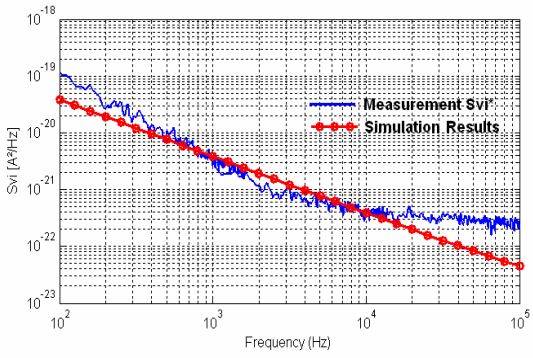


Fig. 4 Cut-off frequency f_{max}-versus collector current I_C

To design low phase noise microwave oscillator, an accurate low frequency noise model of active device is also a critical design issue. In a bipolar device the noise behaviour is fully described by the determination of both the tension and current fluctuations including their correlation [3]. Fig. 5 reports the spectra of S_V and S_I together with their cross-spectrum S_{VI^*} for bias points: I_B=1µA and I_C=1.3 mA.



a)



(b)

Fig. 5 (a) S_V and S_I spectra and (b) their cross-spectrum S_{VI^*}, simulated and measured. The spectra obtained with the HBT, respectively, biased at I_B=1µA, I_C=1.3mA. The HBT under test features an emitter area of 0.17 µm x 6.2 µm

The precision of HICUM is well verified in ADS software. We have used this reliable model of bipolar transistors, in the high performances VCO architectures design.

III. Design Considerations

The differential structure (fig. 6) using crossed transistors exhibits a positive feedback caused by a capacitive connection (C_1, C_2) crossed between the base and collector terminals of transistors in differential pair. These capacitive connections allow independent bias of the collector of T_2 (respectively T_1) of

the base of T_1 (respectively T_2), thus enabling the control of the voltage excursion on the base of transistors.

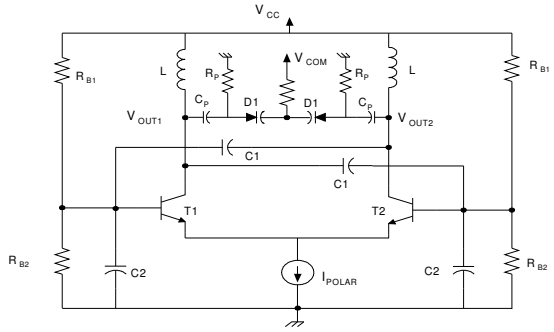


Fig. 6 VCO topology [4], [5]

The transistors in commutation associated with the positive feedback provide a negative resistance which compensates the resonator LC losses and thus the birth of an oscillating regime is caused [4]. The capacitances C_p are used to reduce non linearity's of varactors.

A stable oscillation demands that *Barkhausen criterion* is simultaneously satisfied. The oscillation frequency depends mainly on the values of "LC" components in the resonator, but also on the capacitive bridge C_1, C_2 and the parasites capacitances in the transistors.

A. Operating modes

The operating conditions of the transistors are determined by the feedback capacitances ratio n and the bias current I_{POLAR}.

with
$$n = \frac{C_1 + C_2}{C_1} = 1 + \frac{C_2}{C_1} \qquad (7)$$

Three operating modes *(dynamic modes)* can be distinguished: linear, nonlinear and very strongly nonlinear. The "slightly nonlinear" mode allows an optimization of the output voltage excursion and a relatively low level of harmonics. At fixed I_{POLAR}, the capacitances ratio n controls the transistors operating conditions of the differential pair. A weak capacitance relation increases the gain compression of transistors, and then supports the influence of their non-linearity, trans-conductance and capacitances (junction capacitance, transition capacitance and trans-capacitances). This operating mode also reduces the conduction time of transistors. Usually this last point is a key to reduce the phase noise, due to the cycle-stationary properties of noise sources associated with the collector current.

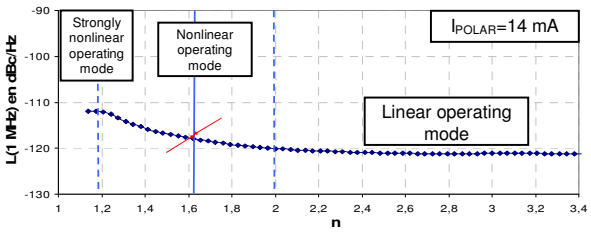


Fig. 7 Phase noise at 1 MHz (dBc/Hz) from the carrier versus capacitances ratio n (bias current Ipolar = 14 mA)

In fig. 7 we have plotted the phase noise at 1 MHz from the carrier versus capacitances ratio *n*.

An absolute nonlinear region can be observed for $1.2 < n < 2$. When n is larger than 1.2, we see an improvement of the phase noise to move away from non-linearities on the transistor, that deteriorate the phase noise. However, if n is too weak ($n < 1.6$), an increase of noise is noted. The phase noise then tends to increase while the conduction time of the transistors diminishes.

B. Results and optimisation

Firstly, a bad second harmonic rejection and an instability in the output power have been observed. The incorporation of a buffer improve the VCO output characteristics: a good isolation between the oscillator and the load (50Ω) to reduce the pulling factor in the circuit; a linear operation of the transistor on the buffer to control the output signal distortion; an input impedance that varies very weakly with the frequency which guarantees a constant level output power on the VCO tuning range and a better power consumption. To optimize VCO features, two configurations (emitter following and common emitter) have been studied and compared in detail [4]. The second harmonic rejection was not sufficient (about 19 dB) to satisfy the initial requirements (25 dB), a simple pass-band filter was placed in the buffer output. This filter increases the rejection of the second harmonic. At the same time it conserves the VCO initial performances. To prevent the degradation of the small fundamental output power variations a wide filter tuning range and a very effective second harmonic filtering are necessary. The common emitter configuration exhibits a greater power output (10 dBm) than the following emitters (7 dBm).

The output power is almost constant over the tuning voltage for both buffer configurations. A wide tuning range have been simulated, 2972 MHz and 2687 MHz for the following emitter and the common emitter respectively.

According to phase noise performance, very good levels have been noted for both buffers configurations, as shown in fig. 8.

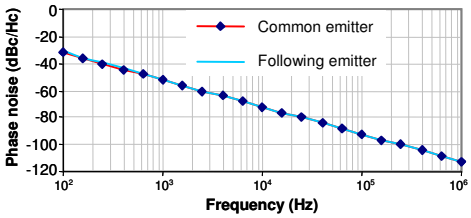


Fig. 8 Phase noise due to noise sources of cross-coupled transistors for the two buffers configurations

Pushing and pulling factors were also simulated in SPectreRF and ADS, by varying the supply voltage and the load resistance, respectively, and observing the change in oscillation frequency.

The layout of the LC-VCO cross-coupled differential pair (Fig. 5) occupies 305 µm x 405 µm of chip area and consumes 46 mW at 3.3V. Special attention was paid to making the layout of the differential circuits a symmetrical as possible. This is clearly visible in Fig. 5.

In addition, the inductors layout and their placement relative

to the core of the VCO were carefully evaluated. The distance between the inductors was also optimized using the concept of coupling inductance coefficient.

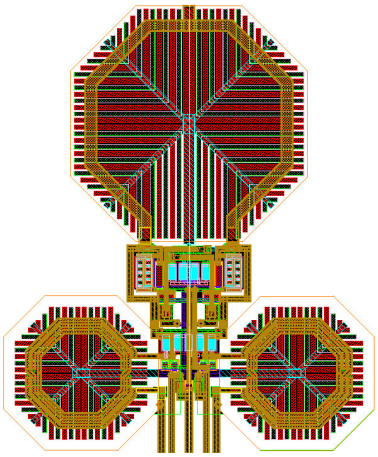


Fig. 9 20 GHz SiGe:C LC-VCO cross-coupled differential pair layout measuring 305 µm x 405 µm

Finally, both VCO exhibits very good performance (table 1) in terms of phase noise (-112 dBc/Hz at 1 MHz offset), power consumption (46 mW at 3.3V supply and without output buffer), output signal power (7.1 dBm and 10 dBm with respectively CC and CE buffer configurations) and second harmonic rejection (~27 dBm with filter).

TABLE I
SUMMARY OF VCO PRINCIPAL PERFORMANCES WITH THE TWO ANALIZED BUFFERS

	Following emitter (CC)	**Common emitter (CE)**
Oscillation frequency f_{osc} (GHz) at V_{tune}=1V	21.78	21.09
Tuning range (MHz) [V_{tune}=0-5V]	2.972	2.687
Phase noise at 1 MHz (dBc/Hz)	-112.41	-112.2
Supply voltage (V)	3.3	3.3
Output power (dBm)	7.1	10.0
Second harmonic rejection (dB)	26.1	27
Output impedance	50	50

The accuracy of the HICUM transistor model and the design methodology seems to be good but this work must be verify by measurements. We have already developed this design methodology in a 0.35 µm BiCMOS SiGe technology with good agreement between simulated and measured data [4]. A low frequency (LF) noise model using an original method based on the correlation resistance concept had been developed and associated with a non-linear non-quasi-static transistor model [6]. Comparative results related to the noise sources contributions for a 5 and 20 GHz VCO using a HBT emitter surface A_E = 3 x 0.4 µm x 60 µm and A_E = 0.17 µm x 6.2 µm respectively are presented in figure 10.

For both VCOs, the dominating LF noise is the differential pair noise (~ 80%). It is effectively generated by the transfer current noise and the internal base resistance noise for the 20 GHz VCO (~ 75%) of transistors T_1 and T_2. For the 5 GHz VCO, the principal LF noise source is the shot noise source S_{ICE}.

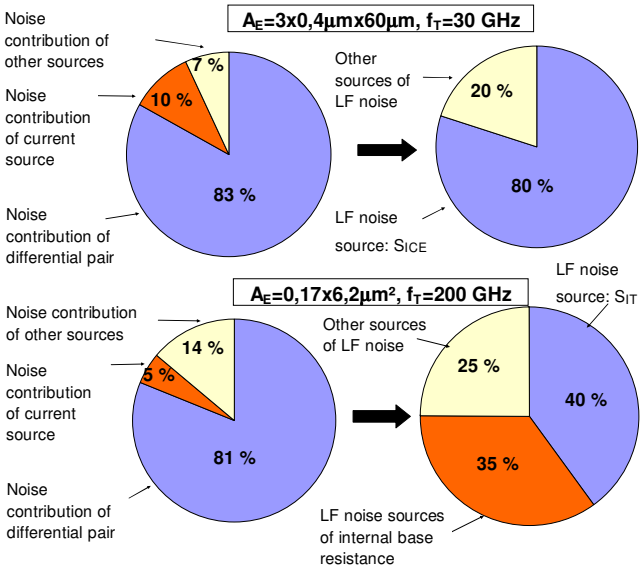


Fig. 10 Phase noise due to noise sources of cross-coupled transistors for the two buffers configurations

IV. CONCLUSION

A complete analysis and design considerations of 20 GHz low phase noise VCO using a 200-GHz-F_{max} BiCMOS SiGeC technology have been presented. To author's knowledge, a phase noise of -113 dBc/Hz at 1MHz offset associated to a tuning range upper than 2.6 GHz are the best obtained for a VCO designed in a monolithic SiGe bipolar technology.

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