Resource Efficient Design and Implementation of Standard and Truncated Multipliers using FPGAs

Muhammad H. Rais, *Member, IAENG,* Mohamed H. Al Mijalli, and Mohammad Nisar

Abstract—**We study the Field Programmable Gate Array (FPGA) implementation of fixed width standard and truncated multipliers using Very High speed integrated circuit Hardware Description Language and implemented on Spartan-3AN, Virtex and Virtex-E devices. We have achieved remarkable reduction in FPGA resources, power and delay when the full precision of standard multiplier is not required and the truncated multiplier can be implemented with fewer resources. The comparisons of different FPGA devices layout show that the standard multipliers utilize lot of space as compared to truncated multipliers which could be utilized for other embedded resources.**

Index Terms—**DSP, Spartan-3AN, Truncated Multiplier, Virtex, Virtex-E, VHDL.**

I. Introduction

MULTIPLICATION requires intensive and tedious scientific computations for signal processing (DSP) applications [1-3]. For the implementation of DSP algorithm demands using Application Specific Integrated Circuits (ASICs), which is especially required for image processing applications such as JPEG and MPEG etc. Due to high development costs for ASICs, algorithms should be verified and optimized before implementation [4].

The current development in very large scale integration (VLSI) technology, hardware implementation has become a desirable alternative. Field programmable gate arrays (FPGAs) have become known as a platform of choice for efficient hardware implementation of computation intensive algorithms [5]. FPGAs enable a high degree of parallelism and can achieve orders of magnitude speedup over general purpose processors (GPPs). This is entirely due to many embedded resources available and benefit of hardware speed and the flexibility of software in FPGA. This makes FPGA a viable technology and an attractive alternative to ASICs [5-6].

DSP, image processing and multimedia applications extensively requires multiplication and squaring functions [7-8]. A full width digital n×n multiplier computes the 2n output as a weighted sum of partial products [9]. If the product is truncated to n-bits, the least-significant columns of the product matrix contribute little to the final result. To take advantage of this, truncated multipliers and squarers do not form all of the least-significant columns in the partial-product matrix [10]. As more columns are eliminated, the area and power consumption of the arithmetic unit are significantly reduced, and in many cases the delay also decreases. The trade-off is that truncating the multiplier matrix introduces additional error into the computation.

Cryptography requires not only a significant number of multiplication and squaring functions but also large integers [11-12]. Many research efforts have been presented in literature to achieve hardware efficient implementation of a truncated multiplier. The basic idea of these techniques is to discard some of the less significant partial products and to introduce a compensation circuit that partly compensates for the dropped terms, thereby reducing approximation error [13-18]. In reference [19] presented a truncated multiplier with minimum square error for every inputs' bit width. By parallel processing and pipelining a high speed multiplication can be achieved for DSP applications, this could be made more efficient by introducing truncated multiplication. Rais has presented a study on standard and truncated multipliers using FPGA devices [20-22]. Babic et al. [23] recently published a new approach to improve the accuracy and efficiency of Mitchell's algorithm based multiplication.

The rest of this paper is structured as follows. In section II, describes the mathematical basis of truncated multiplication. Section III addresses the architectural platform used in this study. Section IV presents the FPGA design and implementation results. Finally, section V presents the conclusion.

II. Mathematical Basis of Truncated Multipliers

Considering the multiplication of two n-bit inputs X and Y, a standard multiplier performs the following operations to obtain the 2n bit product P

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$$P = XY = \sum_{i=0}^{2n-1} P_i 2^i = (\sum_{i=0}^{n-1} x_i 2^i)(\sum_{i=0}^{n-1} y_i 2^i) \quad (1)$$

where x_i, y_i and P_i represent the i^{th} bit of X, Y and P, respectively.

Fig. 1 shows the standard architecture of 6×6-bit parallel multiplier, where HA and FA are the half and full adders respectively. Equation (1) can be expressed by the sum of two segments: the most-significant part *MP* and the least-significant part *LP*

$$P = MP + LP = \sum_{i=0}^{2n-1} P_i 2^i + \sum_{i=0}^{n-1} P_i 2^i \quad (2)$$

The standard 6×6-bit parallel multiplier can also be divided into three subsets: the most-significant part *MP*, input correction *IC* and the least-significant part *LP*. Equation (2) can be rewritten as follows:

$$P = MP + IC + LP \quad (3)$$

The fixed width multiplier can be obtained directly by removing the *LP* region and introducing the *IC* region to obtain MP' region, which is truncated multiplier as shown in Fig. 2 and given by equation (4).

$$P = MP' + IC \quad (4)$$

III. Architecture Platform

Due to the parallel nature, high frequency, and high density of modern FPGAs, they make an ideal platform for the implementation of computationally intensive and massively parallel architecture. In this section a brief introduction about state-of-the-art FPGAs from Xilinx is presented.

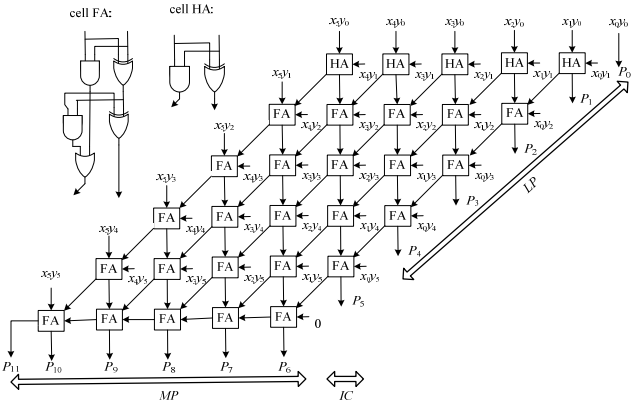

Fig. 1. The architecture of a standard 6×6-bit parallel multiplier

A. Spartan-3 FPGAs

The Spartan-3 FPGA belongs to the fifth generation Xilinx family. It is specifically designed to meet the needs of high volume, low unit cost electronic systems. The family consists of eight member offering densities ranging from 50,000 to five million system gates [24]. The Spartan-3 FPGA consists of five fundamental programmable functional elements: CLBs, IOBs, Block RAMs, dedicated multipliers (18×18) and digital clock managers (DCMs), Spartan-3 family includes Spartan-3L, Spartan-3E, Spartan-3A,

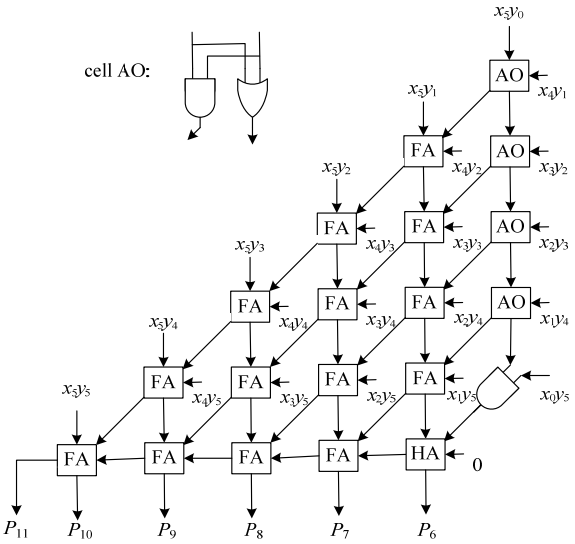

Fig. 2. The architecture of a truncated 6×6-bit parallel multiplier

Spartan-3A DSP, Spartan-3AN and the extended Spartan-3A FPGAs. Particularly, the Spartan-3AN is used as a target technology in this paper. Spartan-3AN combines all the feature of Spartan-3A FPGA family plus leading technology in-system flash memory for configuration and nonvolatile data storage.

B. Virtex FPGAs

Virtex devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The Virtex family comprises of nine members offering densities ranging from 57,906 to 1,124,022 system gates [25]. The abundance of routing resources permits the Virtex family to accommodate even the largest and most complex designs. Virtex FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. In some modes, the FPGA reads its own configuration data from an external PROM (master serial mode). Virtex devices provide better performance than previous generations of FPGA. Designs can achieve synchronous system clock rates up to 200 MHz including I/O.

C. Virtex-E FPGAs

The Virtex-E FPGA family delivers high-performance high-capacity programmable logic solutions. The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

The Virtex-E family delivers a high-speed and high-capacity programmable logic solution. The Virtex-E family comprises the eleven members offering densities ranging from 71,693 to 4,074,387 system gates [26].

Virtex-E devices have up to 640 Kb of faster (250 MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight

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DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication. The Virtex-E devices built aggressive 6-layer metal 0.18 µm CMOS process.

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. Virtex-E FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. Virtex-E devices provide better performance than previous generations of FPGAs. Designs can achieve synchronous system clock rates up to 240 MHz including I/O or 622 Mb/s using Source Synchronous data transmission architectures.

IV. FPGA Design and Implementation Results

The design of standard and truncated 4×4, 6×6, 8×8, and 12×12-bit multipliers are done using VHDL and implemented in a Xilinx Spartan-3AN XC3S700AN (package: fgg484, speed grade: -5), Virtex XCV50 (package: fg256, speed grade: -6) and Virtex-E XCV50E (package: fg256, speed grade: -8) FPGA using the Xilinx ISE 9.2i design tool [27].

FPGA layouts of the standard 4×4, 6×6, 8×8, and 12×12-bit multipliers are shown in Figs. 3, 4, 5 and 6. FPGA layouts of truncated 4×4, 6×6, 8×8, and 12×12-bit multipliers are further shown in Figs. 7, 8, 9 and 10.

The FPGA layouts shown in Figs. 3, 4, 5, 6, 7, 8, 9 and 10 of standard and truncated 4×4, 6×6, 8×8, and 12×12-bit multipliers also show less utilization of FPGA area for truncated multiplier, which is an indication of best utilization of the FPGA resources.

Tables 1, 2 and 3 summarize the FPGA device resources utilization for standard and truncated 4×4, 6×6, 8×8, and 12×12-bit multipliers. Table 4 presents the percentage change between the standard to truncated 4×4, 6×6, 8×8, and 12×12-bit multipliers, which clearly demonstrates that the occupied slices ranges from 145% to 170% for Spartan-3AN, Virtex and Virtex-E FPGA devices. The reduction in pin delay and the number of occupied slices used in truncated multiplier also show that it is one of the viable solutions for image processing applications, where most of the redundant information can be removed.

V. Conclusion

In this paper we have presented hardware design and implementation of FPGA based parallel architecture for standard and truncated multipliers utilizing VHDL. The design was implemented on Xilinx Spartan-3AN XC3S700AN, Virtex XCV50 and Virtex-E XCV50E FPGA devices using the ISE 9.2i design tool. The objective is to present a comparative study of the 4×4, 6×6, 8×8, and 12×12-bit standard and truncated multipliers using FPGA devices. The comparison between standard and truncated multiplier show much more reduction in device utilization. The FPGA devices used almost same number of occupied slices but their average connection and maximum pin delays are different; which clearly indicates that the Spartan-3AN is better FPGA device than other Virtex and Virtex-E FPGAs. The comparison of FPGA layouts of standard and truncated multipliers also demonstrates that the less area is utilized for the resources and the remaining could be utilized for other embedded resources.

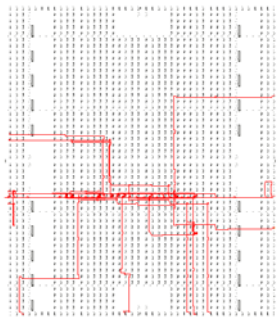

Fig. 3. FPGA layout of standard 4×4-bit multiplier

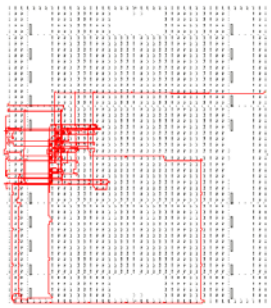

Fig. 4. FPGA layout of standard 6×6-bit multiplier

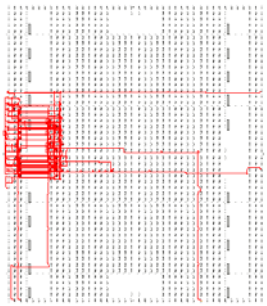

Fig. 5. FPGA layout of standard 8×8-bit multiplier

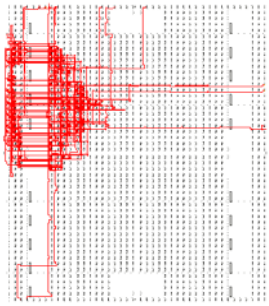

Fig. 6. FPGA layout of standard 12×12-bit multiplier

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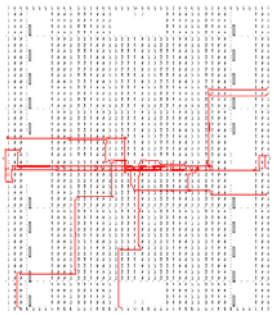

Fig. 7. FPGA layout of truncated 4×4-bit multiplier

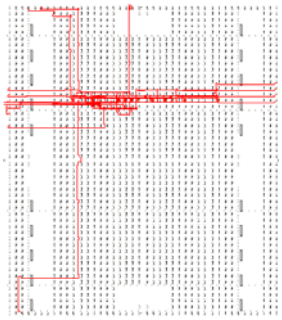

Fig. 8. FPGA layout of truncated 6×6-bit multiplier

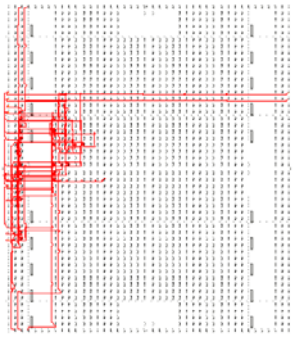

Fig. 9. FPGA layout of truncated 8×8-bit multiplier

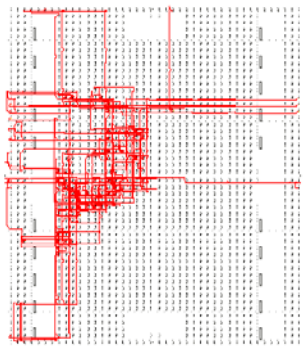

Fig. 10. FPGA layout of truncated 12×12-bit multiplier

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TABLE I
FPGA RESOURCE UTILIZATION FOR STANDARD AND TRUNCATED MULTIPLIER FOR SPARTAN-3AN XC3S700AN (PACKAGE:FGG484, SPEED GRADE:-5)

Bit Width	Multipliers	Four Input LUTs (11776)	Occupied Slices (5888)	Bonded IOBs (372)	Total Equivalent Gate Count	Average Connection delay (ns)	Maximum Pin delay (ns)
4×4	Standard	30	16	16	180	1.421	3.598
	Truncated	18	11	12	111	1.272	2.705
6×6	Standard	67	36	24	402	1.238	4.873
	Truncated	43	24	18	261	1.096	2.722
8×8	Standard	121	62	32	726	1.085	3.968
	Truncated	76	40	24	456	1.072	3.641
12×12	Standard	289	148	48	1734	1.079	3.766
	Truncated	164	87	36	984	1.307	3.971

TABLE II
FPGA RESOURCE UTILIZATION FOR STANDARD AND TRUNCATED MULTIPLIER FOR VIRTEX XCV50 (PACKAGE:FG256, SPEED GRADE:-6)

Bit Width	Multipliers	Four Input LUTs (11776)	Occupied Slices (5888)	Bonded IOBs (372)	Total Equivalent Gate Count	Average Connection delay (ns)	Maximum Pin delay (ns)
4×4	Standard	30	16	16	180	1.343	2.449
	Truncated	18	11	12	111	1.389	3.132
6×6	Standard	67	36	24	402	1.469	3.933
	Truncated	43	24	18	261	1.251	2.759
8×8	Standard	121	62	32	726	1.437	4.254
	Truncated	76	40	24	456	1.466	4.596
12×12	Standard	289	148	48	1734	1.628	4.830
	Truncated	164	87	36	984	1.478	3.460

TABLE III
FPGA RESOURCE UTILIZATION FOR STANDARD AND TRUNCATED MULTIPLIER FOR VIRTEX-E XCV50E (PACKAGE:FG256, SPEED GRADE:-8)

Bit Width	Multipliers	Four Input LUTs (11776)	Occupied Slices (5888)	Bonded IOBs (372)	Total Equivalent Gate Count	Average Connection delay (ns)	Maximum Pin delay (ns)
4×4	Standard	30	16	16	180	1.193	2.141
	Truncated	18	11	12	111	1.009	2.113
6×6	Standard	67	36	24	402	1.264	4.449
	Truncated	43	24	18	261	1.004	2.196
8×8	Standard	121	62	32	726	1.148	2.775
	Truncated	76	40	24	456	1.308	3.437
12×12	Standard	289	148	48	1734	1.358	4.361
	Truncated	164	87	36	984	1.267	3.644

TABLE IV
PERCENTAGE CHANGE BETWEEN THE STANDARD AND TRUNCATED MULTIPLIER FOR SPARTAN-3AN, VIRTEX AND VIRTEX-E FPGA DEVICES

BIT WIDTH (MULTIPLIERS)	Four Input LUTs (11776)	Occupied Slices (5888)	Total Equivalent Gate Count
4×4 (Standard/Truncated)	166.7%	145.4%	162.2%
6×6 (Standard/Truncated)	155.8%	150%	154%
8×8(Standard/Truncated)	159.2%	155%	159.2%
12×12(Standard/Truncate)	176.2%	170.1%	176.2%

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