A RF Low Power 0.18-µm based CMOS Differential Ring Oscillator

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Abstract—A voltage controlled ring oscillator is implemented using the 1P6M 0.18µm CMOS process provided by TSMC with 1.8 volts power supply. Differential delay cell stages are used to reduce noise. The output frequency range is 3.125-5.26 GHz with control voltages range 1 V to 1.8 V. The simulated result of the circuit draws 0.621 mW of power from the 1.8 V supply.

Keywords— CMOS, low power, phase noised, differential delay cell, voltage controlled oscillator (VCO).

I. INTRODUCTION

The VCO is the key component that controls the frequency of the PLL. A good VCO should have low phase noise low DC power and high frequency swing. There are mainly two types of VCOs, ring oscillator and LC tank. LC oscillators have low phase noise but low frequency swing. They are used in wireless communication applications. On the other hand ring oscillators have wide range of frequency swing and are easy to implement. Ring oscillators also occupy less chip area as they do not have inductor as compared to LC tank oscillators but they are more prone to noise. The main objective is to design a ring oscillator whose noise performance is comparable to LC oscillators.

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A three stage ring oscillator is designed using 1P6M 0.18µm CMOS technology provided by TSMC. The circuit achieves RF frequency range with very good noise performance comparable to LC oscillators. The first delay cell is a differential CMOS NAND gate and the other two delay cells are differential CMOS inverters. The inputs of the first delay cell are control voltage and the output feedback.

The output frequency varies from 3.125 GHz to 5.26 GHz at V_{ctrl} = 1 V and V_{ctrl} = 1.8 V respectively. The objective is to achieve good noise performance comparable to LC oscillators and low DC power consumption with RF frequency range. V_{ctrl} is control or tuning voltage.

II. PROPOSED RING OSCILLATOR

A. Differential Delay Cell

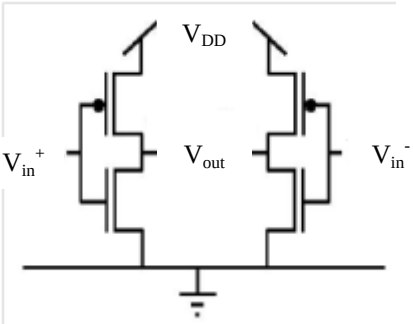

Fig.1 basic differential delay cell

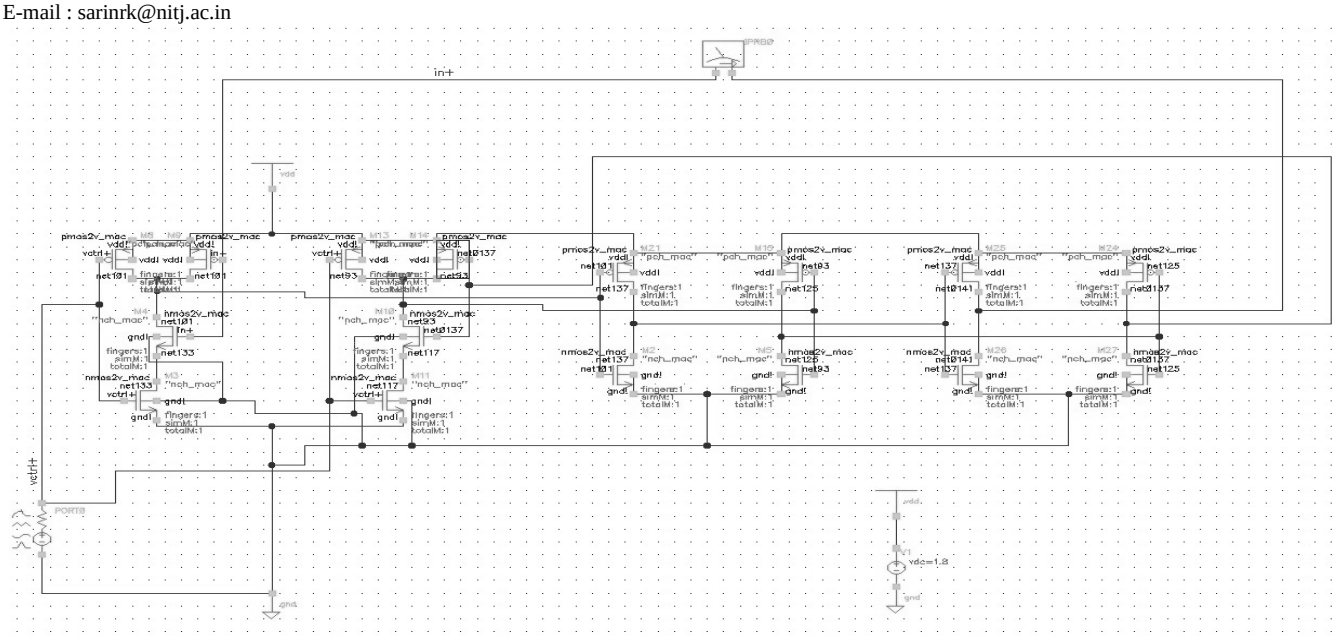

Fig.2 Proposed 3 stage differential delay cell

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A basic differential delay cell is shown in fig. 1[1]. Differential delay cell rejects the common mode and power supply noise. Therefore to improve the noise performance of ring oscillator, differential delay cell is used.

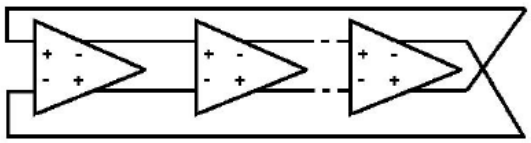

Fig.3 Basic Differential ring oscillator

A basic differential ring oscillator block diagram is shown in fig.3 [1]. The differential ring oscillator has two differential inputs as compared to one in case of basic ring oscillators. If the output is not stable a last differential buffer stage can be added to odd number of delay stages which will make number of stages even.

In this paper a three stage differential voltage controlled is designed. No last differential buffer stage is used. Power consumption will increase with number of components or transistors, thus least three stages are used.

B. Ring oscillator Circuit and Design

The schematic of the proposed ring oscillator is shown in figure 2. The first delay cell is differential CMOS Nand gate and the other two are differential CMOS inverters. The first delay cell Nand gate will act as an inverter if both of its inputs are same; this completes the three inverter stages. Each inverter has a certain delay between stages; this delay is termed as 'inverter pair delay'. It is the sum of the rise and fall time of an individual inverter.

For N stage ring oscillator the oscillation frequency is given by as:

$$F_{osc} = \frac{1}{N\,(\tau_{rise} + \tau_{fall})} \qquad (1)$$

Where τ_{rise} and τ_{fall} are the rise and fall time of a individual delay cell or stage. For a good VCO rise time and fall time should be equal. Thus taking $\tau_{rise} = \tau_{fall} = \tau$. As a three stage ring oscillator is presented in this paper so by taking the value N=3, the frequency of oscillation is given as:

For the inverter shown in fig.4, the (W/L) ratios of the transistors (nMOS and pMOS) are given as [2]:

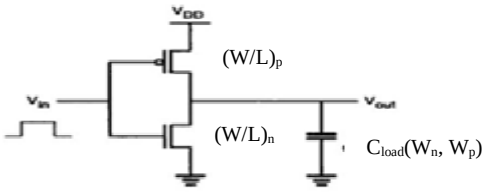

Fig.4 CMOS Inverter [2]

$$\left(\frac{W}{L}\right)_n = \frac{C_{load}}{\tau_{fall}\,\mu_n\,C_{ox}(V_{DD}-V_{t,n})}\left[\frac{2\,V_{t,n}}{V_{DD}-V_{t,n}} + \ln\left(\frac{4(V_{DD}-V_{t,n})}{V_{DD}} - 1\right)\right] \qquad (3)$$

$$\left(\frac{W}{L}\right)_p = \frac{C_{load}}{\tau_{rise}\,\mu_p\,C_{ox}(V_{DD}-|V_{t,p}|)}\left[\frac{2\,|V_{t,p}|}{V_{DD}-|V_{t,p}|} + \ln\left(\frac{4(V_{DD}-|V_{t,p}|)}{V_{DD}} - 1\right)\right] \qquad (4)$$

Where C_{load} is the output load capacitance and C_{ox} is the gate oxide capacitance per unit area. Again taking $\tau_{rise} = \tau_{fall} = \tau$, eq. 3 and 4 will be as:

$$\left(\frac{W}{L}\right)_n = \frac{C_{load}}{\tau\,\mu_n\,C_{ox}(V_{DD}-V_{t,n})}\left[\frac{2\,V_{t,n}}{V_{DD}-V_{t,n}} + \ln\left(\frac{4(V_{DD}-V_{t,n})}{V_{DD}} - 1\right)\right] \qquad (5)$$

$$\left(\frac{W}{L}\right)_p = \frac{C_{load}}{\tau\,\mu_p\,C_{ox}(V_{DD}-|V_{t,p}|)}\left[\frac{2\,|V_{t,p}|}{V_{DD}-|V_{t,p}|} + \ln\left(\frac{4(V_{DD}-|V_{t,p}|)}{V_{DD}} - 1\right)\right] \qquad (6)$$

Clearly as $\mu_p < \mu_n$, the $(W/L)_p$ will be greater than $(W/L)_n$.

C. Power Analysis

The static power consumption of the CMOS inverter is quite negligible. During switching events where the output load capacitance alternatively charged and discharged, the CMOS inverter consumes power [2].

Considering fig.5 and assuming that the input is an ideal voltage waveform with negligible rise and fall time.

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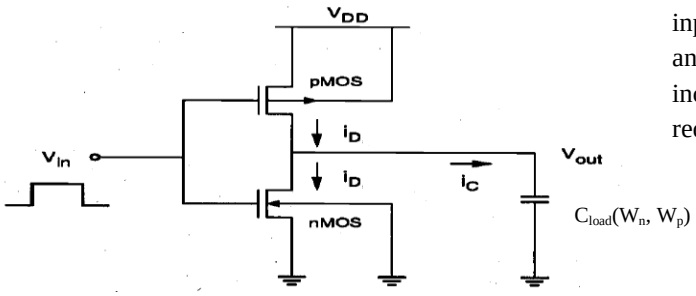

Fig.5 CMOS inverter for power analysis [2]

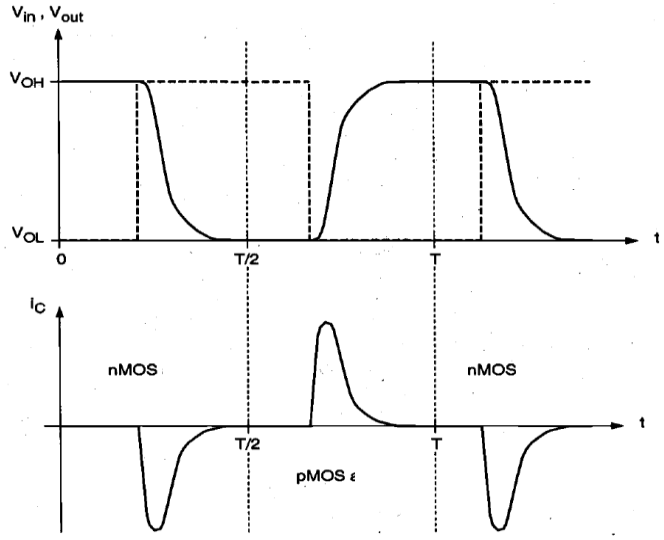

Fig.6 Input and output voltage and capacitor current waveform [2]

From fig.5, 6 and assuming periodic input and output the average power consumed over one period is given as:

$$P_{avg} = \frac{1}{T}\int_0^T v(t)\,.\,i(t)\,dt \qquad (7)$$

The pMOS and nMOS conduct current for half period each thus:

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} V_{out}\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \int_{T/2}^{T}(V_{DD}-V_{out})\left(C_{load}\frac{dV_{out}}{dt}\right)dt\right]$$

Evaluating the integrals we get:

$$P_{avg} = \frac{1}{T}C_{load}{V_{DD}}^2 \qquad (8)$$

As $F_{osc} = 1/T$

$$P_{avg} = C_{load}\,.\,{V_{DD}}^2\,.\,F_{osc} \qquad (9)$$

If the total parasitic capacitance in the circuit can be lumped at the output node with reasonable accuracy and the output voltage swing is between 0 and V_{DD} assuming the input is ideal, the power expression given by (9) is valid for any CMOS circuit when the leakage power is neglected. To increase frequency the parasitic capacitance value has to be reduced.

I. SIMULATION RESULT AND PERFORMANCE COMPARISION

The schematic shown in figure 2 is designed and optimized using Cadence Virtuoso using 0.18µm 1P6M CMOS technology provided by TSMC and the output responses are plotted using Cadence Spectre.

Fig.7 shows the transient response at V_{ctrl} = 1 V with oscillation frequency F_{osc} = 3.125 GHz. Similarly Fig.8 shows the transient response at V_{ctrl} = 1.8 V with oscillation frequency F_{osc} = 5.26 GHz

Fig.9 shows the transient power response at V_{ctrl} = 1 V Similarly Fig.10 shows the transient power response at V_{ctrl} = 1.8 V.

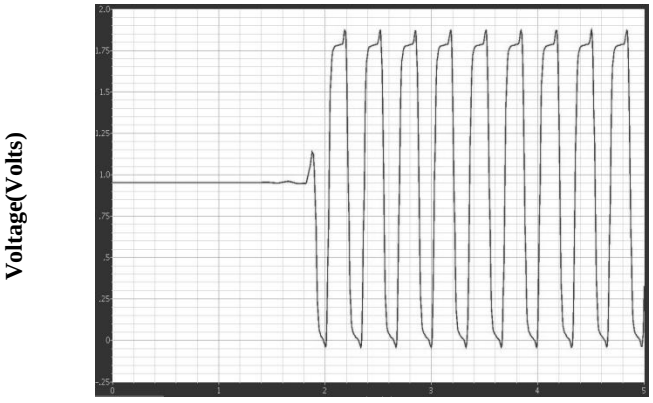

Fig.7 Transient response V_{ctrl} = 1 V, F_{osc} = 3.125 GHz

Fig.8 Transient response V_{ctrl} = 1.8 V, F_{osc} = 5.26 GHz

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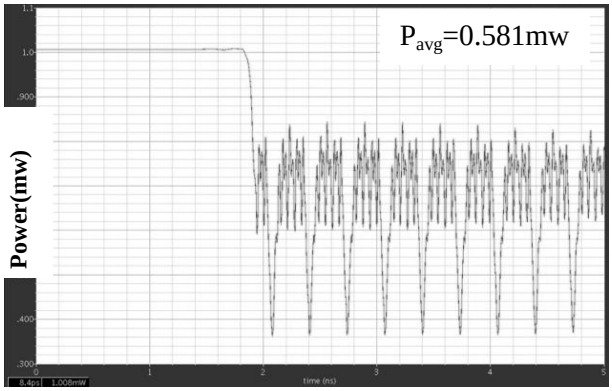

Fig.9 Transient power at V_{ctrl} = 1V

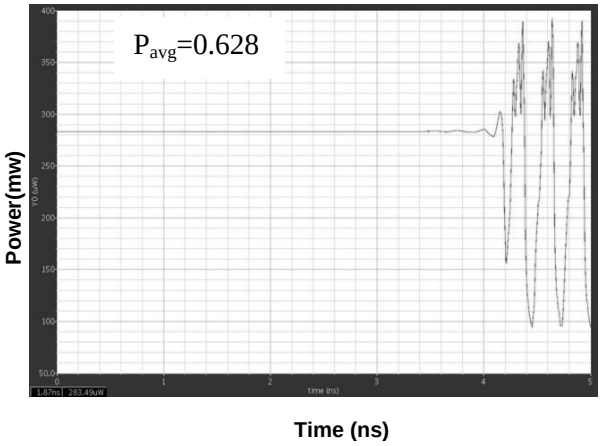

Fig.10 Transient power at V_{ctrl} = 1.8V

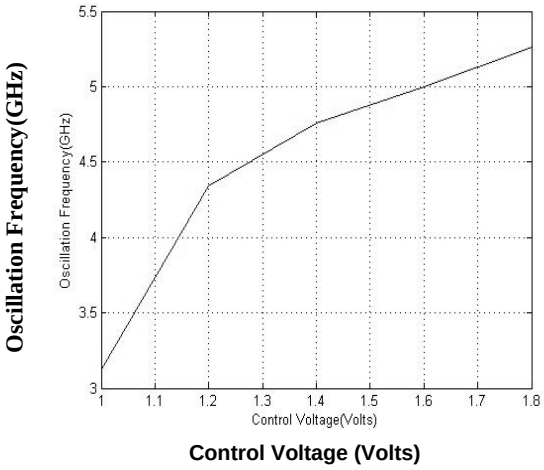

Fig.11 Frequency vs control voltage graph is shown

Table I Performance Comparison

Reference	Process Technology(µm)	Type	Tuning Range (GHz)	Power (mW)	Supply Voltage (Volts)
[6]	0.18 CMOS	Vackar VCO	4.85-4.93	13.5	1.8
[7]	0.18 CMOS	Armstrong VCO	4.96-5.34	3.9	1.8
[8]	0.18 CMOS	Colpitts VCO	4.9-5.46	6.4	1.8
[9]	0.18 CMOS	Hartley VCO	4.02-4.5	6.75	1.8
[10]	0.25 CMOS	LC	4.55-5.45	13.7	1.8
[11]	0.18 CMOS	Ring	5.16-5.93	27	1.8
This Work	0.18 CMOS	Ring	3.125-5.26	0.621	1.8

0.18µm 1P6M CMOS technology provided by TSMC which consumes a very low DC power, P_{avg} = 0.621 mW within the frequency range 3.125 to 5.26 GHz.

IV. LAYOUT CONSIDERATION

Layout of the proposed ring oscillator is shown in fig.12 showing that there is no DRC error. Fig.13 shows no Layout Vs Schematic error means schematic and layout match. Fig. 14 shows the parasitic extracted layout.

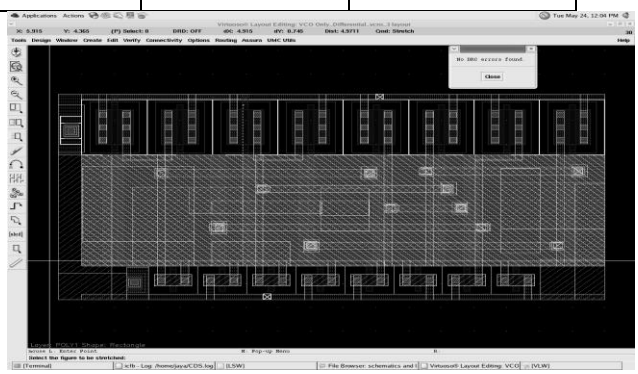

Fig12 Layout of proposed ring oscillator showing no DRC error

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V. CONCLUSIONS

Performance comparison is given in table 1, where it is shown that the frequency range maximum (B.W = 2.135 GHz) power Consumption = 0.621 mw least in this work. So this proposed ring oscillator is used for wide range RF low power application.

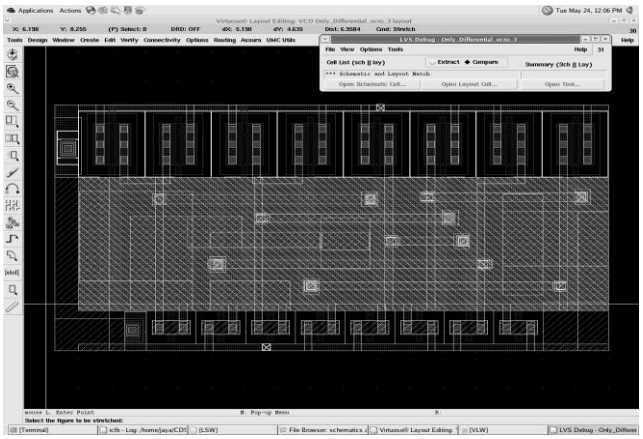

Fig13 Layout of proposed ring oscillator showing no LVS error

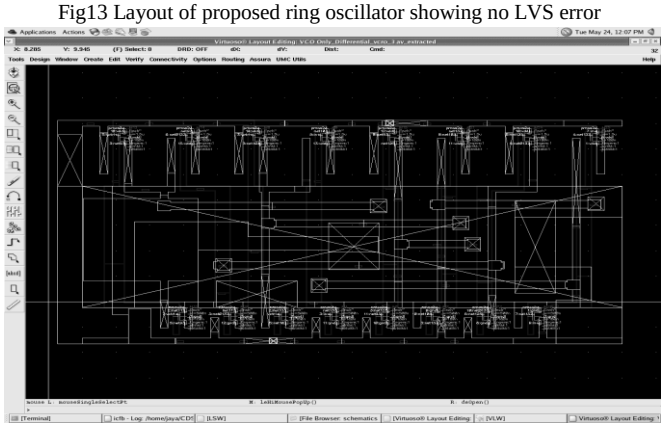

Fig14 Extracted layout of proposed ring oscillator

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