The Experimental Studies of Transient Free Digital SVC Controller with Thyristor Binary Compensator at 125 KVA Distribution Transformer

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Abstract— Electrical distribution systems are incurring large losses as the loads are wide spread, inadequate reactive power compensation facilities and their improper control. A comprehensive static VAR compensator consisting of capacitor bank in five binary sequential steps in conjunction with a thyristor controlled reactor of smallest step size is employed in the investigative work. The work deals with the performance evaluation through analytical studies and practical implementation on an existing system. A fast acting error adaptive controller is developed suitable both for contactor and thyristor switched capacitors. The switching operations achieved are transient free, practically no need to provide inrush current limiting reactors, TCR size minimum providing small percentages of nontriplen harmonics, facilitates stepless variation of reactive power depending on load requirement so as maintain power factor near unity always. It is elegant, closed loop microcontroller system having the features of self regulation in adaptive mode for automatic adjustment. It is successfully tested on a distribution transformer of three phase 50 Hz, Dy11, 11KV/440V, 125 KVA capacity and the functional feasibility and technical soundness are established. The controller developed is new, adaptable to both LT & HT systems and practically established to be giving reliable performance.

Keywords— Binary Sequential switched capacitor bank, TCR, Nontriplen harmonics, step less Q control, transient free.

I. Introduction

It is well documented in literature and through public discussions at various levels that a substantial power loss is taking place in our low voltage distribution systems on account of poor power factor, due to inadequate reactive power compensation facilities and their improper control.

The expansion of rural power distribution systems with new connections and catering to agricultural sector in wide spread remote areas, giving rise to more inductive loads resulting in very low power factors. Thus there exists a great necessity to closely match reactive power with the load so as to improve power factor, boost the voltage and reduce the losses.

In this paper, a more reliable, technically sound, fast acting and low cost scheme is presented by arranging the thyristor switched capacitor units in five binary sequential steps. This enables the reactive power variation with the least possible resolution. In addition a thyristor controlled reactor of the lowest step size is operated is conjunction with capacitor bank, so as to achieve continuously variable reactive power. Besides the enhancement transformer loading capability the shunt capacitor also improves the feeder performance, reduces voltage drop in the feeder & transformer, better voltage at load end, improves power factor, improves system security with enhanced utilization of transformer capacity, gives scope for additional loading, increases over all efficiency, saves energy due to reduced system losses, avoids low power factor penalty, and reduces maximum demand charges.

A. SVC With Binary Sequential Switched Capacitors

The SVC is indispensable and based on proven technology for power factor correction and reactive power compensation. Traditionally SVC has been used as a shunt device that offers voltage stability and reactive power compensation to the load or at PCC. Since EPRI's (Electric Power Research Institute) release of FACTS strategies in 1987 SVC's have grown in popularity and are well established in power industry [1]-[3].

The Basin Electric Power Corporation installed the first SVC in Nebraska in 1977 [4],[5]. The simplest configuration for an advanced shunt compensator essentially consists of the thyristor switched capacitor bank with each capacitor step connected to the system through a thyristor switch. In the proposed paper capacitor bank step values are chosen in binary sequence weights to make the resolution small. An analysis of switching transients indicates that transient free switching can occur if the following two conditions are met [6],[7].

a) The thyristor is fired at the negative/positive peak of voltage, and/or
b) Capacitor is precharged to the negative/positive peak voltage.

The first condition can be met accurately by timing the control circuitry and the second condition is only met immediately after switching off thyristor. The configuration for five capacitor bank steps in binary sequence weight with thyristors switch is shown in Fig. 1

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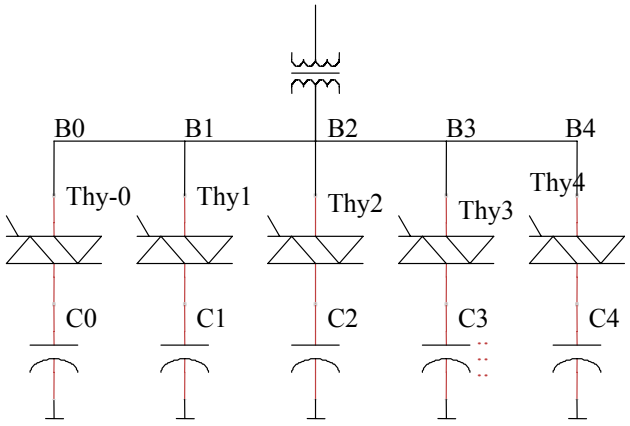

Fig. 1. Thyristor Binary Compensation Scheme (TBC).

B. FC-TCR Scheme

The Fig. 2 shows the basic configuration of static compensator FC-TCR. In this case capacitor represents a thyristor switched capacitor bank in binary sequential steps (TBC) as explained earlier and **L** represents reactor with phase angle control [8]-[10].

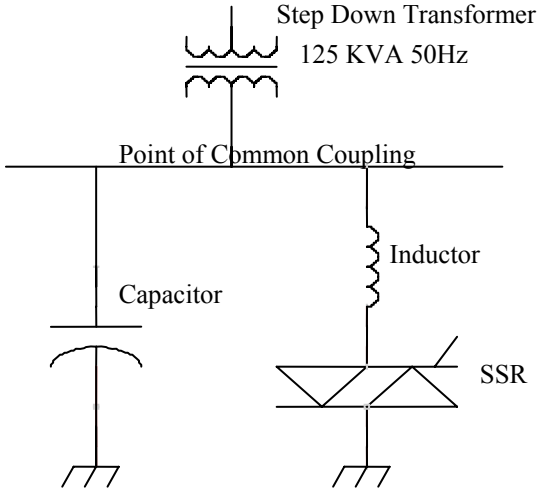

Fig. 2. FC-TCR Scheme

The controllable range of TCR firing angle α extends from 90^0 to 180^0. In case of ideal reactor of **L** Henry firing angle of 90^0 results in full conduction with continuous sinusoidal current flow. Practically all six air cored reactors are designed with an average resistance of 10 Ω and inductance of 230 mH.

The following "(1)" [6] illustrates the relation between firing angle α and the current through inductor I_L for ideal inductor having resistance tending towards zero while "(2)" represents the practical case considering resistance R Ω.

$$I_L = \left(\frac{V}{\omega L}\right)\left(1 - \left(\frac{2}{\pi}\right)\alpha - \left(\frac{1}{\pi}\right)\sin 2\alpha\right) \quad (1)$$

$$I_L(\alpha) = \frac{V_m}{\sqrt{R^2 + X_L^2}}\left[\frac{1}{2\pi}\left\{(\beta - \alpha) + \frac{\sin 2\alpha}{2} - \frac{\sin 2\beta}{2}\right\}\right]^{0.5} \quad (2)$$

The following observations are important.

i) If α = θ i. e. firing angle = phase angle
sin(β - θ) = sin(β - α) = 0
and conduction angle = β - α = π

ii) Conduction angle should not exceed π
The range of control angle α is θ ≤ α ≤ π

$$I_1\alpha = \frac{V_L}{Z} = V_m Y_{TCR(\alpha-\theta)} \quad (3)$$

Where

$$Y_{TCR(\alpha-\theta)} = Y_{Max}\left[\frac{1}{2\pi}\left\{(\beta - \alpha) + \frac{\sin 2\alpha}{2} - \frac{\sin 2\beta}{2}\right\}\right]^{0.5} \quad (4)$$

This TCR acts like a variable admittance. By varying the firing angle α admittance changes and consequently fundamental current component which in turn gives rise to variation of reactive power absorbed by reactor. Hence if α = θ = 85.5^0 continuous conduction of current take place. However, if firing angle is increased beyond this, non-sinusoidal currents are generated and hence harmonics get introduced. The rms value of n^{th} order harmonic is expressed as a function of α in the following equation.

$$I_1(\alpha) = \frac{V}{Z} \times \frac{2}{\pi}\left[\frac{-2\cos(\alpha - \theta)}{n}\sin n(\alpha - \theta) + \frac{\sin(n-1)(\alpha - \theta)}{n-1} + \frac{\sin(n+1)(\alpha - \theta)}{n+1}\right]$$

Where, n = 2k+1 and k = 1, 2, 3 . . . (5)

C. *Error Adaptive Power Factor Controller* :

A pioneering work in the Error Adaptive Power Factor Controller [EAPFC] was done by M.A. EI. Sharkawi et. al. [11],[12]. These EAPFC's do not make use of an inductor branch (TCR) as in SVC's but contributions to effective capacitor switching techniques are notable. The adaptive VAR compensation technology was developed at the University of Washington with sponsorship of Bonneville Power Administration (BPA) and Southern California Edison (SCE). The project was started in 1980 and ended in 1993. Subsequently related to this work number of papers were published [13]-[16]. The major work was carried in the design, development and implementation of 15 kV class of adaptive VAR compensator. The Adaptive Var Compensator (AVC), was solid state switched, binary stepped capacitor bank, used to compensate any rapidly changing reactive demand within one half cycle without introducing transients or harmonics.

In the light of all the developments that have been reported in the recent past, the desirable features for the controller to be developed are listed below which forms the main theme of work under taken.

- It maintains the power factor at the PCC to any specified value.

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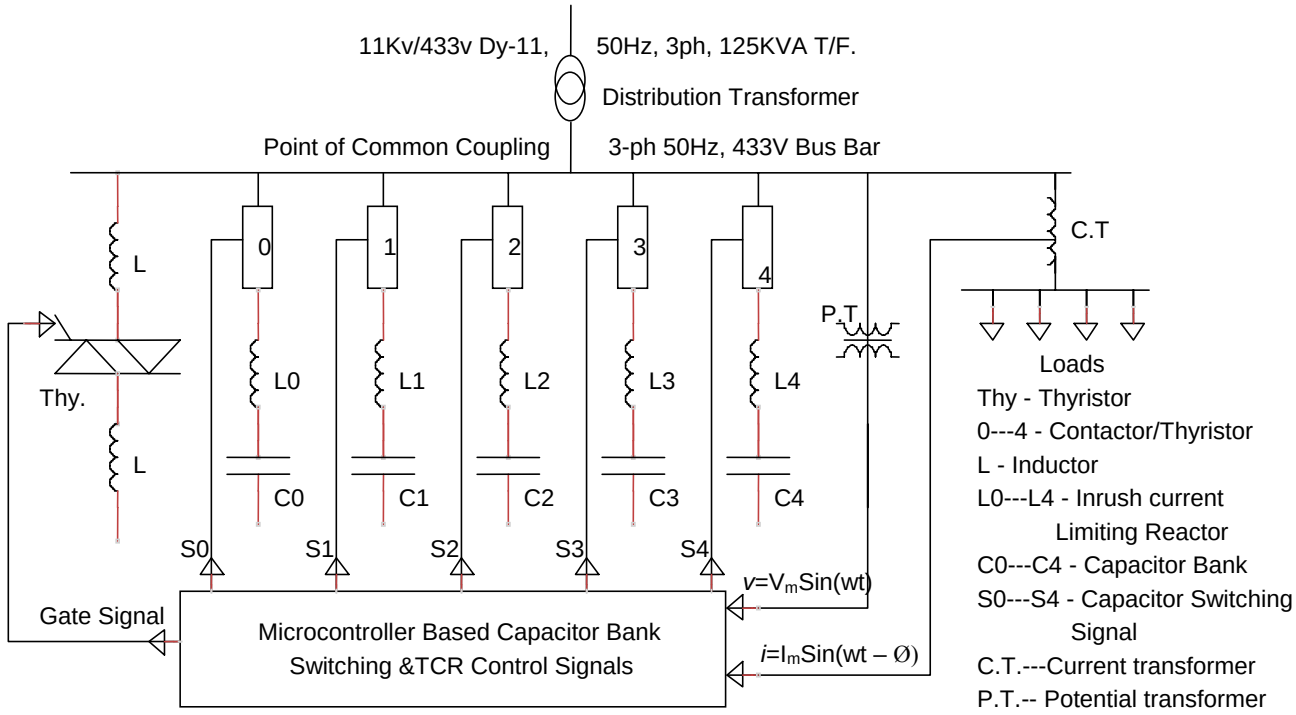

Fig. 3. Proposed Scheme for TBC and TCR

- It compensates for rapid variation in reactive power or voltages.
- Maximum compensation time is 10 msec. (1/2 of a cycle).
- No transients or harmonics are allowed to be present due to fast selective instants of switching in a well coordinated manner.
- It is adaptive in the sense that the amount of the compensation is determined and provided on a cycle by cycle basis.
- It can compensate each phase independently which makes ideal for unbalanced systems.
- It maintains the power factor at the PCC to any specified value.
- Capacitors are sized in binary sequential ratio for minimum size of switching steps (TBC).

The AVC can operate in any one of the following modes –

- Reactive Power Compensation (RPC) mode: Maintaining unity or other desired power factor at the point of common coupling (PCC) with an accuracy of smallest capacitor bit and with the limitation of total capacitance of the AVC per phase.
- Voltage support mode: Regulating the voltage at the point of or at some pre-specified level using under and/or over compensation.
- Flicker Control mode: Used to reduce the fast fluctuations in the voltage.

Any one of the modes can be implemented at a time and can be controlled by specified time scheduling [16]. The potential applications of AVC are at load end or at system level compensation. The load end application includes those requiring rapid compensation such as timber mills, rock crushing plants, steel mills, elevators, arc furnaces, pumps, electric traction. The distribution system application includes reactive VAR compensation, enhancement of voltage regulation, and prevention of voltage collapse, released system capacity, reduction in line losses and increase in efficiency. The innovative and useful design of the AVC has resulted in commercialization of the device and reported in three US patents [13],[17],[18]. All the above referred controllers do not have any reactor part (TCR) as such. To maintain the power factor at unity, binary steps required are high to reduce the resolution. But still these APFC's are robust, controllers catering to the sudden changes in reactive power demand and reduce voltage flicker.

D. *Processor Based Static VAR Compensators:*

In 1990, number of papers got published on microcontroller (Microprocessor) based static VAR compensator [19]. Also [20] gives the details of open loop control strategy of SVC; while in [19] hardware SVC model was developed for laboratory experiments. The model consists of FC-TCR scheme. The control strategy used was based on PD & PID. The paper [20] focused specific inductor control (TCR) through developing a prototype model. While in [21],[22] fuzzy logic control scheme was used. The goal of this fuzzy controller was to provide maximum damping and improve stability in the power system.

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II. The Proposed Binary Sequential Switched Capacitors and TCR Scheme

At the distribution transformer requiring total reactive power Q for improving the power factor from some initial value P_{f1} to the desired value P_{f2} at the load. This Q can be arranged in binary sequential 'n' steps, satisfying the following equation:

$$Q = 2^n C + 2^{n-1} C + ... + 2^2 C + 2^1 C + 2^0 C \qquad (6)$$

The schematic diagram of the capacitor bank in five binary sequential steps through contactors and with respective current limiting reactors is shown in Fig 3. An innovative error adaptive controller is designed, developed and tested for switching operations of the capacitor bank as required for the system under consideration. It possesses the following features.

- The control strategy is error activated to match with the load reactive power for the chosen time interval.
- It eliminates possible over compensation and resulting leading power factor.
- It is flexible to choose required number of steps as per the resolution.
- Resolution can be made small with more number of steps.
- Simple in principle, elegant in usage and of low cost
- Possible to incorporate the idea presented in the controllers for large size transformers at substations.

The controller receives both current and voltage signals through CT and PT, perform necessary calculations through an in built program and generates the activating signals S_0, S_1, S_2, S_3 and S_4 so as to match the reactive power from the compensator with the prevailing load demand. It calculates the reactive power with a microcontroller based processor along with data acquisition card and arrives at the compensation value and the corresponding steps to be kept on.

A. System Data for Experimental Set up:

Walchand college of Engineering, Sangli is getting the supply from State Electricity Board through 11 KV feeders and there are two transformers feeding various loads in the campus. Their ratings are as follows:
11 KV feeders of length 5 km Vishrambag substation to college premises have the following parameters.
Type of overhead line: -Mink 6/3.66
Over all Diameter = 11 mm; Sectional area= 63.1 mm2;
Approximate Weight = 254.9 Kg./Km.;
Current Carrying Capacity = 174 A
D.C. Resistance per Km distance =0.49 Ohms.
Reactance per Km distance =0.365 Ohms

III. Hardware Implementation

This section describes the various components for KVAR sensing used in the controller. The basic difference between SVC and proposed KVAR controller is that former handles the voltage regulation problem through TSC-TCR scheme while the latter performs smooth control with exact matching of reactive power resulting in improved voltage. This facilitates compensation of (lagging) reactive power by TSC-TCR scheme termed as SVC (KVAR controller). It includes KVAR sensor, ADC converter, zero crossing detectors, gate pulse generation for thyristor controlled reactor as well as capacitor switching ON/OFF circuit with the help of microcontroller 89C51. The general block diagram and its implementation in the form of a TSC-TCR type SVC on 11KV/433V, DY11, 125KVA, 3phase, 50Hz transformer at Walchand College of Engineering, Sangli has been shown in Fig. 4

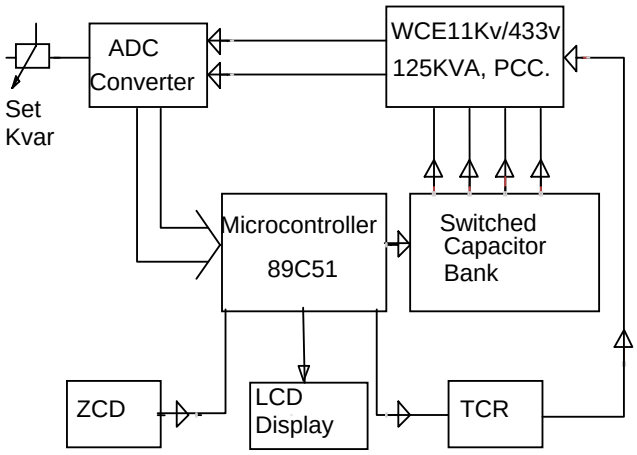

Fig.4. General Schematic Diagram of Digital SVC

A. Calculation of Reactive Power By Sampling:

At the point of common coupling, on the 125 KVA transformer, all the laboratory loads are connected. The actual KVAR at PCC is found by sensing current and voltage through CT and PT. These sensed signals are fed to the data acquisition ADC card. After sampling these signals for half cycle are multiplied element by element and their average value based on polarity is obtained and accordingly reactive power is calculated. The schematic of this sampling process through ADC with Microcontroller 89C51 is shown in Fig.5.

A. Digital KVAR Controller:

This closed loop digital system shown in Fig. 6 senses the KVAr of the system from the point of common coupling (PCC). It is carried out by obtaining I & V signals from CTs and PTs. Through the set point fixation, it is possible to set the PCC's jQ (reactive power) at any desired value. Almost preferred condition of unity power factor can be obtained by setting KVAr set point = 0. The comparison between set value and sensed value is carried out as follows:

$$KVAr_{error} = KVAr_{set} - KVAr_{sensed} = e(t)$$

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Where e(t) is the error signal, a measure of KVAr difference at that time. This error signal is sampled and processed further by proportional and integral controller as shown in Fig. 7.

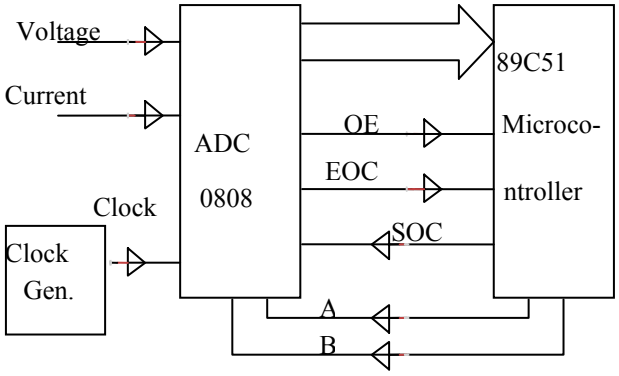

Fig. 5. Digital Data Acquisition through ADC

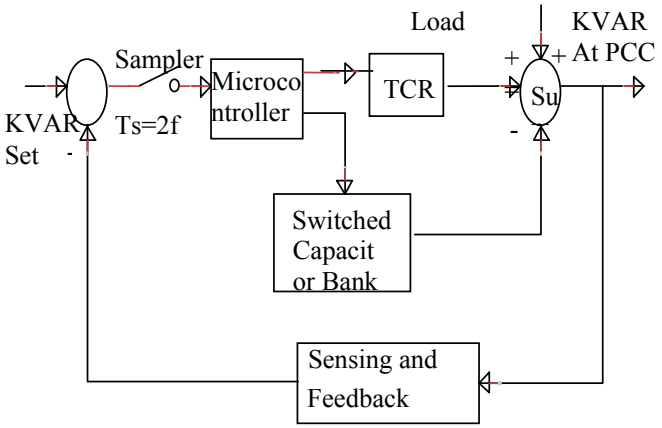

Fig. 6. Block Diagram of digital KVAR Controller.

Digital Controller :

It includes sampler, digital proportional, integral controller and ADC

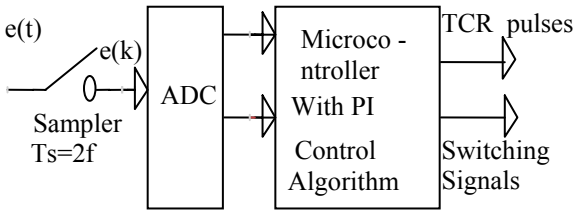

Fig. 7. Digital Controller

Sampling Rate Selection :

The sample and hold circuit can be incorporated through ADC. The sampling frequency f_s is kept just twice the fundamental frequency (f_f) of 50 Hz (i.e. period Ts = 10 ms). The reason behind this is the thyristor dead time required for the susceptance control of the reactor coil (I(α)). In case of 2 pulse TCR per phase firing angle α can change from 90^0 to 180^0 only once in a half cycle. Once the conduction starts in either of the half cycles any change in firing angle of the same thyristor will not have any effect. This restricts the sampling frequency, which cannot be more than twice the fundamental frequency. This is the inability of thyristor to respond at any arbitrary time instant and termed as thyristor dead time T_d. For a 2 pulse TCR this dead time is varying from 0 to T/2. Normally it is assigned to an average value of T/4 (5 ms). Extending the same argument for 6 pulse, delta connected TCR, sampling frequency may be increased up to six times the fundamental frequency ($T_s = 6f_0$), thyristor dead time becomes half of the T/6 i. e. T/12 (20/12 ≅ 1.7 ms). This thyristor dead time T_d and thyristor firing delay time T_y together can be represented by the transfer function,

$$G_y(s) = \frac{e^{-sT_d}}{1+sT_y} \tag{7}$$

$$\text{where, } T_d = \frac{T}{4} = 5 \text{ ms } \& \ T_y = \frac{T}{4} = 5 \text{ ms}$$

Digital Proportional, Integral Control Algorithm **:**

With a primary goal of damping the error signal e(t) and insuring the steady state error to zero, a proportional integral controller has been implemented as shown in fig. 7 and its expression is as follows.

$$u(t) = K_c\left[e(t) + \frac{1}{T_I}\int_0^t e(t)st\right] \tag{8}$$

Where,

u(t) = controller output
e(t) = error signal
K_c = controller gain
T_I = integral time constant

The above expression is approximated by using sampled values of e(t).

The proportional mode requires no approximation, since it is purely static part :

$$u_p(k) = K_c e(t) \tag{9}$$

The integral mode is approximated by trapezoidal rule for integration :

$$u_I(k) = \frac{K_c}{T_I}\int_0^{kT} e(t)dt$$

$$= \frac{K_c}{T_I}\int_0^{(k-1)T} e(t)dt - \frac{K_c}{T_I}\int_{(k-1)T}^{kT} e(t)dt$$

$$= u_I(k-1) + \frac{K_c}{T_I}\frac{T}{2}\left[e(k)+e(k-1)\right] \tag{10}$$

Bringing together , PI controller output is :

$$u(k) = u_p(k) + u_I(k)$$

$$\cong u(k-I) + K_c\left[e(k) + \frac{T}{2}[e(k)+e(k-1)]\right] \tag{11}$$

C. Thyristor Controlled Reactor(TCR

The designed air cored rectors are connected in delta as shown in Fig 9. Instead of thyristors, phase controlled solid state relays (SSR's) are used. The two coils are arranged in series, so that applied line voltage of 440 V is divided in to 220 volts each. As the firing angle increases beyond 85^0 by an angle α, the magnitude of fundamental component I_α goes on

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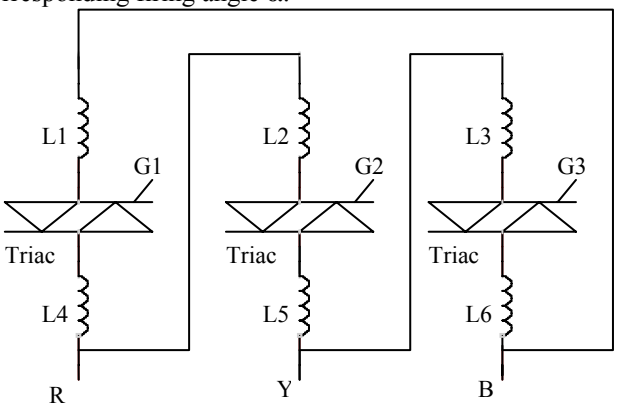
varying as per "(5)". Lagging KVAR is calculated by microcontroller and from lookup tables stored in the memory corresponding firing angle α is obtained. The lookup table provides the information regarding required KVAR and the corresponding firing angle α.



G1, G2, G3----Gate pulses
L1.....L6---Reactors

Fig. 8. Delta Connected TCR

The output of ADC varies from 00h to FFh for input variation of 0-5 volt d. c. (i. e. 100 KVAR lag) this numerical hex value gives the exact requirement of leading KVAR. This value of KVAR is used for capacitor switching strategy. Resultant switched capacitor KVAR is purposely kept on the leading side. This leading KVAR is then compensated by adjusting the conduction duration σ in the thyristor controlled reactor. The capacitor banks are arranged in binary sequence form i. e. in the multiplicity of 16, 8, 4, 2, 1 code. Therefore, $C_5 = 16C_1$; $C_4 = 8C_1$; $C_3 = 4C_1$, and $C_2=2C_1$ with basic unit of 2.5 KVAR.

IV. Experimental Results

All the above components are fabricated, tested and implemented at PCC of a 125 KVA, 433 volts distribution transformer. The load was increased from 30 Amp to 150 Amp. It is observed that without controller p.f. varies from 0.8 to 0.85 while with developed static Var compensator, it was in between 0.99 lag to 0.99 lead. The details of the system performance with and without SVC are given in the Table I, II ,III, IV and V respectively.

The voltage improvement, reduction in regulation, reduction in feeder losses, efficiency of feeder and relief obtained in KVA demand are depicted in Fig. 9 to Fig. 12 respectively.

Economic Justification:

In the college campus installation state electricity boards has been imposing penalties due to poor power factor and excessive maximum demand. The scheme that is proposed eliminates these penalties and college can avail the benefits of incentives by maintaining the power factor nearer to unity. On an average the college is paying the penalties to the tune of Rs 25000/- per month. The overall installation cost of the proposed scheme is of around Rs/- 1.2 lakh. Monthly savings due to incentives offered by state electricity boards for improvement in the power factor from .96 to unity p.f. is of 5 to 6 % of the monthly bill. The average monthly bill is around 5 lakh. Hence straight way monthly incentives obtained are of around 17,000/-. Also incentives are obtained due to reduction in maximum demand charges approximately Rs. 3000/-. Therefore the payback period comes out to be of 6 months for the system installed.

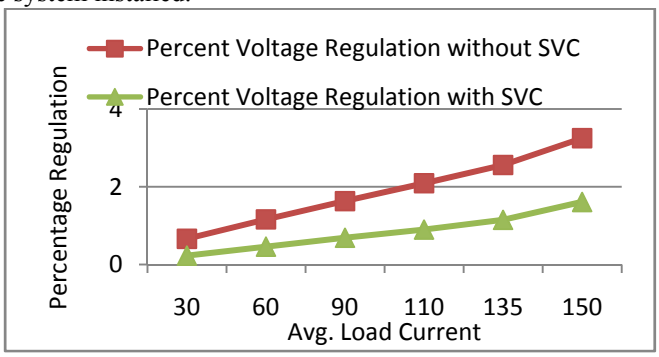


Fig. 9. Voltage Regulation

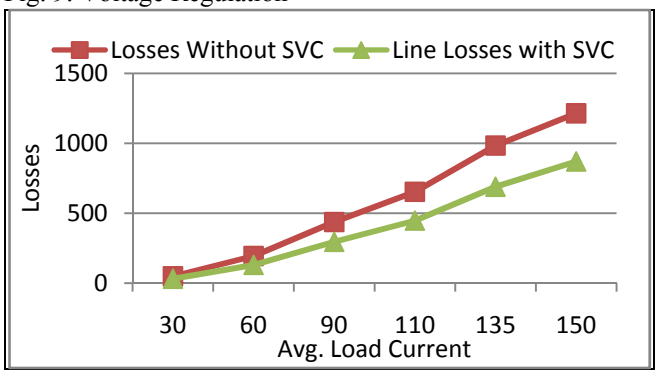


Fig. 10. Feeder Losses with and without SVC

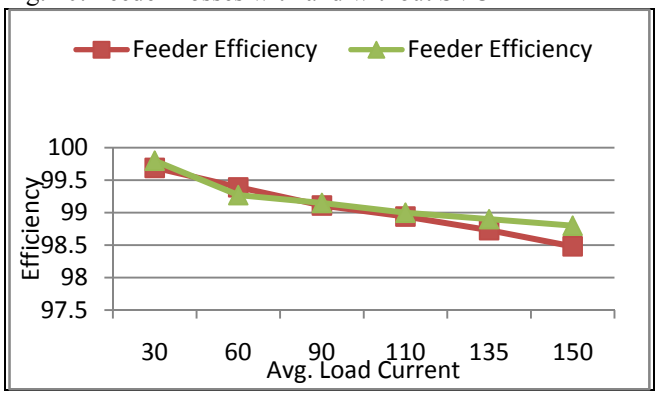


Fig. 11. Feeder Efficiency

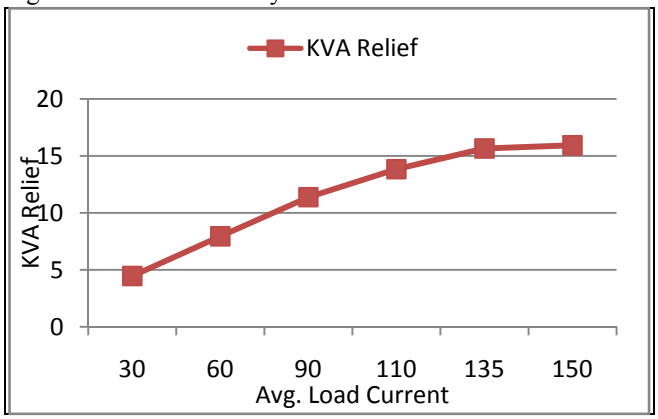


Fig. 12. KVA Relief with SVC

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TABLE I

DISTRIBUTION FEEDER PERFORMANCE WITHOUT COMPENSATOR

Sr. No.	Load Current Amp.	Power Factor Pf.	Real Power KW	Reactive Power KVAR	Apparent Power KVA	Receiving End Voltage Volts	Losses Watts	% Voltage Regulation	% Feeder Efficiency.
01	30.00	0.70	15.6	15.9	022.3	430.10	48.6	0.68	99.69
02	60.00	0.72	31.9	30.8	044.4	427.25	194.4	1.34	99.39
03	90.00	0.74	48.9	44.5	066.1	424.9	437.4	2.00	99.11
04	110.0	0.76	61.2	52.3	080.5	422.78	653.4	2.41	98.94
05	135.0	0.78	76.7	61.5	098.3	420.69	984.1	2.92	98.73
06	165.0	0.80	95.6	71.7	119.5	418.27	1470.1	3.52	98.48

TABLE II

KVAR COMPENSATION IN BINARY SEQUENTIAL STEPS FOR THE CASES REFERRED IN TABLE I

Sr. No.	Compensated Reactive Power KVAR in Binary sequential Steps					TCR Value KVAR Lag.	Reduced Current Amp.	Reduced Losses Watts	TCR + Capacitor Losses Watts	Net Losses TCR+Capacitor+Feeder losses Watts
	Q5	Q4	Q3	Q2	Q1					
01	-	-	10	5	2.5	1.6	21.00	23.8	47.9	71.17
02	-	20	10	-	2.5	1.7	43.20	100.8	55.9	156.7
03	40	-	-	5	-	00	66.60	239.5	3.75	243.25
04	40	-	10	-	2.5	0.2	83.60	377.4	5.12	382.52
05	40	20	-	-	2.5	1.0	105.30	598.8	24.4	623.2
06	40	20	10	-	2.5	0.8	132.00	940.9	18.45	959.35

TABLE III

RESULTS AFTER COMPENSATION FOR THE RESPECTIVE CASES OF TABLES I & II

Sr. No.	Receiving End Volts	% Voltage Reg.	% Feeder Eff.	Increased Load Current Capability Amp	Net Saving in Loss. Watts	Relief in KVA
01	432.3	0.15	99.84	9.00	-23	6.7
02	431.6	0.31	99.68	16.80	38	12.5
03	430.9	0.49	99.51	23.40	194	17.2
04	430.2	0.62	99.38	26.40	271	19.3
05	429.6	0.79	99.22	29.70	361	21.6
06	428.7	1.01	99.02	33.00	511	24.0

TABLE IV

SYSTEM PERFORMANCE WITHOUT SVC

Sr. No.	Avg. Load Current In Amp	Avg. P.F.	Avg. Voltage In volts	Active Power In Kw	Reactive Power In KVAr	Apparent Power In KVA	Percent Voltage Regulation	Losses In watts	Feeder Efficiency In %
1	30	0.8	430	17.9	13.4	22.36	0.66	48.6	99.69
2	60	0.82	428	36.4	25.35	44.35	1.16	194.4	99.39
3	90	0.83	426	55.1	37.19	66.48	1.63	437.4	99.11
4	110	0.83	424	67.0	45.24	80.84	2.09	653.4	98.94
5	135	0.84	422	82.8	53.28	98.46	2.56	984.1	98.73
6	150	0.85	419	92.5	56.6	108.44	3.25	1215	98.48

TABLE V

SYSTEM PERFORMANCE WITH SVC

Sr. No.	Load Current In Amps	Capacitor Bank steps Used	TCR Value KVAr	TCR Current Amps	Line Losses In watts	PCC Voltage In Volts	Percent Voltage Regulation	Feeder Efficiency In %	Increased Load Capability In Amps	KVA Relief
1	24	10+5	1.6	2.5	31	432	0.23	99.8	6	4.46
2	49	20+5	0.0	0.1	130	431	0.46	99.27	11	7.95
3	74	20+10+5+2.5	0.39	0.5	295	430	0.69	99.15	16	11.38
4	91	40+5	0.0	0.1	447	429	0.9	99.00	19	13.84
5	113	40+10+5	1.62	2.7	689	428	1.15	98.9	22	15.66
6	127	40+10+5+2.5	0.9	1.5	870	426	1.61	98.8	23	15.94

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V. CONCLUSION

A comprehensive static VAR compensator consisting of capacitor bank in five binary sequential steps in conjunction with a thyristor controlled reactor of smallest step size is employed in the investigative work. The work deals with the performance evaluation through analytical and practical implementation on an existing system. It is successfully tested on a distribution transformer of three phase 50 Hz.

Dy11, 11KV/440V, 125 KVA capacity. Theoretical and practical results are matching with each other. It gives the following benefits:

- Maintaining the power factor at unity.
- Minimum feeder current and loss reduction.
- Improvement in distribution feeder efficiency.
- Improvement in the voltage at load end.
- Relief in maximum demand and effective utilization of transformer capacity.
- Saving in monthly bill due to reduction in penalty on account of poor power factor, and reduction in maximum demand charges.
- Conservation of energy takes place.
- It is possible to get stepless control of Q closely matching with load requirements.
- The combination offers greater flexibility in control.
- There is substantial reduction in harmonics generated due to small size of reactor employed in the static VAR compensator.

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