Braun's Multipliers: A Delay Study

Mohammed H. Al Mijalli

***Abstract*—Field Programmable Gate Arrays (FPGAs) are required for real time efficient algorithms for medical imaging technology. Aim of this paper is to present the delay study of Braun's multipliers using Very High speed integrated circuit Hardware Description Language (VHDL) and implemented on Virtex-5 FPGA XC5VLX50, and XC5VLX50T devices. The delay study was analyzed using Analysis of Variance (ANOVA) method using the software Statistical Package for Social Science (SPSS). The One way ANOVA method using the SPSS with a 0.05 significance level was used to compare the Virtex-5 FPGA devices. Multiple comparison tests revealed that the differences between the FPGA Virtex-5 devices are insignificant.**

***Index Terms*—Braun's Multipliers, DSP, FPGA, Virtex-5, VHDL**

I. Introduction

FOR scientific computations, multiplication is an important and predominance in all digital signal processing (DSP) applications and its subfields. Application Specific Integrated Circuits (ASICs) utilizes as special purpose processor for DSP algorithms. Including ASICs there are supplementary tools used for DSP includes more powerful general purpose microprocessors, Field Programmable Gate Arrays (FPGAs), digital signal controllers, and stream processors.

The current development in modern FPGA technology has outnumbered ASICs and reached to such degree that the hardware implementation has become a desirable substitute, which makes FPGA a viable and an attractive alternative technology to ASICs [1].

Numerous research efforts have been presented in literature to achieve hardware efficient implementation of parallel multipliers [2-13]. In this study we have used contemporary Virtex-5 FPGA. The purpose of this paper is to present Braun's multipliers design and implementation on Virtex-5 FPGA devices and the statistical evaluation effect of the Braun's multipliers delays in XC5VLX50 and XC5VLX50T devices using one way analysis of variance (ANOVA) using the statistical Package for Social Science (SPSS) software.

This paper is structured as follows. In section II, describes the Braun's multipliers and its mathematical basis. Section III addresses the structural design used in this study. Section IV presents the FPGA delay results. Finally, section V presents the conclusion.

Manuscript received April 19, 2012. This work was supported in part by Cornea Research Chair, the College of Applied Medical Sciences, King Saud University.

M. H. Al Mijalli is with the Biomedical Technology Department, College of Applied Medical Sciences, King Saud University, Riyadh 11433, Saudi Arabia (e-mail: malmijalli@yahoo.com).

II. Braun's Multiplier

Braun's multiplier is an n × m bit parallel multiplier and generally known as carry save multiplier and is constructed with m × (n-1) addres and m × n AND gates. The Braun's multiplier has a glitching problem which is due to the ripple carry adder in the last stage of the multiplier.

A. Mathematical Basis

Consider a generic m by n multiplication of two unsigned n-bit numbers $Y = Y_{m-1} \ldots. Y_0$ and $X = X_{n-1} \ldots X_0$

$$Y = \sum_{i=0}^{m-1} Y_i 2^i \tag{1}$$

$$X = \sum_{i=0}^{n-1} X_i 2^i \tag{2}$$

The product $P = P_{2n-1} \ldots P_1 P_0$, which results from multiplying the multiplicand Y by the multiplier X, can be written as follows:

$$P = XY = \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} (X_i . Y_j) 2^{i+j} \tag{3}$$

III. Structural design

FPGA have the benefit of hardware speed and the flexibility of software. The flexibility of the FPGA allows for even higher performance by trading off precision and range in the number format for an increased number of parallel arithmetic units. The inherent parallelism of the logic resources on an FPGA allows for considerable computational throughput even at a low MHz clock rates. In this section a brief introduction about Virtex-5 from Xilinx is presented.

A. Virtex-5

The Virtex-5 devices [14] are a programmable alternative to custom ASIC technology. In Virtex-5 FPGAs, advanced DSP48E slices are available that helps in accelerating computation intensive DSP and image processing algorithms. These slices can operate at a maximum frequency of 550 MHz, drawing only 1.38 mW of power at 100 MHz frequency.

IV. FPGA Delay Results

The design of Braun's multipliers 4×4, 6×6, 8×8, and 12×12-bit are done using VHDL and implemented in a Xilinx Virtex-5 FPGA family; devices including XC5VLX50 (package: ff676, speed grade: -3), and XC5VLX50T

ISBN: 978-988-19252-1-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

(package: ff665, speed grade: -3) using the Xilinx ISE 9.2i design tool [15].

ANOVA is applied to compare the mean delay time for two devices including XC5VLX50 and XC5VLX50T FPGAs; using four multipliers 4×4, 6×6, 8×8, and 12×12. Table 1 summarizes the statistics of latency in Braun's multipliers for Virtex-5 XC5VLX50 and XC5VLX50T FPGAs. The mean value for multipliers in XC5VLX50 and XC5VLX50T are not similar for 6×6 and 8×8 bit multipliers.

There is a statistically insignificant difference at the 0.05 level in delay time for the two devices [F (1, 38) = .031, p = .861] compared by using ANOVA multiple comparison tests at the 0.05 significance level. The test indicates that the mean of delay time for XC5VLX50 (Mean = 9.02, Standard Deviation = 2.36) is insignificantly different from the other device; XC5VLX50T (Mean = 8.89, Standard Deviation = 2.29), which shows that both devices could be used for medical imaging technology.

Table 1: Statistics of latency in truncated multipliers for FPGAs

Virtex-5 Devices	Bit Width	Mean (ns)	Std. Deviation (ns)	Std. Error of Mean (ns)
XC5VLX50	4×4	6.58	0.2588	0.1158
	6 ×6	8.14	0.2881	0.1288
	8×8	8.6	0.1581	0.7707
	12×12	12.78	0.1304	0.0583
XC5VLX50T	4×4	6.78	0.5404	0.2417
	6 ×6	7.82	0.7396	0.3308
	8×8	8.46	0.0548	0.0245
	12×12	12.52	0.6221	0.2782

V. Conclusion

In this paper we have demonstrated delay study of Braun's multipliers utilizing VHDL. The design was implemented on Xilinx including XC5VLX50 and XC5VLX50T Virtex-5 devices using the Xilinx ISE 9.2i design tool.

The objective is to present a delay study of the Virtex-5 FPGA devices using 4×4, 6×6, 8×8, and 12×12-bit Braun's multipliers. The comparison between Virtex-5 devices shows insignificant results using ANOVA method using the software SPSS, which shows both devices, could be used for medical imaging technology.

References

[1] W. Stallings, "Cryptography and Network Security: Principles and Practices", Prentice-Hall, 4th edn. Upper Saddle River, NJ, 2006.

[2] M.H. Rais, M.H. Al Mijalli, "Braun's multipliers: Spartan-3AN based design and implementation", *J. Comput. Sci.*, vo. 7, no. (11), pp. 1629-1632, 2011.

[3] K.N.Vijeyakumar, V. Sumathy, S. Komanduri, C.C.G. Suji, "Design of low- power high-speed error tolerant shift and add multiplier", *J. Comput. Sci.*, vol. 7, no. (12), pp. 1839-1845. 2011.

[4] M.H. Rais, M.H. Al Mijalli, "Field programmable gate arrays based design, implementation and delay study of Braun's multipliers", *J. Computer Sci.*, vol. 8, no. (2), pp. 227-231, 2012.

[5] M.H. Rais, M.H. Al Mijalli, "Field programmable gate arrays based realization of truncated multipliers", *Am. J. Applied Sci.*, vol. 8, no. (7), pp. 681-684, 2011.

[6] M.H. Al-Mijalli, "Spartan-3AN field programmable gate arrays truncated multipliers delay study", *Am. J. Applied Sci.*, vol. 8, no. (6), pp. 554-557, 2011.

[7] M.H. Al Mijalli, "FPGA Based Truncated Multipliers: A Study of Latency in FPGA Devices", *European J. Sci. Res.*, vol. 60, no. (2), pp. 273-279, 2011.

[8] M. H. Rais, M. H. Al Mijalli, "Reconfigurable Design and Implementation of Standard and Truncated Multipliers Using Spartan-3AN, Spartan-3E, Virtex-2 and Virtex-4 FPGAs", *European J. Sci. Res.*, vol.60, no. (3), pp.469-481, 2011

[9] M. H. Rais, M. H. Al Mijalli, M. Nisar, "Resource Efficient Design and Implementation of Standard and Truncated Multipliers using FPGAs", *in Proc. of the World Congress on Engineering*, vol. II, 2011.

[10] M. H. Al Mijalli, "Delay Study of Virtex-2, Virtex-4 and Spartan-3E Based Truncated Multipliers", *Int. J. Comput. Sci. Network Security*, vol. 11, no. (7), pp. 68-71, 2011.

[11] M. H. Rais, M. H. Al Mijalli, "Virtex-5 FPGA Based Braun's Multipliers", *Int. J. Comput. Sci. Network Security*, vol. 11, no. (8), pp. 81-84, 2011.

[12] M.N.M. Isa, M.I. Ahmad, S.A.Z. Murad, M.K.M. Arshad, "FPGA Based SPWM Bridge Inverter", *Am. J. Applied Sci.*, vol. 4, no. (8), pp. 584-586. 2007.

[13] Y.S. Algnabi, R. Teymourzadeh, M. Othman, M.S. Islam, M.V. Hong, "On-Chip Implementation of Pipeline Digit-Slicing Multiplier-Less Butterfly for Fast Fourier Transform Architecture", Am. J. Eng. Applied Sci., vol. 3, no. (4), pp. 757-764, 2010.

[14] Xilinx, Virtex-5 FPGA family datasheet, (2009). http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf

[15] Xilinx, ISE 9.2i design tool, (2007). www.xilinx.com/prs_rls/2007/software/0786_ise92i.htm

ISBN: 978-988-19252-1-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)