Analytical Investigation of Subthreshold Swing to Study the Scaling Capability of Graphene Field-effect Transistors

K. Tamersit, F. Djeffal, D. Arar and M. Meguellati

Abstract— **In this paper, we investigate the scaling capability of planar Graphene field-effect transistors G-FETs using an analytical analysis of the subthreshold swing. To obtain such analytical investigation, an analytical expression of the channel potential is presented through the use of a good approximation. Then an analytical expression for subthreshold swing is achieved, which is given as function of electrical and dimensional parameters. Based on the developed model, we have studied the immunity of the G-FETs against the short-channel-effects and the scalability limits of Graphene and Silicon FETs and compared their performances. In addition, in this work we show through illustrative computations the challenges to use the graphene-based devices for low power and digital applications. The proposed analytical analysis can be applied to design and optimize the G-FETs for digital nanoelectronic applications.**

Index Terms— **Graphene, FET, bandgap-engineering, subthreshold swing.**

I. Introduction

In today's world, the importance of Graphene-based device is rising in nanoelectronic design. This is mainly due to the low manufacturing costs of graphene and its outstanding electronic properties [1, 3]. In addition, the graphene material exhibits very high mobility (10cm2/V.s) and saturation velocity (108 cm/s), together with a promising ability to scale to short gate lengths and high speeds by virtue of its thinness. Recently, some analytical investigations have been proposed to analyze the G-FET and to make us better understanding of its physics [3-10]. The main disadvantage of the G-FET is the absence of a gap, therefore limiting the usefulness in digital applications. Accurate analytical models, to study the device subthreshold behavior, are very important in improving the G-FET performance during fabrication process and in device simulation and modeling. Therefore, In this work, we investigate the G-FET at nanoscale regime and, in doing so; we tackle the drift-diffusion carrier transport, which is accurate to explain the electrical behavior of G-FETs [7,8]. Assuming a concept of device turn-off caused by the applied gate voltage, the analytical model explains the dependence of subthreshold swing (S) according to the dielectric thickness, dielectric values, and graphene width and channel length. Analytical models obtained from this work will be used to study the scaling capability of G-FETs for Subthreshold applications.

In this work, we investigate the G-FET, without bandgap engineering, at deep submicron regime and, in doing so; we tackle the drift-diffusion carrier transport, which is accurate to explain the electrical behavior of G-FETs [12]. New analytical subthreshold swing model comprising subthreshold current and subthreshold swing factor have been developed in order to investigate the scaling capability of the G-FET over the conventional Dual Gate Silicon MOSFET with the same geometric specifications. This investigation will be used to study scaling capability and the immunity of the analyzed G-FET design against the short-channel- effects. The results so obtained are in close proximity with the experimental results thus confirming the validity of the proposed models.

This paper is organized as follows. In Sect. 2, we derive the analytical expression of the drain current. The subthreshold swing, threshold voltage and DIBL effects can then be determined based on the drain current model. In Sect. 3, we investigate the scalability of G-FETs based on our calculated subthreshold parameters. The conclusions will be drawn in Sect. 4.

II. Analytical analysis

Figure.1 shows the cross sections of the G-FET considered in this work. The electrostatics of this device can be understood using the equivalent capacitive circuit from [12].The current density primarily flows from the drain to the source and consists of both terms of drift current and diffusion current. The 1-D potential model proposed by [11] can be used to drive the explicit analytical current equation in the subthreshold regime. For this, we follow the procedure proposed for Dual- gate G-FETs [11]. In the weak inversion region, the current is principally diffusion dominated and proportional to the electron concentration.

The voltage drop in the graphene channel V(x), which is zero at the source end at x=0 and equal to the drain-source voltage (Vds) at the drain end at x=L, is considered the main parameter which controls the drain current. Therefore, the development of an analytical expression of this parameter is important.

K. Tamersit is with the Laboratory of Advanced Electronic, Department of Electronics, University of Batna, 05000, Algeria (e-mail: K-Tamersit@ gmail.com).

F. Djeffal is with the Laboratory of Advanced Electronic, Department of Electronics, LEPCM, University of Batna, 05000, Algeria (e-mail: faycaldzdz@hotmail.com, faycal.djeffal@univ-batna.dz).

D. Arar is with the Laboratory of Advanced Electronic, Department of Electronics, University of Batna, 05000, Algeria (e-mail: hakosp82@yahoo.com).

M. Meguellati is with the Laboratory of Advanced Electronic, Department of Electronics, University of Batna, 05000, Algeria (e-mail: m_meguellati @yahoo.fr).

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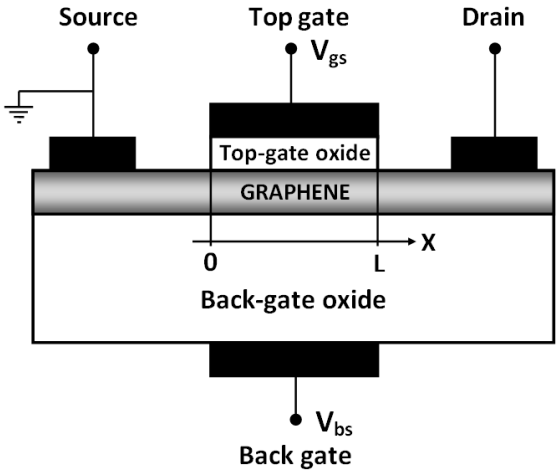

Figure 1. 2D Cross section Dual- Gate G-FET considered in this work: Graphene channel and metal-like source/drain regions are used in this study

Applying circuit laws to the equivalent capacitive circuit and noting that the overall net mobile sheet charge density in the graphene channel the following relation is [12] obtained:

$$V_c(x) = \left(V_{gs} - V_{gs_0} - V(x)\right)\frac{C_t}{C_t + C_b + \frac{1}{2}C_q} + \left(V_{bs} - V_{bs_0} - V(x)\right)\frac{C_b}{C_t + C_b + \frac{1}{2}C_q} \quad (1)$$

where C_t and C_b are the top and bottom oxide capacitances. $C_q = k|V_c|$ represents quantum capacitance of the graphene, the potential V_c represents the voltage drop across C_q, $k = (2q^2/\pi)\left(q/(\hbar v_F)^2\right)$, $v_F (= 10^6\, m/s)$ is the Fermi velocity. The potential V_c can be obtained from Eq.1 [11], $V_{gs} - V_{gs_0}$ and $V_{bs} - V_{bs_0}$ are the top and back gate-source voltage overdrive, respectively. These quantities comprise work-function differences between the gates and the graphene channel, eventual charged interface states at the graphene/oxide interfaces, and possible doping of the graphene.

To study the drain-current behavior in subthreshold regime a drift-diffusion carrier transport is assumed under the form $I_{ds} = -W\,|Q_c(x)|\,v(x)$, where W is the gate width, $Q_c(x)$ is the free carrier sheet density in the channel at position x, which is mainly depends on the channel potential V(x); and v(x) represents the carrier drift velocity in the channel.

After some mathematical manipulations, the subthreshold current derived for our G-FET can be expressed [12] as

$$I_{ds} = \frac{\mu W \int_{Vcs}^{Vcd} |Q_c(V_c)|\frac{dV}{dV_c}dV_c}{L + \mu\frac{|V_{ds}|}{v_F}} \quad (2)$$

where μ represents the electron mobility in the channel, L is the channel length.

The solution of (2) leads to:

$$I_{ds} = \frac{\mu k}{2}\frac{W}{L_{eff}}\left|g(V_c)\right|_{V_{cs}}^{V_{cd}} \quad (3)$$

with $g(V_c) = \frac{-V_c^3}{3} - sgn(V_c)\frac{kV_c^4}{4(C_t + C_b)}$

and $L_{eff} = L + \mu\frac{|V_{ds}|}{v_F}$.

A negative (positive) V_c means that the channel charge density is dominated by holes (electrons).

The key electrical parameter that indicates the impact of short channel effects on a FET is the subthreshold swing (S) [5-7]. S is defined as the required change in the applied gate voltage that results in an order-of-magnitude change in the subthreshold current. Therefore, the study of the impact of the device electrical and dimensional parameters on the subthreshold swing behavior becomes very important in order to study the scaling capability of the G-FET for digital applications. A general subthreshold swing (S) model is obtained as

$$S = \frac{\partial V_{gs}}{\partial \log I_{ds}} = \left[\frac{\partial \log I_{ds}}{\partial V_{gs}}\right]^{-1} = \left[\frac{\frac{\partial I_{ds}}{\partial V_{gs}}}{I_{ds}\,ln(10)}\right]^{-1} = \left[\frac{g_m}{I_{ds}\,ln(10)}\right]^{-1} \quad (4)$$

where g_m represents the transconductance function in subthreshold domain. This latter can be calculated from the subthreshold drain current model as,

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\partial I_{ds}}{\partial V_{cd}}\times\frac{\partial V_{cd}}{\partial V_{gs}} + \frac{\partial I_{ds}}{\partial V_{cs}}\times\frac{\partial V_{cs}}{\partial V_{gs}} = \frac{\mu k}{2}\frac{W}{L_{eff}}\left(\frac{g'(V_{cd})}{1 + sgn(V_{cd})\frac{kV_{cd}}{C_t + C_b}} - \frac{g'(V_{cs})}{1 + sgn(V_{cs})\frac{kV_{cs}}{C_t + C_b}}\right) \quad (5)$$

with $g'(Vc) = -Vc^2 - sgn(Vc)\frac{kVc^3}{Ct + Cb}$.

Substituting (5) and (3) in (4), an analytical subthreshold swing model can obtained.

The developed compact subthreshold swing will be used to plot a graphical abacus to study the scaling capability of the G-FET.

III. RESULTS AND DISCUSSION

Figure.2 shows the variation of the subthreshold drain current as function of applied top gate voltage (for different applied drain source voltages) at applied top gate voltage, , for $L=1\mu m$, $W=2.1\ \mu m$, and , the high-quality HfO_2 dielectric layer is used as top-gate insulator. The simulated voltage range is extended beyond the experiment range to show the predictive behavior of the analytical model. The obtained results show good agreement in comparison with experimental measurements [13].

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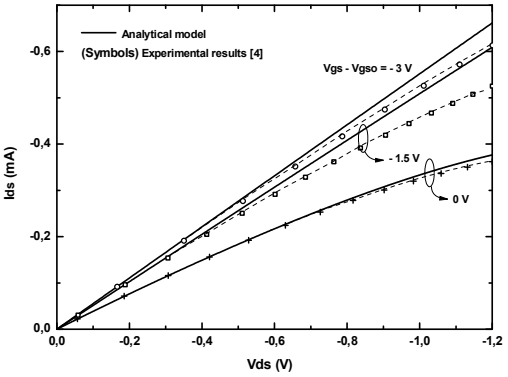

Figure 2. Output characteristics obtained from the analytical model compared with experimental results

Figure.3 plots the subthreshold swing as a function the device dimensions calculated from our analytical model. The subthreshold swing is predicted for both designs, Graphene and Silicon-based FETs, and compared for equal electrical and geometrical parameters. It can be shown that the subthreshold swing increases rapidly as the G-FET lengths down to small values. In addition, the subthreshold swing reaches its better value (S=95mV/Dec) for Channel length L ≥ 1µm. Contrary, the subthreshold swing maintains its ideal value (S=60mV/Dec) for full channel length range in the case of Dual Gate Si FET. It is noticed that the subthreshold swing, in the case of G-FET, does not reach the ideal value contrary to the Dual-gate Si FETs. Therefore, the DG Si FET structure is more stable in subthreshold regime, in comparison to the G-FET design, which indicates the fact that the incorporation of graphene-based channel leads to a degradation of short-channel-effects. Consequently, new graphene fabrication process and design approaches should be developed in order to improve the device performance for digital applications.

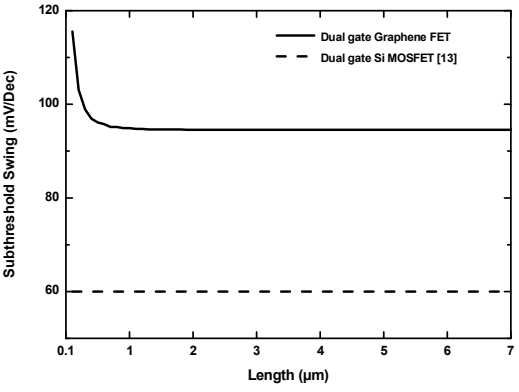

Figure 3. Subthreshold swing versus channel length

The predicted results of our analytical subthreshold swing model are used to form a graphical abacus in order to study the scaling capability of the G-FETs as it is illustrated in Fig. 4. The evolution of the subthreshold swing shows the effect of the top-gated graphene design on the law of scaling capability of the G-FETs. Clearly, G-FETs (with L=0.1µm and ttop-gate =2nm) are likely t o be used for the condition where S = 79 mV/dec is tolerable. Also, the short- channel-effect is improved as the insulator thickness is narrow due to the higher gate to channel coupling relative to source/drain to channel coupling.

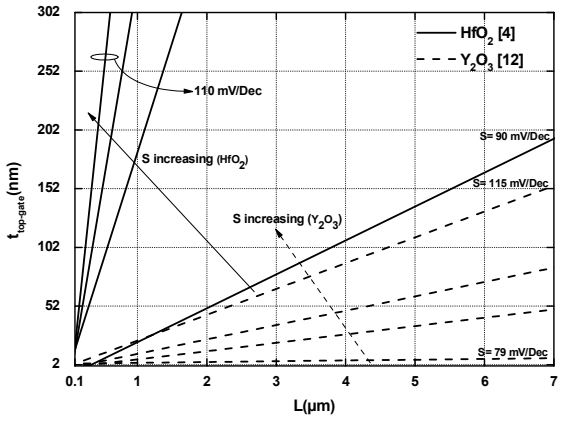

Figure 4. Graphical abacus which allows studying the scaling capability of the G-FETs

In addition, it has been found that the scaling capability is improved for the case of Y2O3 top-gate insulator in comparison to the HfO2 dielectric one, where a tolerable subthreshold swing value, S = 79 mV/dec, can be found in this case. Our results show that Y2O3 may be the ultimate dielectric material for graphene. It is also shown the Y2O3 gate dielectric layer with thickness of 2nm may also satisfy the ultimate vertical and lateral scaling requirement on the gate length of G-FET and be used effectively to control a G-FET with a gate length as small as 0.1µm. It is to note that the ideal subthreshold swing value, 60 mV/dec, cannot be reached by the G-FETs. Contrary, the subthreshold swing maintains its ideal value (S=60mV/Dec) for full channel length range in the case of Dual Gate Si FET [14]. Therefore, the G-FETs cannot provide an excellent immunity against the short-channel-effects. Consequently, new design approaches and planar graphene elaboration process should be developed in order to enhance the subthreshold behavior for planar G-FET-based digital applications.

IV. Conclusion

In this paper, we investigate the G-FET, without bandgap engineering, at deep submicron regime. In this context, we have presented an analytical analysis of the subthreshold performance for Dual- Gate G-FET in order to study the scalability behavior of this device. The analytical model has been used to predict and compare the performance of downscaled Dual- Gate G-FET. The high subthreshold swing values, for the G-FETs, diminish for drain current near the dirac-point of the output characteristics due to the decreasing of the gate controllability of the channel. This effect seriously limits the speed commutation performance of G-FETs, which

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is an important parameter for digital applications. The law of scaling capability of the proposed investigated device was compared to the conventional Dual- Gate Silicon (Si) -FET, illustrating the degraded subthreshold behavior of the Dual-Gate G-FET over Dual- Gate Si-MOSFET. As device dimensions penetrate into the deep submicron regime, the degraded obtained subthreshold performance makes G-FETs a worse choice for deep submicron digital G-FET-based devices. Therefore, new graphene fabrication process and design approaches should be developed in order to improve the device immunity against the short-channel-effects and the scalability limits of the G-FETs for digital applications. It is to note that the proposed investigation can be extended to study the nanoscale G-FET behavior for analog applications. However, new complex and compact models that include the ballistic transport and quantum effects should be developed. The obtained results may provide a theoretical basis and physical insights for submicron planar G-FET design including short-channel-effects.

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