

Analysis of Phase Noise Profile of a 1.1 GHz Phase-locked Loop

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Abstract – We analyzed the phase noise of a 1.1 GHz phase-locked loop system for frequency synthesis. The system has been designed, fabricated and tested in the Instrumentation and Informatics Research Laboratory, Department of Electronics & Communication Technology, Gauhati University, Assam, INDIA. Details results of the analysis have been presented in this paper.

Index Terms - Phase Noise, Phase Locked Loop, Charge pump, Spectrum Analyzer

I. INTRODUCTION

Phase noise (PN) in phase locked loop (PLL) system is an important parameter in communication system. It degrades the system performance by increasing bit error rate (BER). The PLL concept was first appeared in the papers by Appleton in 1923 and de Bellescize in 1932 [1]. It is essentially a control system which employs feedback mechanism to synchronize the phase of output signal with the phase of a reference signal [2], [3]. When the PLL is in lock, there is a small phase difference between the two input signals of a phase frequency detector (PFD) and produce a dc voltage at the detector output, which is required to shift voltage controlled oscillator (VCO) from its free-running frequency and keep the loop in lock.

A basic PLL consists of a VCO, a PFD and a loop filter (LF). In the modern PLL system a charge pump (CP) is included with the PFD unit. It produces a current proportional to the error between the reference and feedback signal. The block diagram of a simple PLL is shown in Fig. 1.

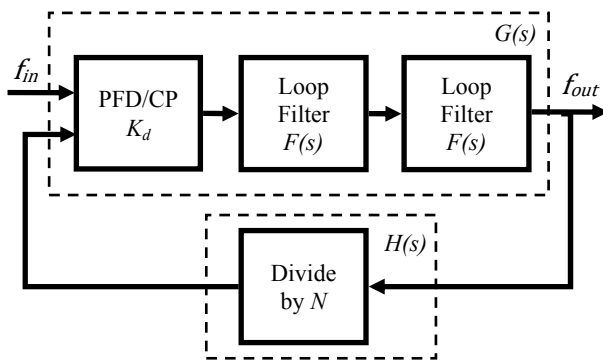


Fig.1: Block diagram of PLL

The PFD compares the phase of the output signal to the phase of the reference signal. If there is a phase difference between the two signals, it generates an output voltage, which is proportional to the phase error of the two signals. This output voltage passes through the LF whose function is

to filter any high frequency harmonics from the PFD and to provide a dc signal output. The LF output is then fed to the VCO as control voltage to control the output frequency. Due to this self-correcting technique, the output signal will be in phase with the reference signal. When both signals are synchronized, the PLL is said to be in lock condition. The phase error between the two signals is zero or almost zero at this state. As long as the initial difference between the input signal and the VCO is not too big, the PLL locks onto the input signal.

There is various noise sources present in the PLL system. Noise sources in the PLL circuit can be divided into two groups – (i) device noise and (ii) interference [4]. Thermal, shot, and flicker noise are included in the device noise and substrate and supply noise are included in the interference noise.

All the PLL output noises are generated by the reference signal, the PFD/CP unit, the LF, the VCO and the frequency divider (FD). The VCO PN is high pass filtered by PLL. Hence, the noise from the VCO at lower frequencies can be corrected relatively fast by the PLL. Again, the noises from the reference frequency, the PFD, the CP and the frequency divider are filtered at the PLL output. The resistor in the LF produces thermal noise in the synthesizer. The thermal noise of the resistor is band pass filtered at the PLL output. The noise gets increased as the value of resistor increases. Reference spurs appear in the sideband of PLL spectrum due to the coupling of the reference frequency to the VCO control voltage, the UP and DOWN mismatch of the PFD, and the charge injection mismatch of CP.

The PN is one of the most critical performance parameters of PLL system. The ultimate goal in any design of PLL system is to generate precise and stable output frequencies with fast switching and minimal spurious and PN. The output of an ideal PLL should be a single tone at the output in order to provide a stable channel frequency in the desired output frequency. The random amplitude and phase deviations from the desired values produce the energy sideband of the desired frequency and undesired sidebands are produced. The performance of PLL depends on PN and spurious tones of the system. Reference spurs are also undesirable signals besides the PN which can affect the performance of the PLL system. The location of these sidebands depends upon the reference input signal.

Noise in the control path of a VCO translates directly into PN in the output signal by frequency modulation. It can cause distortion or complete loss of incoming information in traditional receivers. This PN degrades the synthesizer's performance and causes the communication system to have a higher BER. This makes it a necessity to predict and understand this noise in the oscillator, so that its effect on the system can be minimized. Hence, predicting and analysis of noise in high frequency system at the design stage is extremely important.

In view of the above we propose to design, fabricate

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and analyze phase noise of a 1.1GHz PLL frequency synthesizer suitable for wireless communication systems.

II. SYSTEM DESIGN AND HARDWARE FABRICATION

The proposed system is consists of a frequency synthesizer (ADF4002), a passive LF, a VCO (MC100EL1648), a reference frequency generator. The system is interfaced with an 8085 microprocessor (μ P) unit through a buffer amplifier unit. The complete block diagram of the proposed system is shown in Fig. 2. The synthesizer consists of a low noise PFD, a programmable R divider, a feedback frequency N divider, and a precision CP.

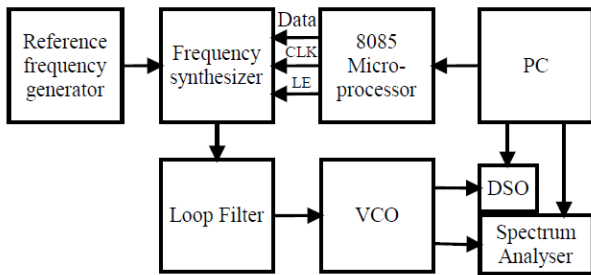


Fig.2: Block diagram of proposed PLL

The R divider allows the input reference frequency to be divided down to produce the reference clock (CLK) for the PFD. It has a wide range of division ratio from 1 to 16383. The N divider is a 13-bit counter and has division ratios from 1 to 8191 [5]. The PFD compares the phase and frequency of the signal from R and N divider. It produces an output control signal proportional to the phase and frequency difference between them. The on-chip registers of the synthesizer can be programmed externally by using serial peripheral interface (SPI) through writing to CLK, DATA and latch enable (LE) control of the device. The maximum allowable CLK rate of the device is 20MHz. The system is interfaced to personal computer (PC) through 8085 μ P via RS232 for writing data to the device. The synthesizer includes a 24-bit shift register where the data is clocked down on each rising edge of the signal. Initially, the data is clocked with most significant bit (MSB) and transferred from the shift register to one of the four latches available in the device on the rising edge of latch enable (LE). The destination latch is determined by the state of the two least significant bits (LSB) in the shift register. An external parallel tank circuit consisting of an inductor and a capacitor is used with the VCO to adjust the frequency. The varactor diode (MMBV609) with a parallel inductor is connected into the tank circuit to provide a voltage variable capacitance for the input of the VCO. These components have direct impact on the tuning sensitivity and PN. The quality factor (Q) of the tank circuit has direct impact on the resulting PN of the oscillator [6]. Therefore, the Q is kept high for lower PN in the oscillator. The typical operating frequency of the VCO is 1100MHz.

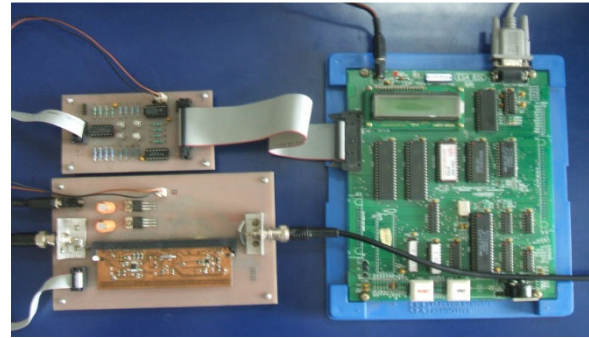


Fig.3: Hardware of PLL system

The VCO output is fed to Spectrum Analyzer and Digital Phosphor Oscilloscope (DPO) to record the data of the system. The spectrum analyzer and the DPO is interfaced to PC via universal serial bus (USB) for online monitoring and recording data.

IV. PROGRAMMING FOR HARDWARE CONTROLLING

The PLL is programmed by using initialization latch method. In this method, data for initialization latch is clocked first by setting the LSB of data set to 11 after initially powering up the device. Then the data for function latch, R and N divider are clocked by setting LSB to 10, 00 and 01 respectively. A microprocessor 8085 is used to program the device. The program was developed in 8085 simulator IDE from OshonSoft with user-friendly graphical development environment for Windows with integrated simulator, basic compiler, assembler, de-assembler and debugger for Intel 8085. The developed program is then transferred to 8085 processor from the PC.

V. EXPERIMENTAL RESULTS

The output PN of the PLL is measured with a Spectrum Analyzer (Agilent, Model: N9320B, 9 KHz - 3 GHz). The gain of the VCO used in the system is kept at 31 MHz/V. The loop bandwidth of the PLL system is 3.5 KHz and Phase Margin is 46°. A second order LF is used in the loop and hence forms a third order system. The loop BW is selected to optimize the output PN and to maintain reasonable settling time and spur rejection. The CP current is set at 2.5 mA. Output frequency spectrum of the system is shown in the Fig. 4, 5, 6 and 7 for the locked frequency of 212.1 MHz, 226.3 MHz, 240.4 MHz and 254.6 MHz respectively. The output power of the locked frequencies is recorded and given in Table. 1. The recorded PN is - 71.13 dBc/Hz and - 121.8 dBc/Hz at 1 kHz and 1 MHz offset respectively from the carrier for the locked frequency of 212.1 MHz. The output of PN at different offset is shown in Fig. 8, 9 and 10.



Fig.4: Output spectrum of the frequency synthesizer at 212.1 MHz

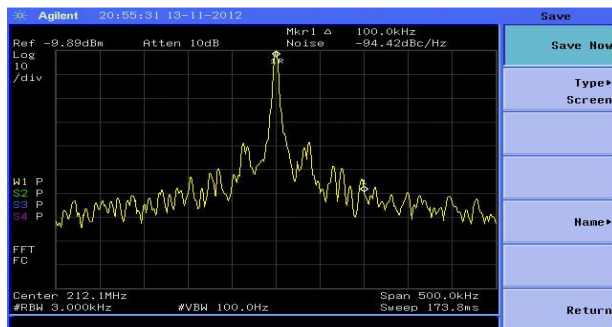


Fig.9: PN at 100 kHz offset from the carrier when system locked at 212.1 MHz

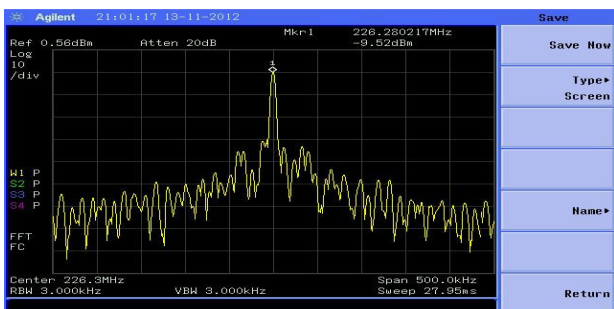


Fig.5: Output spectrum of the frequency synthesizer at 226.3 MHz

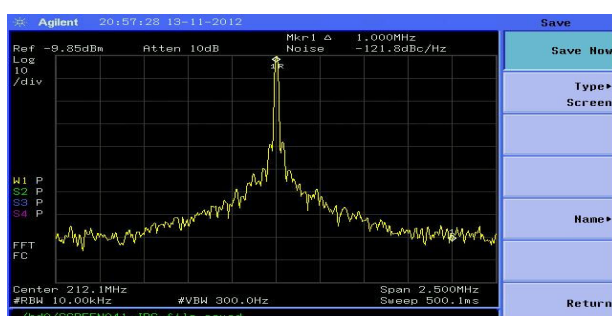


Fig.10: PN at 1 MHz offset from the carrier when system is locked at 212.1 MHz

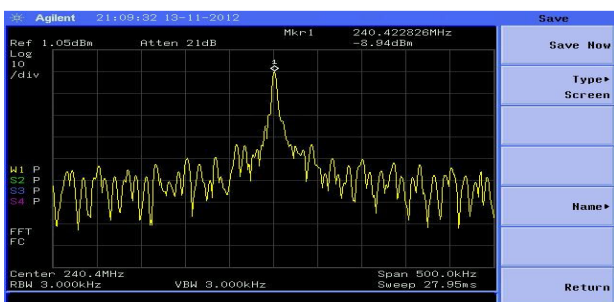


Fig.6: Output spectrum of the frequency synthesizer at 240.4 MHz

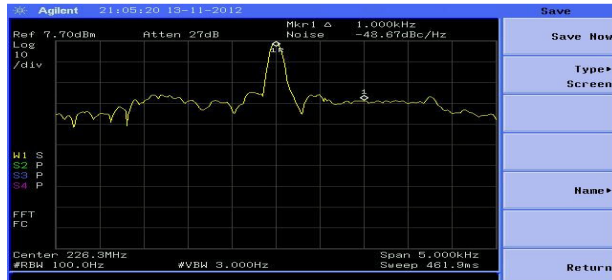


Fig.11: PN at 1 kHz offset from the carrier when system is locked at 226.3 MHz

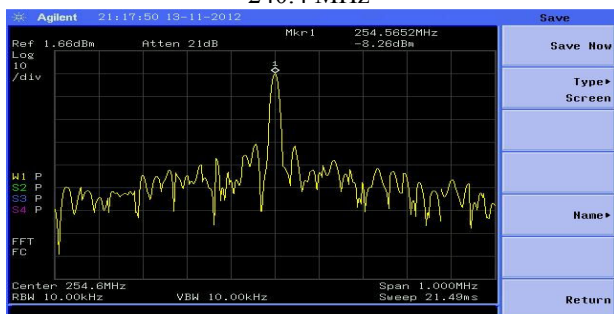


Fig.7: Output spectrum of the frequency synthesizer at 254.6 MHz

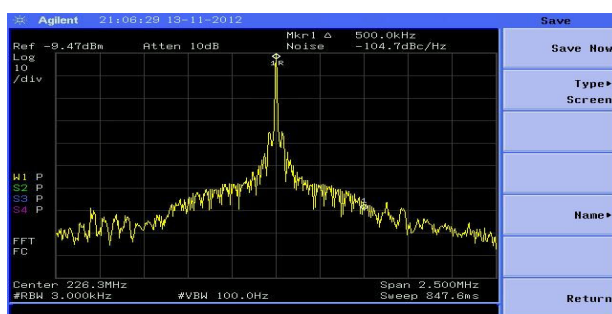


Fig.10: PN at 500 kHz offset from the carrier when system is locked at 226.3 MHz

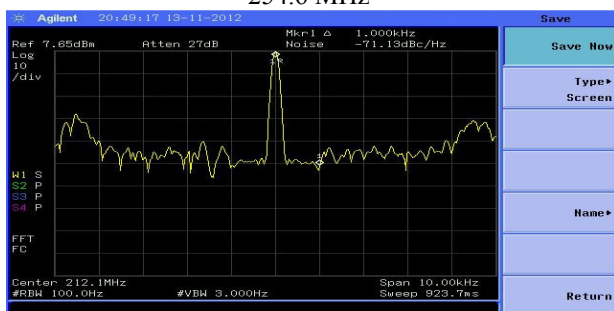


Fig.8: PN at 1 kHz offset from the carrier when system is locked at 212.1 MHz

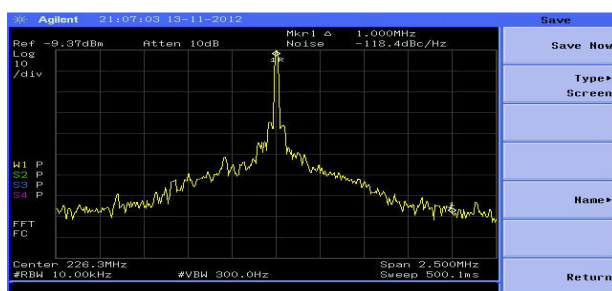


Fig.11: PN at 1 MHz offset from the carrier when system is locked at 226.3 MHz

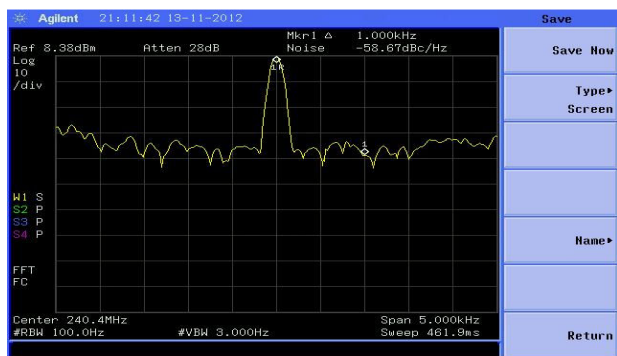


Fig.12: PN at 1 kHz offset from the carrier when system is locked at 240.4 MHz

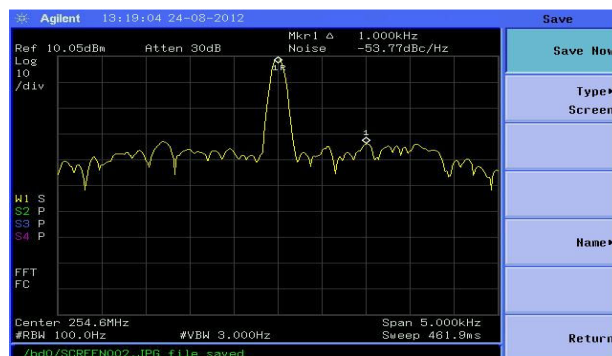


Fig.14: PN at 1 kHz offset from the carrier when system is locked at 254.6 MHz

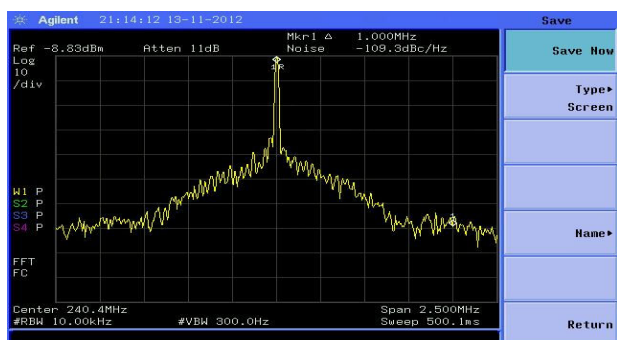


Fig.13: PN at 1 MHz offset from the carrier when system is locked at 240.4 MHz

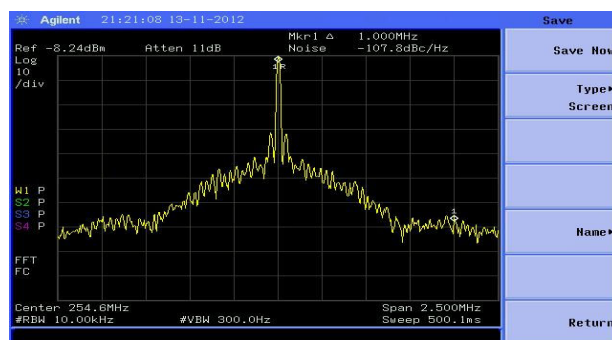


Fig.15: PN at 1 MHz offset from the carrier when system is locked at 254.6 MHz

TABLE 1
THE PN MEASUREMENT SUMMERY OF THE SYSTEM

Locked frequency (MHz)	Output power (dBm)	PN @ 1 KHz (dbc/Hz)	PN @ 100 KHz (dbc/Hz)	PN @ 1 MHz (dbc/Hz)
212.1	-9.88	-71.13	-94.42	-121.8
226.3	-9.52	-48.67	-85.61	-118.4
240.4	-8.94	-58.67	-78.37	-109.3
254.6	-8.26	-53.77	-77.98	-107.8

The measured output power is -9.52 dBm and PN is -48.67 dBc/Hz and -118.4 dBc/Hz respectively at 1 kHz and 1 MHz offset from the carrier when the system is locked at output frequency of 226.3 MHz. The output spectrum for PN is shown in Fig. 11, 12 and 13. Fig. 14, 15, 16 and 17 shows the output PN at 1 KHz and 1 MHz offset from carrier frequency when the system is locked at frequency 240.4 MHz and 254.6 MHz respectively.

VI. CONCLUSION

The lowest recorded PN of the system is -121.8 dBc/Hz at 1 MHz offset from the carrier when it is locked at 212.1 MHz. The VCO produces a wide range of output frequency as the varactor controlled LC circuit is used which changes the equivalent parallel resistance of the LC circuit in a wide range across the full operating voltage of power supply. Measurement shows that the PN is below -100 dBc/Hz @ 1 MHz offset for all the cases. The PN at lower frequencies is better than at higher frequencies. In the PN spectrum, some spurs are observed and these spurs may come from different sources such as PLL reference spurs, some internal or

external signals coming through bias and control interface circuits. It is observed that the spurs are located at the multiple of PFD comparison frequency. Hence it may be due to reference frequency.

The fractional-N frequency PLL can provide small frequency resolution and can improve PN performance compared to integer-N PLL. The PN contributed by the LF can be reduced by optimizing the values of LF components.

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