Design of Sub-1mW Q-Enhancement CMOS LC VCO with Body-Biased Technique

Meng-Ting Hsu, *Member, IEEE*, Tsung-Han Han, Po-Yu Lee

***Abstract* — A new CMOS LC Voltage Controlled Oscillator (VCO) for IEEE 802.11a application with low phase noise and consumed power less than 1mW is presented. This circuit was taped out by TSMC 0.18um 1P6M process. The measured phase noise is -115-88dBc/Hz at 1MHz offset at the operation frequency of 5.815GHz. And the dc core current consumption is 0.71mA at a supply voltage of 1.4 V. Its figure of merit (FOM) is -191dBc/Hz.**

***Index Terms* — Current Reused, Voltage Controlled Oscillator, Q-enhancement, body-biasing, low power, Sub-1mW.**

I. Introduction

Recently, due to the rapid development and maturity of wireless communications and single-chip system integration, the RF block design embedded with digital baseband is more requirement than hybrid circuit for low power design in standard CMOS technology [1,2]. For the transmission of text, audio-visual, multimedia information and data, distance and time constraints can almost be ignored. All this will be due to the wireless communication technology, wireless communication products has also been used in daily life, has brought many conveniences for human life.

With RF circuit design, low power consumption will be a very important consideration, the voltage controlled oscillator (VCO) in a wireless communication also plays a key block [3,4]. In recent years, the technology of current reuse and low voltage supply has been studied for low power consumption, such as less than 1mW voltage-controlled oscillator (Sub-1mW VCOs) [5,6,7].

In this paper, the proposed circuit focuses on the frequency range of IEEE 802.11a. The Section II introduced the proposed voltage-controlled oscillator architecture. And the Section III shows the measured parameter and results. Finally, Section IV is the conclusion.

Manuscript received Feb. 17, 2013; revised April 3, 2013. This work was supported in part by the U.S. Department of Commerce under Grant BS123456.

M.-T. Hsu was with the National Chiao Tung University, Hsin Chu, Taiwan R.O.C.. He is now with the Department and Institute of Electronic Engineering, National Yunlin University of Science and Technology, Douliou, Yunlin 64002, Taiwan R.O.C. (corresponding author to provide phone: (8865)5342601 Ext.4322; fax: (8865)5312063; e-mail: hsumt@yuntech.edu.tw

T.-H. Han was with the Department and Institute of Electronic Engineering National Yunlin University of Science and Technology, Doliou, Yunlin 64002, Taiwan R.O.C. (e-mail: g9913720@yuntech.edu.tw).

Po-Yu Lee is with the Department and Institute of Electronic Engineering National Yunlin University of Science and Technology, Doliou, Yunlin 64002, Taiwan R.O.C. (e-mail: M10013233@yuntech.edu.tw).

II. Circuit Design

The proposed current reused VCO realized by body-biased and Q-enhancement circuit. The schematic of the proposed VCO is shown in Fig.1.

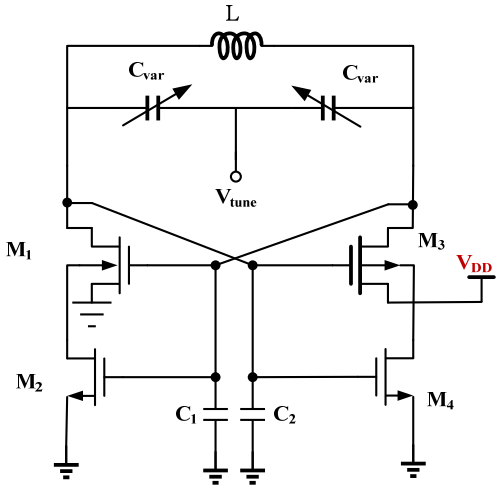

Fig.1 The schematic of the propose VCO

The transistor M_1 and M_3 are cross connection to provide the negative resistance. The body of transistor M_3 and M_1 connect with drain of M_4 and M_2 separately to build up the body-biased structure. Capacitors C_1 and C_2 can improve starting current of oscillation, while reducing the total conductance value to enhance the Q value of the circuit.

III. Measurement Results

The proposed VCO is fabricated by TSMC 0.18um 1P6M CMOS technology. This chip was measured by Agilent E5052A (Signal source analyzer, SSA).By a given supply voltage (1.4v) and voltage modulation level. To retrieve a single-ended output spectrum signal, in order to reduce the impedance mismatch and parasitic effect from bonding wire, this chip is used on-wafer measurements.

Fig.2. shows the die micrograph of the proposed sub-1mW VCO with Q-enhancement and body-biasing circuit, which cost a chip area of 651.81 X 701.98 μm^2 (including the output buffers and output pads). Fig.3.shows the tuning ranges of the oscillation frequency versus varactor controlled voltage (Vtune) which is tuned from -1 to 2V. The proposed VCO operated between 5.082GHz and 5.958GHz, achieved 15.8% and 876MHz tuned-range frequency. The phase noise is -115.883dBc/Hz at 1MHz offset frequency from 5.814GHz in Fig.4.

ISBN: 978-988-19252-8-2
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

The general performance with comparison FOM of VCO is defined as following[4] :

$$\mathrm{FOM} = \mathrm{L}(\Delta f) - 20\log\left(\frac{fo}{\Delta f}\right) + 10\log(P) \qquad (1)$$

where ω_0 is the center frequency, $\Delta\omega$ is the frequency offset, $L\{\Delta\omega\}$ is the phase noise at $\Delta\omega$, P_{dc} is the dc power consumption in 0.99 mW. By the calculation, the figure of merit (FOM) of this proposed VCO is about -191dBc/Hz at the carrier frequency of 5.814 GHz. The performance comparison between reported paper and proposed VCO is shows in Table I.

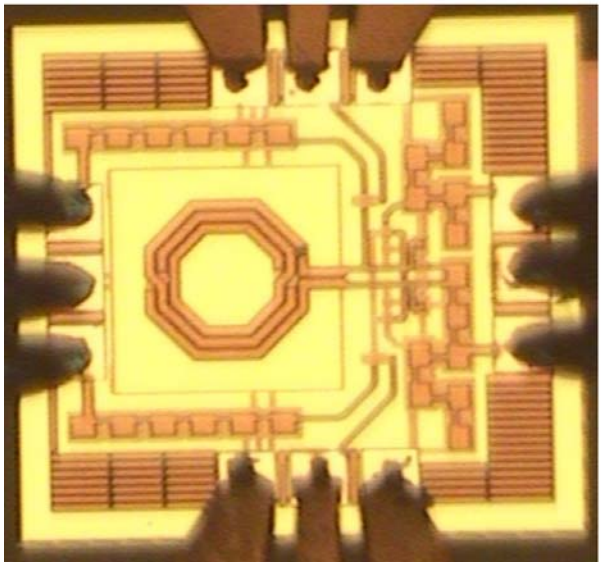

Fig.2 Chip photograph of the proposed VCO.

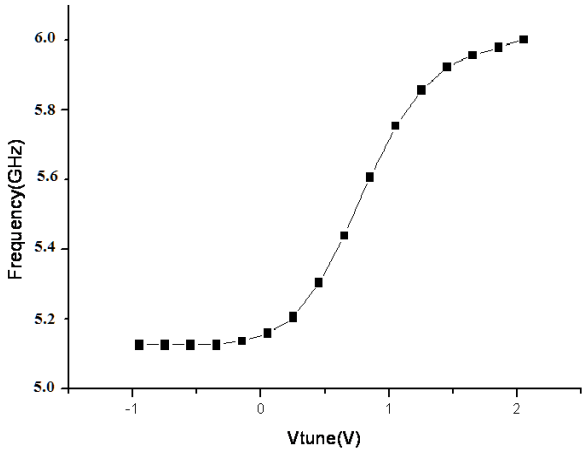

Fig.3 Output oscillation frequency versus control voltage.

IV. Conclusion

In this paper, the new topology with low phase noise and ultra low-power voltage-controlled oscillator is proposed. Measured tuning range is about 15.8% from 5.082GHz to 5.958GHz and power dissipation is 0.99mW. The FOM of the VCO is about -191dBc/Hz.

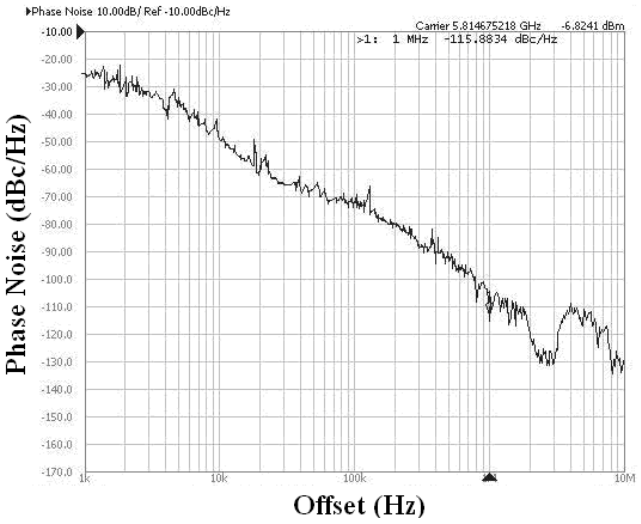

Fig.4 Measured phase noise of proposed VCO

Acknowledgement

The authors would like to thank the Taiwan Semiconductor Manufacture Company (TSMC) and National Chip Implementation Center (CIC) for the wafer fabrications and IC measurement. This project was supported by National Science Council (NSC 100-2221-E-224-072).

References

[1] Y.-H. Chuang, S.-L. Jang, Senior Member, IEEE, S.-H. Lee, R.-H. Yen, and J.-J. Jhao,"5-GHz Low Power Current-Reused Balanced CMOS Differential Armstrong VCOs" IEEE MWCL, Volume: 17, Issue: 2, Page(s): 139 - 141 Feb. 2007

[2] J. Hong, S. Yun, and S. Lee, "360uW/1mW Complementary Cross Coupled Differential Colpitts LC-VCO/QVCO in 0.25um CMOS," IEICE Trans. Electron., vol. E90, no. 12, December 2007.

[3] K. Kwok and H. Luong, "Ultra-low-Voltage high-performance CMOS VCOs using transformer feedback," IEEE J. Solid-State Circuits, vol. 40, no. 3, pp. 652-660, March 2005.

[4] Meng-Ting Hsu, Po-Hung Chen "5GHz low power CMOS LC VCO for IEEE 802.11a application" Microwave Conference Proceedings(APMC), 2011 Asia-Pacific, Dec. 2011

[5] S. Jang, C. Hsue, and C. Chang, "A 0.3 V Cross-Coupled VCO Using Dynamic Threshold MOSFET," IEEE Microw. Wireless Compon. Lett., vol. 20, no. 2, pp. 166-168, March 2010.

[6] S. Jang and C. Lee., "A Low Voltage and Power LC VCO Implemented With Dynamic Threshold Voltage MOSFETS," IEEE Microw. Wireless Compon. Lett., vol. 17, no. 5, pp. 376-378, May 2007.

[7] D. Park and S. Cho, "Design Techniques for a Low-Voltage VCO With Wide Tuning Range and Low Sensitivity To Environmental Variations," IEEE Trans. Microw. Theory Tech., vol. 57, no. 4, pp. 767-774, April 2010

[8] Jaeyoung Jung, Parag Upadyaya, Peng Liu and Deukhyoun Heo "Compact Sub-1mW Low Phase Noise CMOS LC-VCO Based on Power Reduction Technique", IEEE MTT-S International , June 2011

[9] Seok-Ju Yun, So-Bong Shin, Hyung-Chul Choi, Sang-Gug Lee "A 1mW Current-Reuse CMOS Differential LC-VCO with Low Phase Noise," ISSCC 2005, SESSION 29 / RF TECHNIQUES / 29.6

[10] J.-H. Chang and C.-K. Kim, "A symmetrical 6-GHz fully integrated cascode coupling CMOS LC quadrature VCO," IEEE Microw. Wireless Compon. Lett., vol. 15, no. 10, pp. 670-672, Oct.2005.

[11] Y. C. Tsai, Y. S. Shen, and C. F. Jou, "A low-power quadrature VCO using current-reused technique and back-gate coupling," Progress In Electromagnetics Research Symposium pp. 192-195, (2007).

[12] I-Shing Shen, Han-Tzung Ke, and Christina F. Jou," A Ultra Low Power 5.4-GHz Current-Reused VCO with Internal LC Series Resonance in 0.18-μm CMOS technology," Proceedings of Asia-Pacific Microwave Conference 2010,WE3G-26 pp.457-460 (2010)

TABLE I COMPARISON OF LOW POWER VCO PERFORMANCE

	unit	**[4]**	**[9]**	**[10]**	**[11]**	**[12]**	**This work**
Technology	-	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS	**0.18um CMOS**
Frequency	GHz	5.31	2	5.5	5.25	5.4	**5.8**
V_{DD}	V	1.4	1.25	1.8	1.8	1.2	**1.4**
Core Power Diss.	mW	2.5	1	5.76	2.7	0.9	**0.99**
Phase noise @1MHz offset	dBc/Hz	-118	-121	-115	-107	-112.7	**-115.88**
Tuning range	%	14.7	N/A	20	11.4	2.6	**15.8**
FOM	dBc/Hz	-188.6	-189.5	-182	-177	-188	**-191**

ISBN: 978-988-19252-8-2
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)