A 3ps Resolution Time-to-digital Converter in Low-cost FPGA for Laser Rangefinder

M. Maamoun, *Member, IAENG* S. Arami, R. Beguenane, A. Benbelkacem and A. Meraghni

***Abstract*— This paper concerns a new and accurate low cost time-to-digital converter (TDC) for laser rangefinder measurements systems. The proposed TDC system is based on a digital technique, which can be implemented on a single field programmable gate array (FPGA) device or on a single complex programmable logic device (CPLD). In order to achieve the time-to-digital conversion, the system uses a claver method to accumulate a sequence of time-of-flights (TOF) and compares the result with a reference clock time-counter. In this technique, each measurement is based on a automatic calibration, which characterize the reference, followed by time conversion. The automatic calibration method was achieved to obtain an accurate result and to reduce the temperature dependency. To validate the performance of the proposed architecture, FPGA implementation are performed on Xilinx Spartan 3E device. The obtained results show that, the proposed TDC provides a resolution about 3 ps.**

***Index Terms*—Time-to-digital converter (TDC), field programmable gate array (FPGA), laser rangefinder, time-of-flights**

I. Introduction

SHORT time intervals with precise measurements are frequently needed in many radar and laser range-finding applications. The pulsed time-of-flight (TOF) laser range-finding device process is based on the measurement of the time which a laser pulse uses to move from the transmitter to the target and back to the receiver. Using the laser light velocity, the TOF of the laser pulse can be converted to a distance. The TDC performs conversion of a time interval into a digital word, frequently displayed in the decimal form. Originally the name time-to-digital converter (TDC) referred to non-interpolating time-interval meter (TIM) with a short measuring range [1]-[2].

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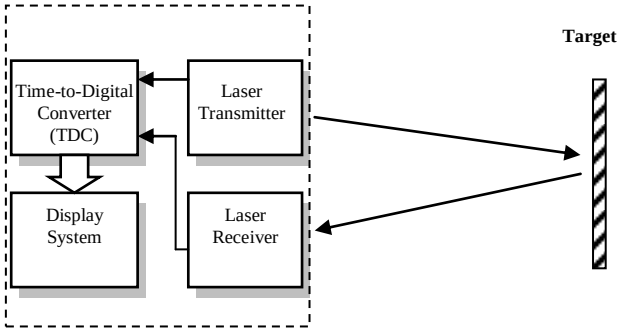

Figure 1. Block diagram of the pulsed time-of-flight laser rangefinder.

The main block diagram of the pulsed TOF laser rangefinder contains a pulsed laser transmitter, laser receiver, time-to-digital converter (TDC) and a display system (figure 1). The accuracy of the measurement result in the pulsed time-of-flight laser rangefinder can be increased further by averaging over several successive measurements [2]-[4]. The time-to-digital conversion can be done by analogue or digital techniques. The analogue conversion is mainly based on time measurement of capacitor charge and discharge. The high resolution is the main advantage of the analogue method. However, the disadvantage is the long conversion time, the poor stability and the non linearity [5]-[8].

The digital method is linear on a large measurement range and the related incertitude can be improved by averaging. The main digital techniques, used in the programmable logic devices (PLDs) implementation, are the modified Vernier methods, time-to-digital conversion using tapped delay lines and inverters lines.

The TDC presented in this work is designed with a new digital approach for radar and laser rangefinders using low-cost FPGA devices. The implementation was achieved in a Xilinx Spartan 3E FPGA and the obtained resolution was 3ps.

II. Programmable Digitale Techniques

A. Vernier Method

The basic principle of the Vernier method uses two startable oscillators with different periods T_1 and T_2 (figure 2). T_1 and T_2 differ only slightly,

where

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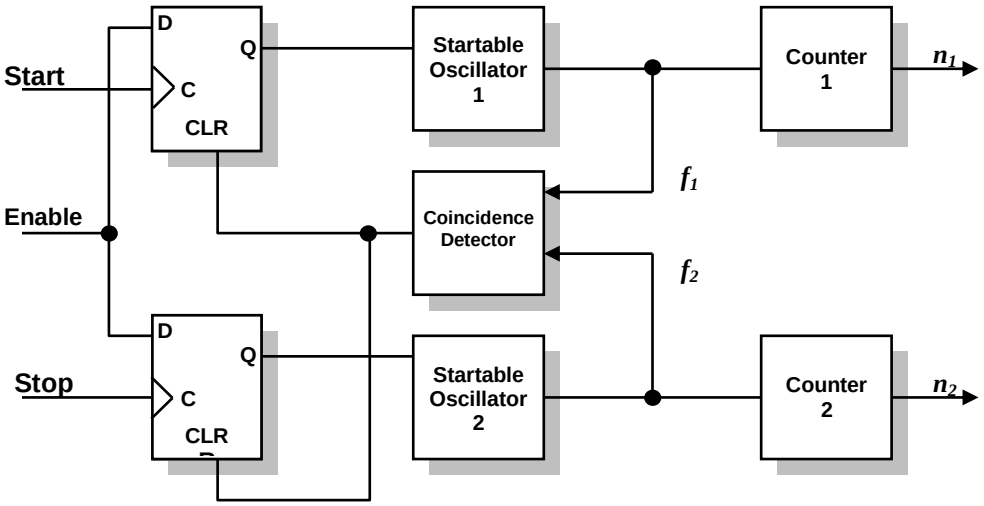

Figure2. Block diagram of the Vernier method

$$f_1 = \frac{1}{T_1} \qquad 2.1$$

and

$$f_2 = \frac{1}{T_2} \qquad 2.2$$

The incremental theoretical resolution is $r = T_1 - T_2$. The startable oscillators are enabled with the active edge of the related input signal, STAR and STOP respectively. The conversion is achieved when coincidence of the active edges of the oscillators' pulses is detected by the coincidence circuit (figure3). Then the oscillators are disabled and the counters store the numbers n_1 and n_2. When the quantization error is ignored, the measurement time interval can be calculated according to equation 2.3.

$$T = (n_1 - 1) \cdot T_1 - (n_2 - 1) \cdot T_2 \qquad 2.3$$

The maximum conversion time (CT) for this method is:

$$\frac{T_1 \cdot T_2}{r}$$

To attain very good resolution using the Vernier method, the startable oscillators should have high accuracy and stability, which presents a considerable implementation challenge [1], [9].

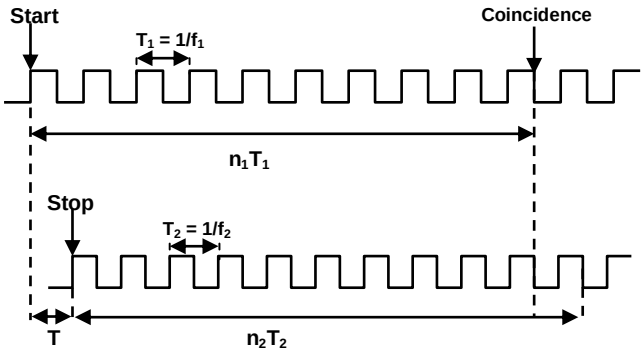

Figure 3. Conversion process of the Vernier method.

B. Time-to-digital Conversion Using Tapped Delay Lines

This method of time interval measurement is based on the use of the tapped delay line. The delay line is made up of number of delay cells with the same theoretical propagation delay τ. The time interval is achieved by sampling the state of the delay line during the time between the START and STOP instances [1]-[2].

There are various configurations used to obtain a tapped delay lines. The figure 4 presents the simplest one. A train of buffers can be used to create a delay line. Each of the buffers should have the same theoretical propagation delay τ. The measurement is achieved by sampling the buffers outputs.

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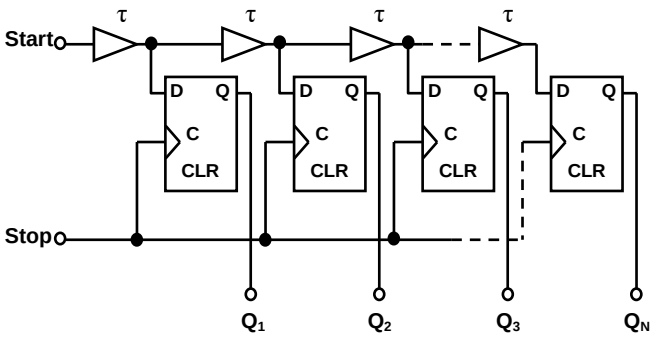

Figure 4. Tapped delay lines using buffers with simultaneous sampling.

The next configuration interchanges the inputs of the clock and data (D). The figure 5 presents the configuration which operates like a multiphase clock.

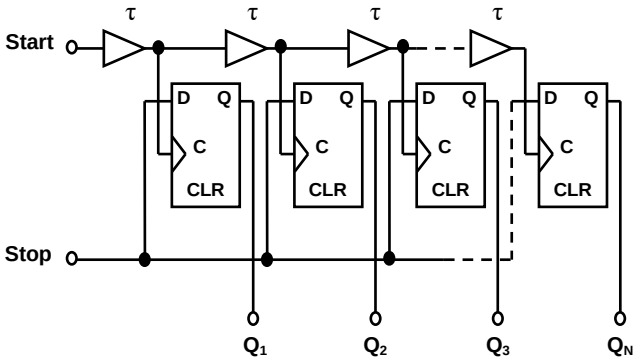

Figure 5. Tapped delay lines using buffers with successive sampling.

C. Inverter Based Time-to-Digital Converter

The resolution and the accuracy of the Time-to-Digital Converters are limited by the technology and delay of the buffers. By changing the buffers by CMOS inverters, the TDC resolution can be multiplied by two. The figure 6 presents the configuration using the inverters instead of buffers

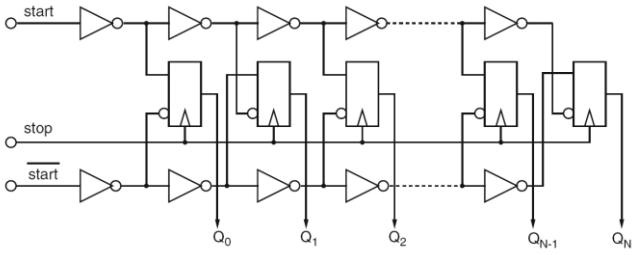

Figure 6. Time-to-digital converter based on inverters

III. The Proposed TDC Architecture

The developed system is based on the digital time interval measurement principle with a new approach. The basic block diagram of the proposed TDC, for Laser rangefinder, is shown in figure 7. This new TDC contains two internal counters, ***A*** and ***B***, driven respectively by a reference crystal-based oscillator and a variable oscillator.

The reference oscillator gives a fixed period T_0 and the variable oscillator gives two different periods, T_1 and T_2. T_1 is the period at the zero distance and T_2 is the period with the time of flight τ, where

$$T_2 = T_1 + \tau \qquad 3.1$$

$$f_1 = \frac{1}{T_1} \qquad 3.2$$

$$f_2 = \frac{1}{T_2} \qquad 3.3$$

$$f_0 = \frac{1}{T_0} \qquad 3.4$$

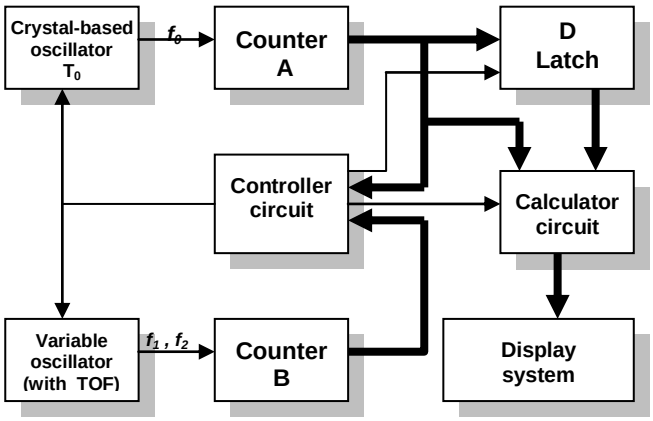

Figure 7. Bock diagram of the proposed TDC

In addition to this, the system contains a controller circuit and a simple calculator circuit. All the digital parts, except the two oscillators, are implemented in a single field programmable gate array (FPGA) device.

IV. Calibration And Time Conversion

In this system, each measurement is based on a calibration followed by time conversion. At the calibration phase, the two counters ***A*** and ***B*** start at the same time. The first one is driven by the T_0 period and the second one is driven by the T_1 period. This phase is completed when the counter ***B*** reaches the number ***N***, which is a programmable number. Then the counter ***A*** is disabled and the ***D*** latch stores the

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number N_1 (figure 8).When the uncertainty of the +/- clock cycle is ignored, the equation 4.1 can be given.

$$N \cdot T_1 = N_1 \cdot T_0 \qquad 4.1$$

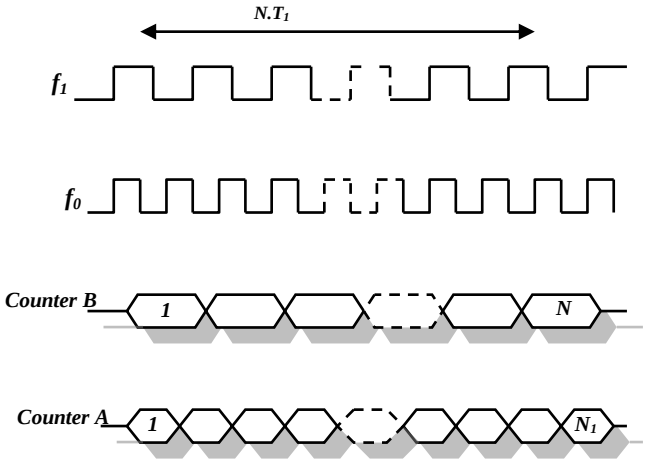

Figure 8. Calibration process.

At the time conversion phase, the two counter start at the same time. However, the T_2 period is used for the counter ***B***. Similar to the first phase, the conversion is completed when the counter ***B*** reaches the number ***N***. Then the counter ***A*** is disabled and the calculator circuit stores the number N_2 and compares it with N_1 to obtain the displayed number (figure 9).

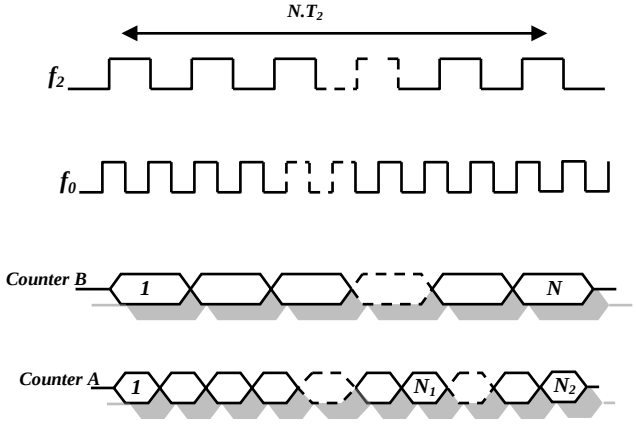

Figure 9. Time conversion process.

When the quantization error is ignored, the equation 4.2 can be given and the measurement time interval can be calculated according to equation 4.3.

$$N \cdot T_2 = N_2 \cdot T_0 \qquad 4.2$$

$$\tau = \frac{(N_2 - N_1).T_0}{N} \qquad 4.3$$

To accomplish good accuracy of measurements using this method, a small T_0 period and a relatively significant ***N*** are preferred.

V. Experimental Results

The proposed TDC was implemented and tested using a Xilinx XC3S500E-5FG320 field programmable gate array (FPGA) Device [10]. A VHDL description was exploited to create the TDC module and the Integrated Software Environment (ISE) has been used for the programmable logic implementation [11]. The FPGA device utilization summary is shown in table 1.

TABLE I
Device Utilization Summary

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	85	9,312	1%
Number of 4 input LUTs	43	9,312	1%
Number of occupied Slices	80	4,656	1%
Number of Slices containing only related logic	80	80	100%
Total Number of 4 input LUTs	127	9,312	1%
Number used as logic	43		
Number used as a route-thru	84		
Number of bonded IOBs	22	232	9%
IOB Flip Flops	16		
Number of BUFGMUXs	3	24	12%

The system accumulates N (N=10000) time-of-flights and compares the result with the fixed clock (50 MHz) counter to achieve the time-to-digital conversion. The figure 10 presents the RTL schematic of the proposed TDC implemented in the Xilinx Spartan 3E FPGA.

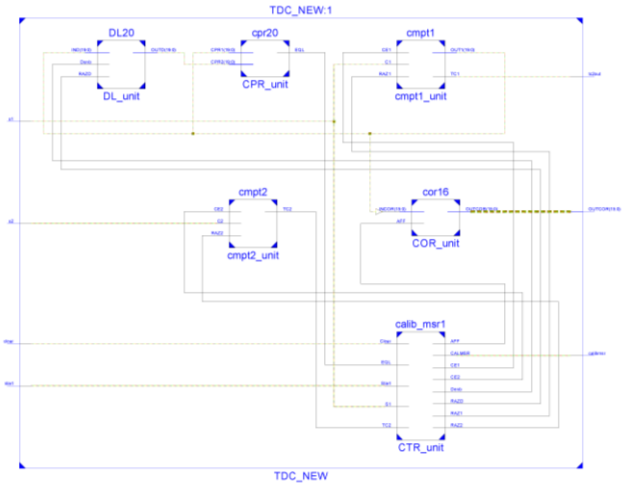

Figure 10. The RTL Schematic of the proposed TDC

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V. Conclusion

We have presented a high-resolution time-to-digital converter using a new programmable digital technique. The described system allows precise measurement at a lower price. The laser rangefinder presents the main target of our system, but it can also be used in other advanced system applications.

The TDC was implemented in a Xilinx Spartan 3E FPGA and tested at the ambient temperature of 20°C. The obtained resolution is 3 ps, which can be improved with averaging a series of measurements.

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