Data Phase Synchronizers of Closed Loop

Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro and Jose P. Carvalho

***Abstract*— This work studies the data phase synchronizers of closed loop or data phase lock loop (DPLL). This synchronizer have all its blocks inside of the loop, for this reason it is called closed loop. The synchronizer is a loop with a phase comparator and VCO (Voltage Controlled Oscillator), that synchronizes the output feedback with the main input data.**

We consider four data synchronizers namely the analog, the hybrid, the combinational and the sequential.

The objective is to study the four synchronizers and to evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal to Noise Ratio).

***Index Terms*—Synchronism, Digital Communications**

I. INTRODUCTION

This work studies the data phase synchronizers of closed loop. It is designed closed loop since all its components are inside the loop [1, 2, 3, 4, 5, 6, 7].

This synchronizer is a data Phase Lock Loop (DPLL) based in a phase comparator and VCO (Voltage Controlled Oscillator) that synchronizes the VCO output clock feedback with the main input data transitions [8, 9, 10, 11, 12].

We consider four synchronizers which are the analog (DPLL_ana), hybrid (DPLL_hib), combinational (DPLL_cmb) and sequential (DPLL_seq) [13, 14, 15].

The data phase synchronizers of closed loop have three blocks which are the input adapter circuit, the clock recovery and the output decision circuit.

The synchronizers DPLL_ana, DPLL_hib, DPLL_cmb need the adapter circuit, but the DPLL_seq synchronizes its VCO output clock directly by the input data transitions.

The adapter, in data transitions, generates a previous pulse of half period T/2, for posterior synchronism The clock recovery recoveries the clock. The decision samples and retimes the data (Fig.1).

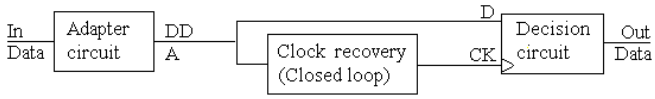

Fig.1 Blocks of the closed loop data phase synchronizer

The DPLL has the phase comparator gain Kf, the loop filter F(s), the VCO gain Ko and Ka is the loop gain factor that controls the root locus and then the loop characteristics.

In the prior and actual art - state, was developed various synchronizers, now it is need to know their performance.

The motivation is to study new synchronizers. This contribution increases the knowledge about synchronizers.

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A. D. Reis is with the University of Beira Interior Covilha and Group of A. P. and Telecommunications, Portugal (e-mail: adreis@ ubi.pt).

J. F. Rocha is with the University of Aveiro and Institute of Telecommunications, Portugal (e-mail: frocha@ ua.pt).

A. S. Gameiro is with the University of Aveiro and Institute of Telecommunications, Portugal (e-mail: amg@ ua.pt).

J. P. Carvalho is with the University of Beira Interior Covilha and Group of A. P. and Telecom., Portugal (e-mail: pacheco@ ubi.pt).

Following, we present the four closed loop data phase synchronizers: analog, hybrid, combinational and sequential.

After, we present the project and tests. Then, we present the results. Finally, we present the conclusions.

II. FOUR SYNCHRONIZERS OF CLOSED LOOP

This synchronizer has all its components inside of the loop. We consider four types namely the analog, the hybrid, the combinational and the sequential [1, 2].

The difference between them is in the phase comparator since the others blocks are equal.

A. Analog closed loop data synchronizer

The analog closed loop synchronizer has a phase comparator based on analog components such as the multiplier. The previous block generates the pulse D (Fig.2).

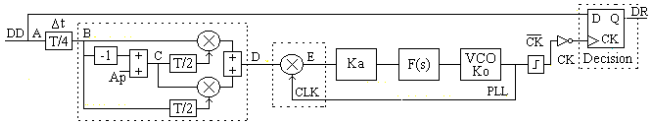

Fig.2 Analog closed loop symbol synchronizer (DPLL-ana)

This DPLL inputs (main input and VCO output feedback) are both analog.

Fig.3 shows the operation mode waveforms of the analog closed loop data synchronizer.

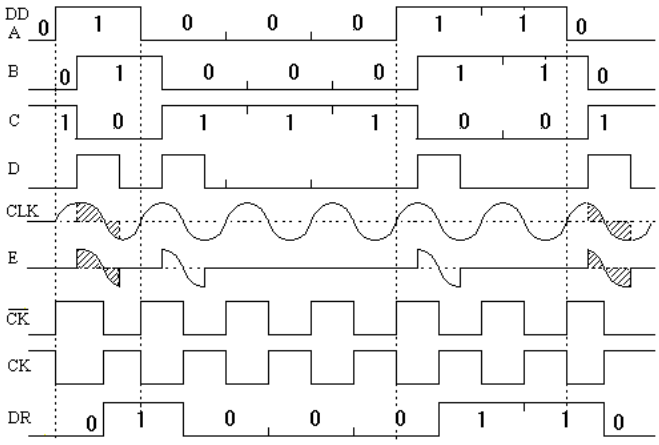

Fig.3 Waveforms of the analog closed loop synchronizer

At the equilibrium point, the positive area is equal to the negative one, so the error pulse average Pe tends to zero.

B. Hybrid closed loop data synchronizer

The hybrid closed loop synchronizer has a phase comparator based on hybrid components such as the real switch. The previous block generates the pulse D (Fig.4).

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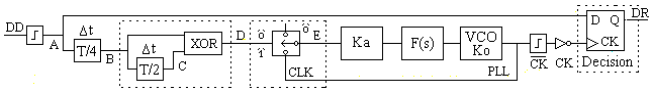

Fig.4 Hybrid closed loop symbol synchronizer (DPLL-hib)

This DPLL main input is digital but the VCO output feedback continues to be analog.

Fig.5 shows the operation mode waveforms of the hybrid closed loop data synchronizer.

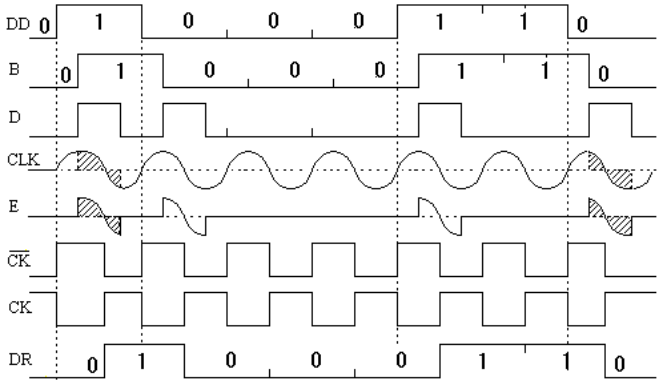

Fig.5 Waveforms of the hybrid closed loop synchronizer

At the equilibrium point, the positive area is equal to the negative one, so the error pulse average Pe tends to zero.

C. Combinational closed loop data synchronizer

The combinational closed loop synchronizer has a phase comparator based on combinational components such as the AND gate. The previous bloc generates the pulse D (Fig.6).

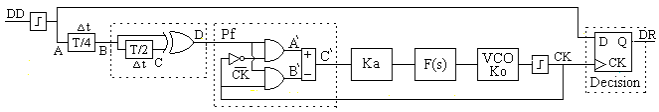

Fig.6 Combinational closed loop data synchronizer (DPLL-cmb)

This DPLL inputs (main input and VCO output feedback) are both digital, but the output is only function of the inputs.

Fig.7 shows the operation mode waveforms of the combinational closed loop data synchronizer.

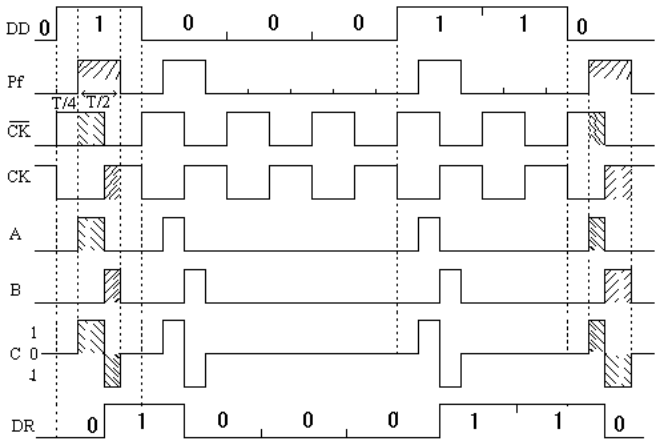

Fig.7 Waveforms of the combinational closed loop synchronizer

At the equilibrium point, the positive area is equal to the negative one, so the error pulse average Pe tends to zero.

D. Sequential closed loop data synchronizer

The sequential closed loop synchronizer has a phase comparator based on sequential components such as the flip flop. It don't needs the previous pulse (Fig.8).

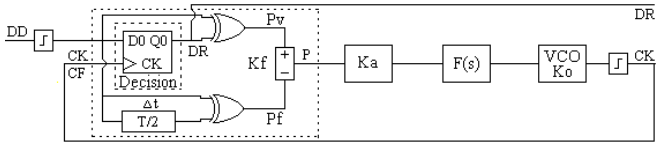

Fig.8 Sequential closed loop data synchronizer (DPLL-seq)

This DPLL inputs (main input and VCO output feedback) are both digital, but the output is function of the inputs and also of the state.

Fig.9 shows the operation mode waveforms of the sequential closed loop data synchronizer.

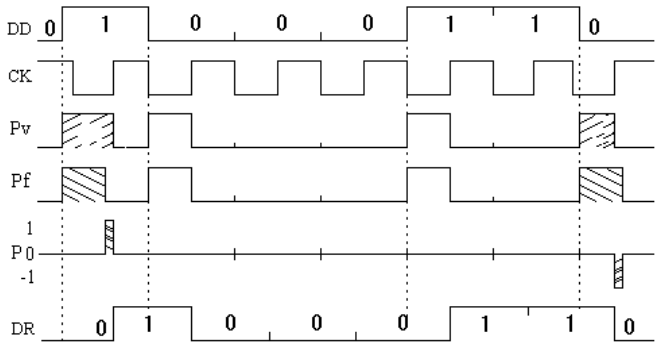

Fig.9 Waveforms of the sequential closed loop synchronizer

In synchronism, the error pulse Pe diminishes its area, tends to zero and disappear at the equilibrium point.

III. PROJECT, TESTS AND RESULTS

We present the project, the tests and the results of the referred synchronizers [5].

A. Project

We project all the synchronizers with the same loop gain conditions to have guaranteed results. The loop gain is Kl = Ka.Kf.Ko, where Kf and Ko are fixed. The Ka is the variable parameter that controls the loop characteristics.

To facilitate the analysis, we use normalized values for the bit rate tx= 1baud, clock frequency f_{CK}=1Hz, extern noise bandwidth Bn=5Hz and loop noise bandwidth Bl=0.02Hz.

We apply a power signal Ps= A^2_{ef} with power noise Pn= No.Bn= $2\sigma n^2.\Delta\tau.Bn$, where σn is the noise standard deviation and $\Delta\tau$ =1/fSampling is the sampling period.

Then, the relation between SNR and noise variance σn^2 is SNR= Ps/Pn= $A^2_{ef}/(No.Bn)= 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$ (1)

Now, for each synchronizer, we must measure the output jitter UIRMS versus the input SNR

- 1st order loop:

The loop filter F(s)=1 has cutoff fc=0.5Hz, which is 25 times greater than Bl= 0.02Hz, eliminates the high frequency but maintains the loop characteristics.

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The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (2)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (3)$$

So, with (Km=1, A=1/2, B_a=1/2, B_h=0.45, Ko=2π) and loop bandwidth Bl=0.02, we obtain respectively the Ka, for analog, hybrid, combinational and sequential synchronizers:

$$Bl=(Ka.Kf.Ko)/4=(Ka.Km.A.B_a.Ko)/4 \rightarrow Ka_a=0.08*2/\pi \quad (4)$$
$$Bl=(Ka.Kf.Ko)/4=(Ka.Km.A.B_h.Ko)/4 \rightarrow Ka_h=0.08*2.2/\pi \quad (5)$$
$$Bl=(Ka.Kf.Ko)/4=(Ka*1/\pi*2\pi)/4 \rightarrow Ka_c=0.04 \quad (6)$$
$$Bl=(Ka.Kf.Ko)/4=(Ka*1/2\pi*2\pi)/4 \rightarrow Ka_s=0.08 \quad (7)$$

For the analog PLL, the jitter is

$$\sigma_\phi^2=Bl.No/Aef^2=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2 \quad (8)$$

For the others PLLs, the jitter formula is more complicated.

- 2nd order loop:
It is not used here, but provides similar results.

B. Tests

Following Fig.10 shows the setup that was used to test the various synchronizers.

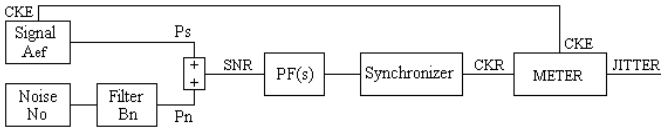

Fig.10 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.11).

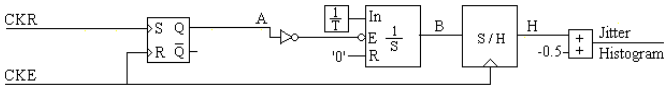

Fig.11 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Fig.12 illustrates the operation of the jitter measurer.

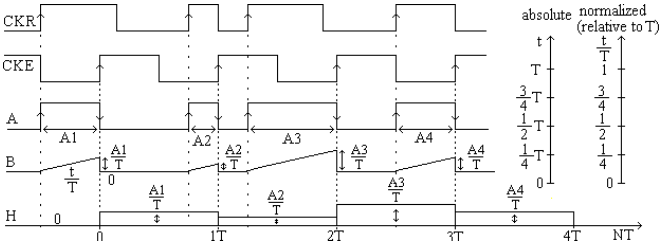

Fig.12 Waveforms at the jitter measurer

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present the results (output jitter UIRMS versus input SNR) for the four closed loop data synchronizers.

Fig.13 shows the jitter - SNR curves of the four synchronizers: analog data synchronizer (DPLL-ana), hybrid data synchronizer (DPLL-hib), combinational data synchronizer (DPLL-cmb) and sequential data synchronizer (DPLL-seq).

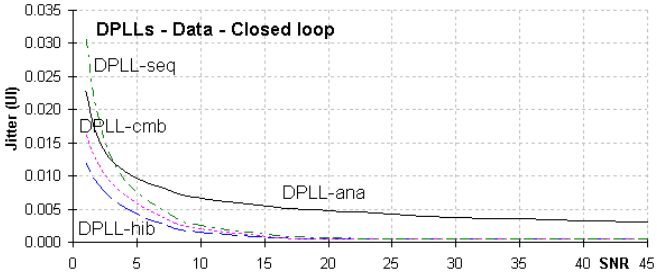

Fig.13 Jitter-SNR curves of the four synchronizers(ana,hib,cmb,seq)

We see, that generally the output jitter UIRMS diminishes almost exponentially with the input SNR increasing.

For high SNR, the synchronizers with input limiter (DPLL-hib, DPLL-cmb, DPLL-seq) are similar and have a slightly advantage over the synchronizer without input limiter (DPLL-ana).

However, for low SNR, the synchronizers without intern memory (DPLL-ana, DPLL-hib, DPLL-cmb) have a slightly advantage over the synchronizer with intern memory (DPLL-seq).

IV. CONCLUSIONS

We studied four data phase synchronizers of closed loop, or data phase lock loop namely the analog (DPLL-ana), the hybrid (DPLL-hib), the combinational (DPLL-cmb) and the sequential (DPLL-seq). Then, we tested their output jitter UIRMS versus input SNR.

We saw that, generally, the output jitter UIRMS diminishes almost exponentially with the input SNR increasing.

We verified that, for high SNR, the synchronizers with input limiter (DPLL-hib, DPLL-cmb, DPLL-seq), have a slightly advantage over the others without input limiter (DPLL-ana). This is comprehensible since the input limiter is a digital components with noise margin what ignores low noise spikes.

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However, for low SNR, the synchronizers with intern memory (DPLL-seq) have a slightly disadvantage relatively to the others synchronizers without intern memory (DPLL-ana, DPLL-hib, DPLL-cmb). This is comprehensible since the intern memory provokes random switching between the memory states, what increments the jitter. This disadvantage can be minimized with a prefilter. Anyway, the intern memory provides important project potentialities.

In the future, we are planning to extend this study to other new synchronizers.

ACKNOWLEDGMENTS

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