Analysis of Die Tilt Effect on the Stress Distribution in a Small Outline Transistor Using Finite Element Method

Jennifer J. Fabular, Hannah Erika R. Ducusin, Manolo G. Mena, Louis Angelo M. Danao, *Member, IAENG*

***Abstract*—The increasing demand for miniaturization and high function integration in today's microelectronic industry poses a big challenge in maintaining the reliability of the package. Majority of the reliability problems can be attributed to thermal and mechanical loadings during manufacturing and assembly process. One of the most common defects originating from these processes is die tilting. In this study, the behavior of a Small Outline Transistor (SOT) when exposed to thermal loads was analyzed using finite element method. This work also investigated the effect of varying solder tilt angle configurations on the stresses experienced by the package. A 5-layer, multi-material, non-symmetric SOT package was modeled in detail to determine the interlayer stresses caused upon by the CTE mismatched between each material. Three different tilt angle configurations for both upper and bottom solder were simulated using ANSYS software. The 3D model of the package was exposed to temperature load of 370˚C and cooled down to room temperature. Material modeling and mesh sensitivity analysis were also conducted in this research to determine the most appropriate material type and mesh density to be used for the simulation. The maximum principal stress distribution, taken after the cooling stage of die bonding process, was used as a criterion to determine the location of the maximum stress on the silicon die. Results from the simulation have shown that the maximum principal stress distribution shifted to the area of thinner solder as the tilt angle is increased. The results holds true for both upper and bottom solder tilting. In addition, the results show that the magnitude of the stresses in the area where the solder becomes the thinnest also increases. This study presents a clear relationship between the thermo-mechanical response of the silicon die and changing die tilt angles. These observations can be helpful in detecting and locating the possible site of failure and can be used to develop more reliable microelectronic packages.**

***Index Terms*— ANSYS, Die Tilt, Small Outline Transistor, Thermo-mechanical**

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I. Introduction

ONE of the most important inventions of the 20th century is the transistor. It revolutionizes the electronic industry. Millions of this device can be found in almost all technological products. They are the fundamental building blocks of modern electronics and affect various fields such as telecommunication, biomedicine, aviation, automotive, manufacturing and virtually every aspect of human life. [1]

As the demand for functionality and miniaturization increase, strength and reliability of the electronic package are utmost importance. During the different stages of production and assembly, the package is exposed to varying temperature and power load. Its subcomponents and layers respond differently to the change in temperature due to the dissimilarity in their material properties. This difference in components' response produces thermal stresses. Reliability and die strength issues often arise from these stresses. Constant exposure to these stresses, and given that defects, such as voids, notch, and micro cracks, are present, will cause die cracking and eventually lead to package failure. Thermo-mechanical reliability is the ability of the package to withstand thermal stresses brought about by varying temperature as it is subjected to thermal loadings. [2]

In a microelectronic industry, thermo-mechanical reliability is of major concern. According to the studies of Zhang, 2003; [2] Zhang et al. 2006b [3] approximately 65% of microelectronic failures are due to or related to thermo-mechanical issues arising from the different stages of manufacturing process.

Early detection of these failures is important for it will not only reduce the cost of production but more importantly, it will save life. There are several ways to test the package for failure. It can be through experiments, analytical methods, or virtual simulations. This research will make use of the latter to simulate the effect of various die tilt angle on the stress distribution on the silicon die. This research also determines the applicability of ANSYS software to simulate thermo-mechanical behaviour of transistor and also identify the specific settings for the mesh density and material model to be implemented in the actual simulation.

II. Methodology

This research is divided into three phases. In Phase I, the capability of the software will be determined. Phase II will give the most appropriate settings for the simulation and Phase III will be the actual modelling and simulation.

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Phase I

In order to verify the capability of ANSYS software to model multilayer packages, the experiment set-up made by Wen and Basaran was recreated using this numerical software. An idealized geometry of the actual microelectronic package was modeled as shown in Figure 1.

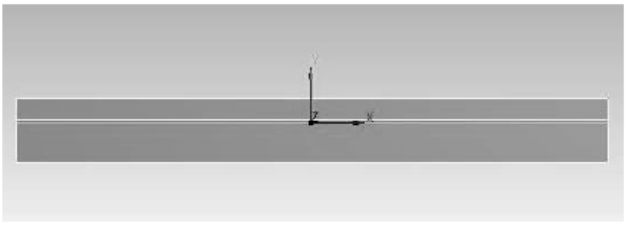

Fig. 1. Idealized geometry model of the microelectronic package.

The model is consists of three layers of different materials. The bottom layer is made up of BT-resin which is connected to the top silicon layer via a thin eutectic Pb/Sn solder. The dimensions and material properties of each layer are summarized in Table 1. A uniform temperature change of 30°C was the thermal load of the package. [4]

TABLE I
MATERIAL PROPERTIES AND DIMENSIONS [4]

	M_1(BT)	M_2(Pb/Sn solder)	M_3(Silicon)
E_1 (GPa)	17.5	24.3	112
E_2 (GPa)	10.4	24.3	148
E_3 (GPa)	4.7	24.3	168
G_{12} (GPa)	3.54	9.2	46.2
G_{13} (GPa)	9.04	9.2	33.2
G_{23} (GPa)	1.58	9.2	51.7
v_{12}	0.32	0.32	0.28
v_{13}	0.32	0.32	0.28
v_{23}	0.32	0.32	0.28
α_1 (e-6/°C)	16	24.7	3
α_2 (e-6/°C)	16	24.7	3
α_3 (e-6/°C)	16	24.7	3
h (mm)	1.32	0.096	0.714
$2L$ (mm)		20.5	

The assembly was modelled using finite element method in ANSYS workbench. It was meshed using quadrilateral elements. The mesh generated a total of 123,000 elements which gave fairly accurate results. All corners of the assembly were constrained to move in the y-direction to avoid rigid body motion. Figure 2 shows the applied boundary conditions for each vertex.

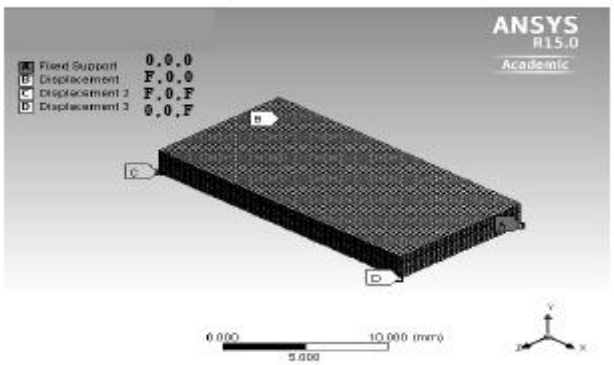

Fig. 2. Boundary conditions applied to the idealized package.

Finite element simulation showed that the package deformed shape is concave upwards. This is because the coefficient of thermal expansion of the bottom layer is higher than that of the top layer. Figure 3 shows the deformed shape of the package.

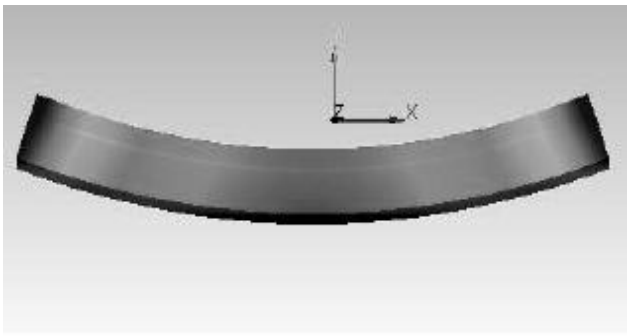

Fig. 3. Deformed shape by finite element analysis.

The maximum deflection computed from the FEA simulation was 5.49x10-3 mm. Basaran et al. [5] also conducted an FEA simulation and their results showed that the maximum deflection of the package was 7.85x10-3 mm.

Comparing the results obtained from the experiment and the two FEA simulations, it can be observed that the experimental data and the FEA results of this research are in good correlation with each other as shown in Figure 4. The normalized error between the experimental data and the FEA simulation in the current study is 11.87%. This value is closer to the test data as compared to the values obtained from FEA results of Basaran et al. as shown in Table 2.

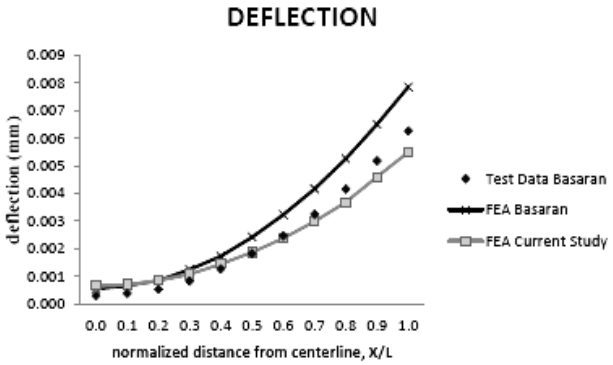

Fig. 4. Deflection results for FEA and experimental data (ΔT=10°C).

TABLE II
COMPARISON OF EXPERIMENTAL AND FEA RESULTS

	Maximum Deflection	Normalized Error
Experimental Data (Basaran)	$6.23x10^{-3}$	0
FEA (Basaran)	$7.85x10^{-3}$	26%
FEA (Current Study)	$5.49x10^{-3}$	11.87%

Phase II

A. Material Modelling

According to Basaran and Zhao [5] the type of model used in characterizing a material greatly affects the results of an analysis. In this study, the effect of using elasto-viscoplastic model to characterize the materials versus elastic model was examined. Table 3 and Table 4 shows the detailed material characteristics of the SOT package used.

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TABLE III
ELASTIC PROPERTIES OF SOT PACKAGE

Material	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/C)
Silicon Die	169.00	0.23	3.0 (100)
Clip	120.00	0.35	17.7
Leadframe	120.00	0.35	17.7
Solder	26.00 (-65 C)	0.4	13.3(-65 C)
	16.93 (260 C)		9.2 (150 C)

TABLE IV
ANAND CONSTANTS FOR SnPb SOLDER

Parameter Symbol	Units	Value
s_0	MPa	1.00
Q/R	1/K	7416
A	s^{-1}	2000
ξ	-	6.0E-4
m	-	0.303
h_0	MPa	1.0E-09
S	MPa	1.00
n	-	1.0E-09
a	-	1.00

The SOT package used in this study is a multilayer structure consisting of different materials, namely silicon, solder, and metal alloy. Figure 5 shows the geometry of the model. It has 4.13mm x 3.53mm silicon die bonded to a 4.5mm x 4.68mm copper leadframe using a 10µm thick solder. The copper clip is attached on top of the die using 75µm solder.

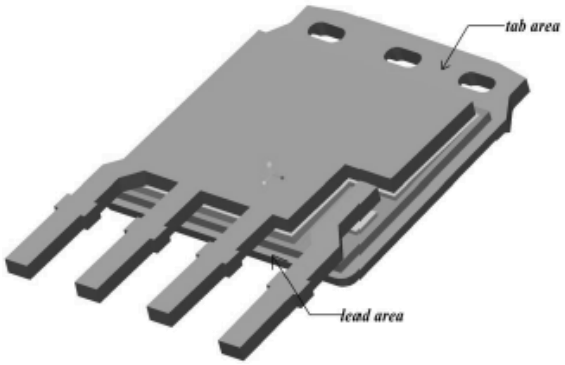

Fig. 5. Actual clip and die assembly.

Maximum principal stress and time to finish the simulation were the parameters being checked. Table 4.3 shows the result of the simulation. It can be observed that there is no significant difference in the maximum principal stress between the two models. However, it took 120 minutes for the elastic-viscoplastic model to finish the simulation while the elastic model took only 20 minutes. Based from the gathered results, the author decided to use the elastic model to characterize the materials.

TABLE V
COMPARISON BETWEEN ELASTIC AND VISCOPLASTIC MODEL

Model	Maximum Principal Stress (MPa)	Time to Finish the Simulation (min)
Elastic Model	1037.8	20
Viscoplastic Model	1037.8	120

B. Mesh Sensitivity Analysis

In finite element simulation, proper meshing not only gives accurate results but also cuts the simulation time and storage requirement to a manageable limit. For this study, a global mesh sensitivity analysis was done to the non-tilt die configuration of the whole geometry.

For the global mesh refinement, all sizing parameters were set to medium. A local body sizing was applied to the silicon layer. Three different meshes generated were tested to check the convergence of the results. The first mesh had 60000 elements, which is relatively coarse. The second one had 120000 elements and the last has 230000. Table 6 shows the summary of the total number of elements and the maximum principal stress produced in the mesh density study using no tilt configuration. As one can observe, for the simulation that used viscoplastic model, the result is not mesh sensitive while that of elastic varies with mesh density.

From the said table, it is observed that the results for the coarse mesh is almost the same for elastic and viscoplastic model and simulation using elastic model is 80% faster compared to viscoplastic. Thus, in this research, the elastic model of material with relatively coarse mesh was used in the actual simulation.

Phase III

The material model and mesh density obtained in the previous phase were used in the actual simulation. Thermal loads and boundary conditions were also applied.

In a normal flow of an assembly process, the SOT package would be subjected to a series of thermal processes such as in die and clip attach, molding, post-mold curing, reflow temperature cycling, etc. [6] During this processes, thermal stresses are accumulated due to the differences in coefficient of thermal expansion of each component layer. According to the study of Y. Shi et al. [7] residual stresses develop during the cooling process. In this research, only the cooling process after die and clip attach was simulated.

TABLE VI
MESH SENSITIVITY RESULTS FOR NO TILT CONFIGURATIONS

Total No. of Elements	Max. Principal Stress (MPa) Elastic	Location	Max. Principal Stress (MPa) Viscoplastic	Location
60,671	1022.9	Solder1	1022.9	Clip
123,133	1118.9	Solder1	1023.0	Clip
228,368	1307.6	Solder1	1023.6	Clip

Temperature change from this cooling process is the only loading parameter applied to this simulation. The SOT package was exposed to a temperature of 370°C, which is the die and clip attach reflow temperature, and was cooled down to room temperature of 25°C. At the start of the simulation, the package was assumed to be in a stress free situation. Usually, the stress free temperature is set at the melting point of the die attach material.

To avoid the rigid body motion, the neutral point in the package (all DOF are constrained to zero) was set to be the right most bottom corner of the copper leadframe. On the other hand, the other corners were constrained to move in y-z, x-z, and y directions. These boundary conditions are shown in Figure 7.

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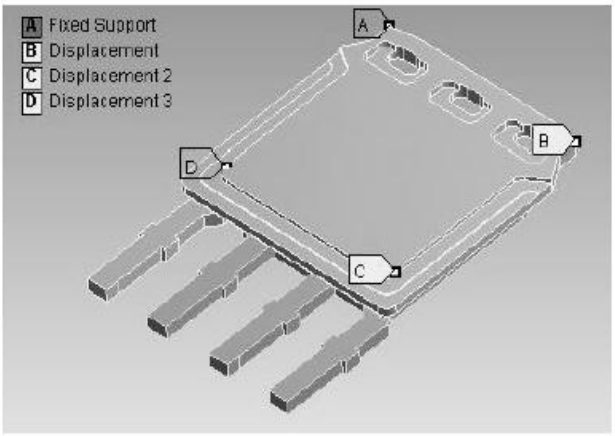


Fig. 7. Boundary conditions applied in a clip assembly.

Die Tilt Simulation

After ensuring that appropriate models were used and proper loading conditions were applied, die tilt simulation was conducted. Both the upper and bottom solder tilt were modeled and simulated in this study. Die tilt here was defined by the vertical displacement of the silicon die and is measured along the lead area. The bottom solder is designated as the layer between the leadframe and the silicon die. The bottom solder measures 10µm. For this simulation, three tilting cases were tested. The tilt was oriented in such a way that the thinner side is along the tab area. The maximum measured tilt angle was 0.32° which corresponds to a die's vertical displacement of 20µm. All models were subjected to the same mesh set-up, boundary conditions and temperature loading. The different tilt variations are shown in figure 8.

On the other hand, the layer between the silicon die and the copper clip is what referred here as upper solder. Only the solder below the larger clip was tilted. This set-up is shown in Figure 9. Same with the bottom solder, three tilting cases were also tested. The first case is a no tilt case. In this case, the solder is uniformly distributed and the top surface is flat. The third case is the worst case. Here, one edge of the clip is touching the silicon die surface. For the upper solder, the maximum tilt angle is around 2.57°. Note that in this simulation, it was the clip's angle that varies. The silicon die remains flat for all five cases. The mesh set-up and boundary conditions applied to the bottom solder were also used in this simulation.

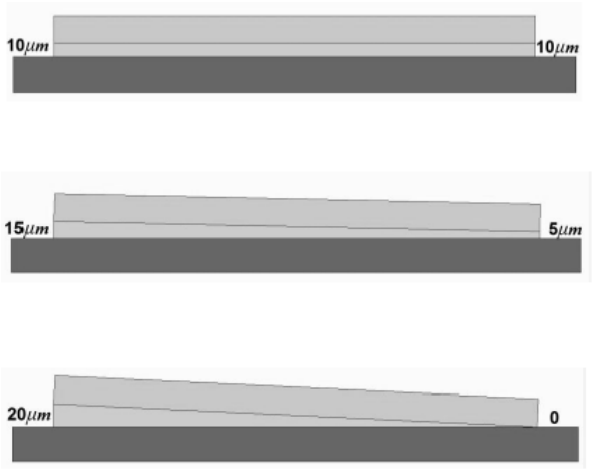


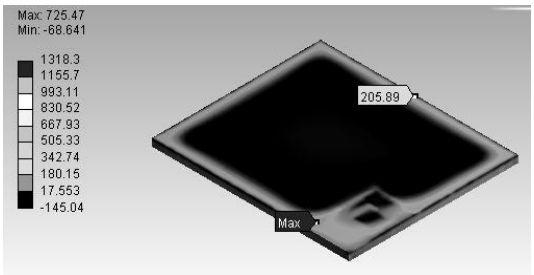
Fig. 8. Bottom solder tilt angle variations.

Fig. 9. Upper solder tilt angle variations.

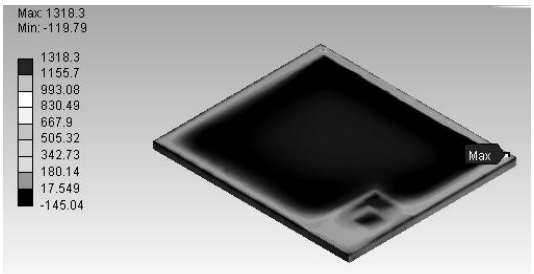
III. Results and Discussions

After running a simulation, a lot of information could be gained from the results. To avoid confusion, it is important to choose only those information that would clarify the problem at hand. For this study, the maximum principal stress was used as failure criterion. This criterion is often used to check whether a brittle material will fracture or not when subjected to severe loadings. Since the focus of this study is on the die behavior, which is a brittle material, the result obtained using this failure criterion will give an insight on how the die is affected by the changing parameter.

Figure 10 and Figure 11 show the maximum principal stress distribution on the die. For the upper solder configuration, the maximum stress is located on the interface between the silicon die and the upper solder. As the tilt increases, the maximum principal stress distribution shifted to the thinner side. It can also be observed that the stresses in the die where the thinner side of the solder is located, increases with increasing tilt angle.



a.



b.

Fig. 10. Maximum principal stress on the die due to upper solder tilting: a) no tilt, b) worst tilt.

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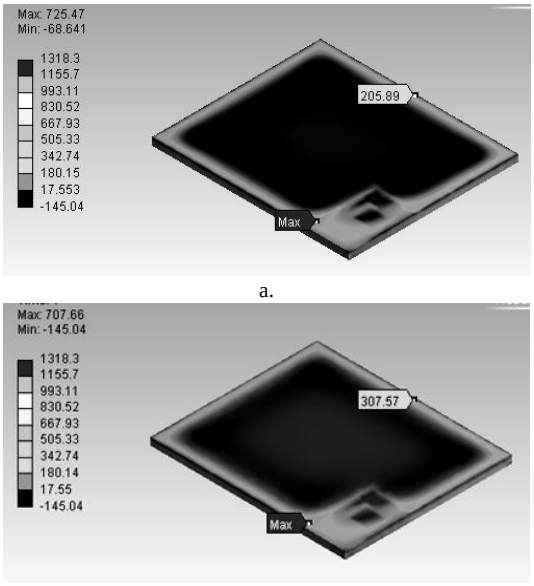

Fig. 11. Maximum principal stress on the die due to bottom solder tilting: a) no tilt, b) worst tilt.

For the bottom solder tilt, it was observed that as the tilt angle increases, the maximum principal stress on the thicker side of the die decreases. However, stresses on the side of the die (tab area) started to increase. The maximum principal stress in the die is 725.47 MPa on no tilt case and 707.66 MPa for worst case tilt. While for the upper solder tilt, the maximum stress is 1318.3 MPa and is located on the corner where the solder is the thinnest. For bottom solder tilt, the maximum principal stress is located on the intersection of the upper solder and the die. This could be attributed to the geometrical discontinuity between the upper solder and the die.

The maximum compressive stress on the die was also determined after the cool down process. It was found out that the maximum compressive stress increase with increasing tilt angle for both upper and bottom solder.

IV. Conclusion

In this study, thermo-mechanical simulations, using ANSYS software, were conducted for multilayer SOT package to assess its thermal behavior. From the initial analysis, the software was proven to be capable of modelling multilayer packages. The mesh settings and material model applied in the simulation were sufficient and provide a good representation of the behavior of the actual model.

Based from the simulation results, it can be concluded that die tilting has significant influence on the thermo-mechanical behavior of the SOT package. Die tilting can be used as a guide in determining the most stressed area in the package when exposed to different loading conditions.

For future studies, it is recommended to look into the effect of different tilt angle configuration to the possibility of crack propagation and to consider three-dimensional tilt.

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