Estimation of Error in Nonlinearity in ADC using Standard Histogram Technique

R. S. Gamad and D. K. Mishra

Abstract—**This paper reports estimation of error in nonlinearity in ADC using histogram test. Also variance estimation in nonlinearity is done. Error determination in Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) of an ADC is done by taking deviation of estimate value from actual value. Variance in estimated INL and DNL is determined to check the usefulness of basic histogram test algorithm. Arbitrary error is introduced in ideal simulated ADC transfer characteristics and full scale simulated sine wave is applied to ADC for estimation of transition errors and nonlinearity errors. Simulation results for 5 bit ADC are presented which show effectiveness of the proposed method.**

***Index Terms*— Nonlinearity, Transfer Characteristics, Code bin width, Error estimation, Transition levels.**

I. Introduction

Digital systems outperform analog systems in many applications. Most of the time signals are available in analog domain and need arises to convert them in digital using ADC. Various applications of ADC are data acquisition systems, measurement systems, and digital communication systems. Such a wide spread usage confers great importance to the testing activities, which now a days largely contributed to the production costs of integrated circuit devices. In this regards, it should be observed that the ADC test duration and costs tend to grow significantly for high resolution ADCs [1]. Hence, choosing an efficient test and improving the associated performance may significantly reduce the industrial cost of an ADC manufacturing process. ADC is usually characterized by its figures of merit like Effective Number of Bits (ENOB), Signal to Noise and Distortion ratio (SINAD), DNL and INL [2]. The histogram test is extensively used in the area of ADC testing to obtain its transfer function and consequently several parameters of interest namely, INL, DNL, ENOB, gain error and offset error, among others. All these parameters attest the capacity of the ADC to perform its intended function. ADCs are rarely used alone, but are often included in more elaborate systems. The performance of the ADCs will affect the performance of the system where it is included and the precision with which the ADC parameters are known is necessary to compute the precision of the final result of the system using it [3]. Standard histogram technique is popular method which estimates DNL and INL related to each transition voltages of an ADC [4]. Earlier work on ADC testing using histogram technique has been reported for determination of DNL, INL, gain error, offset error and ENOB [5]–[10]. Recently work on estimation of errors in code transition levels and computation of variance in gain and offset has been published [3] [4] and performance of ADC parameters has been evaluated [12]. In this paper our contribution is in estimation of error in DNL and INL in addition to variance determination in both type of non-linearity. Section II presents brief review of earlier work using histogram technique. Mathematical formulae for estimation of error in nonlinearity and variance in DNL and INL are presented in section III. Simulation results and discussion are reported in section IV. Conclusions are presented in section V.

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II. Earlier work based on histogram technique

A sinusoidal stimulus signal with frequency (f), amplitude (A), and offset (O) is applied to the ADC under test and predefined number of samples, M, with sampling frequency (fs) are acquired. The expression used to estimate the transition levels, T[k], of an ADC with N bits is given as [3] [7].

$$\hat{T}[k+1] = O - A.cos\left(\pi \frac{C_k}{M}\right), \text{K=1, 2… } 2^{N-1} \qquad (1)$$

Where $C_k = \sum_{i=0}^{k-1} h[i]$

$h[i]$ = The total number of samples received in code bin I

The number of counts in the cumulative histogram is a random variable and it depends on real transition voltages ‘T’ and number of samples ‘M’. The normalized transition voltages ‘U’ can be expressed as:

$$U[k] = \frac{T[k] - O}{A} \quad (2)$$

For any particular values for the gain and the offset, the DNL and INL can be estimated as follows:

$$DNL = \frac{GW[K] - Q}{Q} \quad (3)$$

$$INL = \frac{[K-1].Q + T[1] - T[K]}{Q} \quad (4)$$

Where, G = gain, W[k] = K^{th} code bin width,
Q = ideal code bin width

III. ESTIMATION OF NON LINEARITY AND VARIANCE

DNL is deviation of actual code bin width from ideal code bin width and INL is maximum deviation of actual transfer characteristics from ideal or best fit transfer characteristics. Estimation of DNL and INL is given as below. In all formulae this symbol ^ on top of parameter indicates estimate value.

$$\hat{DNL} = \frac{\hat{G}\hat{W}[K] - \hat{Q}}{\hat{Q}} \quad (5)$$

$$\text{Or, } \hat{DNL} = \left[\left\{ \frac{\hat{G}\hat{W}[K]}{\hat{Q}} \right\} - 1 \right] \quad (6)$$

Finally estimate of DNL can be expressed as:

$$\hat{DNL} = \left[\left\{ \frac{\hat{G}\left(\hat{W}[K]\right)\left(2^N - 2\right)}{\hat{L} - \hat{F}} \right\} - 1 \right] \quad (7)$$

Similarly estimate of INL can be expressed as:

$$\hat{INL} = \frac{\left\{\hat{G}.\hat{T}[K] + \hat{O}\right\} - T_K^{ideal}}{Q} \quad (8)$$

Or,

$$\hat{INL} = \frac{\left\{\left(\hat{G}.\hat{T}[K] + \hat{O}\right)\left(2^N - 2\right)\right\} - T_K^{ideal}}{\hat{L} - \hat{F}} \quad (9)$$

Where from [2] [3]

$$\hat{G} = \frac{L_{ideal} - F_{ideal}}{\hat{L} - \hat{F}}$$

Where L = Last transition, F = First transition and O = Offset

$$\hat{Q} = \frac{\hat{V}}{2^N - 2}$$

$$\hat{V} = T\left[2^N - 1\right] - T[1]$$

$$\hat{V} = \hat{L} - \hat{F}$$

Therefore,

$$\hat{Q} = \frac{\hat{L} - \hat{F}}{2^N - 2} \text{ and } \hat{W}[K] = \hat{T}\left[K+1\right] - \hat{T}\left[K\right].$$

A. Error Estimation in DNL and INL

From equation (3) and (7) error in estimate of DNL can be written as:

$$e_{\hat{DNL}} = DNL_{est} - DNL$$

$$e_{\hat{DNL}} = \frac{\left(2^N - 2\right)\left\{\hat{G}\hat{W}[K]\right\}}{\hat{L} - \hat{F}} - W[K] \quad (10)$$

From equation (4) and (9) error in estimate of INL can be given as:

$$e_{\hat{INL}} = INL_{est} - INL$$

Alternately,

$$e_{\hat{INL}} = \frac{\left\{\left(\hat{G}.\hat{T}[K] + \hat{O}\right)\left(2^N - 2\right)\right\} - T_K^{ideal}}{\hat{L} - \hat{F}} - \frac{T[1] - T[K]}{Q} + [K-1] \quad (11)$$

B. Variance in estimate of DNL and INL

The variance in the estimate of DNL can be approximated as below [3] [11].

$$\sigma^2_{\hat{DNL}} \approx \left(\frac{\partial \hat{DNL}}{\partial \hat{F}} \right)_{\hat{F} = \mu_{\hat{F}}} \sigma^2_{\hat{F}} + \left(\frac{\partial \hat{DNL}}{\partial \hat{L}} \right)_{\hat{L} = \mu_{\hat{L}}} \sigma^2_{\hat{L}} \quad (12)$$

Which in this case leads to:

$$\sigma^2_{\hat{DNL}} \approx \frac{\left(\hat{G}\hat{W}[K]\left(2^N-2\right)\right)^2}{\left(\mu_{\hat{L}}-\mu_{\hat{F}}\right)^4}\sigma^2_{\hat{F}} + \frac{\left(\hat{G}\hat{W}[K]\left(2^N-2\right)\right)^2}{\left(\mu_{\hat{L}}-\mu_{\hat{F}}\right)^4}\sigma^2_{\hat{L}} \tag{13}$$

Or,

$$\sigma^2_{\hat{DNL}} \approx \frac{\left(\hat{G}\hat{W}[K]\left(2^N-2\right)\right)^2}{\left(\mu_{\hat{L}}-\mu_{\hat{F}}\right)^4}\left(\sigma^2_{\hat{F}}+\sigma^2_{\hat{L}}\right) \tag{14}$$

Approximating the mean of the estimated values of $\hat{F}$ and $\hat{L}$ by their ideal value leads to:

$$\sigma^2_{\hat{DNL}} \approx \frac{\left(\hat{G}\hat{W}[K]\left(2^N-2\right)\right)^2}{4\left(FS-Q\right)^4}\left(\sigma^2_{\hat{F}}+\sigma^2_{\hat{L}}\right) \tag{15}$$

Similarly the variance in INL can be derived as:

$$\sigma^2_{INL_{est}} = \left(\frac{\partial_{INL_{est}}}{\partial\hat{F}}\right)_{\hat{F}=\mu_{\hat{F}}}\sigma^2_{\hat{F}} + \left(\frac{\partial_{INL_{est}}}{\partial\hat{L}}\right)_{\hat{L}=\mu_{\hat{L}}}\sigma^2_{\hat{L}} \tag{16}$$

Which in this case leads to:

$$\sigma^2_{INL_{est}} \approx \frac{\left(\left\{\hat{G}T[K]+\hat{O}\right\}-T_K^{ideal}\right)^2\left(2^N-2\right)^2}{\left(\mu_{\hat{L}}-\mu_{\hat{F}}\right)^4}\sigma^2_{\hat{F}} + \frac{\left(\left\{\hat{G}T[K]+\hat{O}\right\}-T_K^{ideal}\right)^2\left(2^N-2\right)^2}{\left(\mu_{\hat{L}}-\mu_{\hat{F}}\right)^4}\sigma^2_{\hat{L}} \tag{17}$$

Approximating the mean of the estimated values of $\hat{F}$ and $\hat{L}$ by their ideal values leads to:

$$\sigma^2_{INL_{est}} \approx \frac{\left(\left\{\hat{G}.\hat{T}[K]+\hat{O}\right\}-T_K^{ideal}\right)^2\left(2^N-2\right)^2}{4\left(FS-Q\right)^4}\left(\sigma^2_{\hat{F}}+\sigma^2_{\hat{L}}\right) \tag{18}$$

IV. RESULTS AND DISCUSSION

Five bit ideal ADC is simulated and arbitrarily nonlinearity error is introduced in transfer characteristics of the ADC. Simulated full scale sine wave with 0.98 MHz frequency with slight overdrive is applied to the ADC and large number of samples at 5 MHz sampling frequency is collected. In first case arbitrarily DNL error [9] is introduced and estimation of DNL is done. Error in estimate of DNL is computed and is shown in Fig. 1. The error in DNL estimate is plotted with respect to ADC code. The variation in DNL is observed with maximum value of approximately of 0.4 and minimum value of 0.2. Similarly arbitrarily INL error [9] is introduced in 5 bit ADC. Error estimation in INL is done and is shown in Fig. 2. The variation in error in INL estimation is from 0.35 to less than -0.3. In addition to error estimation we have also carried out computation of variance in DNL estimation and INL estimation. Fig. 3 shows variance in DNL estimation as a function of normalized transition voltage and ADC code while Fig. 4 shows variance in INL estimation. From these two figures it is observed that variance in both DNL and INL increases with normalized transition voltage and with higher ADC codes up to a particular value after that variance reduces with increase in normalized voltage and it becomes nearly constant at lower ADC code. In this paper results for 5 bit ADC are presented. Same test technique can be applied for testing higher resolution ADC. Simulation results obtained are useful in estimating errors in different nonlinearity in high speed ADC.

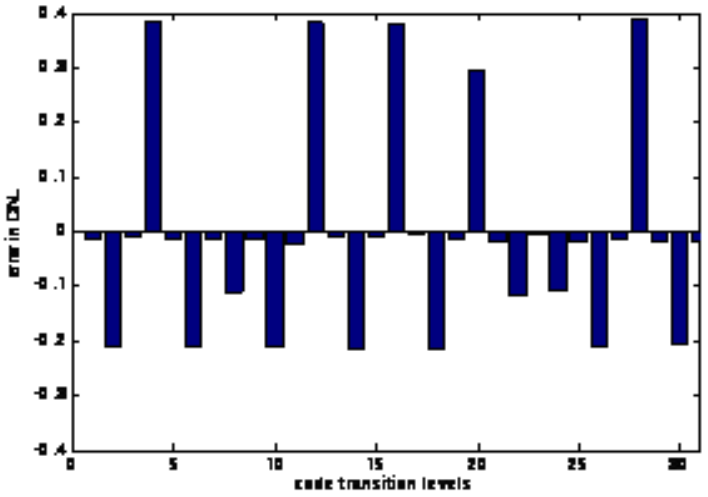

Fig 1. Error in 5 bit ADC DNL estimation

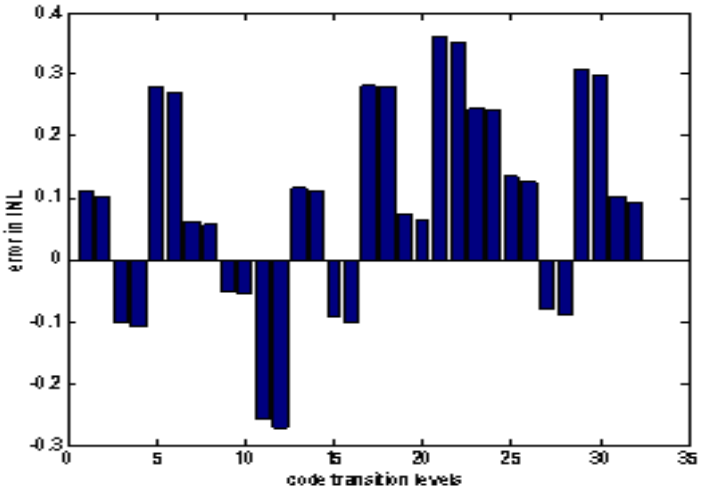

Fig 2. Error in 5 bit ADC INL estimation

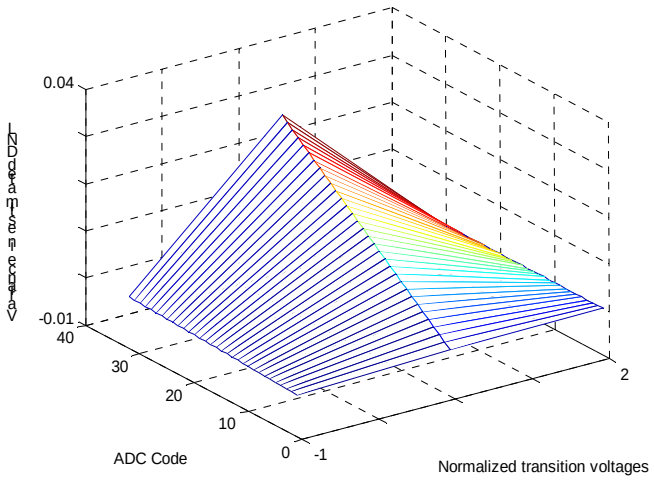

Fig. 3. Variance in 5 bit ADC DNL estimation

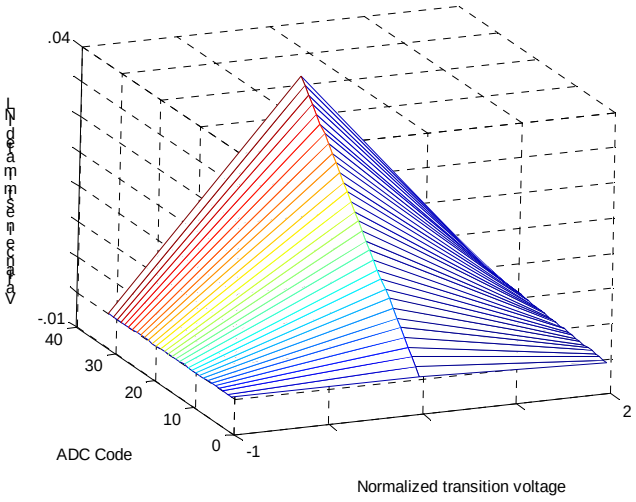

Fig 4. Variance in 5 bit ADC INL estimation

V. CONCLUSIONS

In this work a detailed study of INL and DNL estimate and their errors is done for 5 bit ADC. Variance for both INL and DNL estimate shows effectiveness of algorithm for testing ADC using histogram technique. Ideal ADC transfer characteristic simulation is done and arbitrarily nonlinearity error is introduced. Extensive test and evaluation is done by doing simulation of 5 bit ADC characteristics. We have incorporated estimation of error in DNL, INL and variance in estimated DNL and variance in estimated INL. This work is an extension of earlier published work on ADC testing using histogram technique.

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REFERENCES

[1] P. D. Capofreddi, B. A. Wooley, "The use of linear models in A/D converter Testing" IEEE Transaction on circuits and systems –I, vol. 44, No. 12, Dec.1997, pp. 1105- 1113.

[2] IEEE std- 1057-1994, "IEEE standard for digitizing waveform recorders".

[3] F. Correa Algria and A. Cruz Serra, "Standared Histogram Test Precision of ADC gain and offset error estimation" IEEE transaction on instrumentation and measurement, vol 56, No 5, October, 2007.

[4] F. Correa Algeria and A. Cruz Serra, "Error in the estimation of transition voltages with the standard histogram test ADCs" ELSEVIER international Journal on Measurement, 35 (2004) pp 389-397. 2004.

[5] IEEE std. -2000 "IEEE standard for terminology and test methods for analog to digital converters".

[6] Jerome Blair, "Histogram measurement of ADC nonlinearity using sine waves", IEEE transaction on instrumentation and measurement, Vol 43, no 3, PP 378-383, June 1994.

[7] D. K. Mishra, N S Chaudhary & M C Shrivastava, "New dynamic test methods for determination of Nonlinearity and effective resolution of A/D converters", IETE journal of research *(INDIA),* Vol. 43, no 6 , pp 403-409, Nov - Dec.1997.

[8] D. K. Mishra, "Some Methods for Dynamic Testing of A/D Converters" Ph. D. Thesis, May 2000.

[9] D K Mishra, Dynamic testing of high speed A/D converters using triangular Wave as input test signal, IE (I) Journal-ET-2005, Vol 85, pp 68-71, January 2005.

[10] D. K. Mishra and R. S. Gamad, "Determination of Non linearity and effective resolution of an A/D converter for arbitrary application input" international conf. on circuits and systems, San *Francisco*, USA 24-26, OCT. 2007.

[11] Athanasios Papoulis, "Probability, Random Variable and stochastic process," McGraw-Hill, Third edition, 1991.

[12] Hsin-Wen Ting, Bin-Da Liu and Soon-Jyh Chang," A Histogram- Based Testing Method for Estimating A/D Converter Performance" *IEEE transaction on Instrumentation and measurement,* vol 57, No 2, Feb 2008.