A Ka-Band CMOS Voltage Controlled Oscillator for High Speed Wireless Communication

Zhe-Yang Huang

***Abstract* — A 32.09GHz-34.59GHz Ka-Band CMOS Voltage-Controlled Oscillator (VCO) is designed for high speed wireless communication. The oscillator providing a center frequency of 33.34GHz and is implemented in 90nm Logic CMOS Technology. The oscillator core consumes 4.39mW through 1.0V supply voltage and the total chip area is 0.29mm^2 including pads and by-pass capacitors. A tuning range of 2.5GHz (32.09GHz-34.59GHz) with maximum control voltage of 1.0V can be achieved. And the phase noise is -85.2dBc/Hz at 1MHz offset from the center oscillator frequency. The calculated figure-of-merit (FOM) is -171.9dBc/Hz.**

***Index Terms* — CMOS, Voltage-Controlled Oscillator, VCO, Ka-Band.**

I. Introduction

In convention, the millimeter wave radio circuits are implemented in Gallium Arsenide (GaAs) or Silicon Germanium (SiGe) technologies [1-4]; but those technologies are not easy to integrate with baseband circuits and the cost is also high. Due to the CMOS technology is rapidly progressing, CMOS technology is becoming a good choice for millimeter wave components design. This paper is presenting a Ka-Band CMOS voltage controlled oscillator (VCO) for high speed wireless communication applications. VCO is a crucial component in wireless receiver system, and the most important performance is the phase noise which influences the sensitivity of the wireless communication system.

II. Circuit Implementation

Voltage controlled oscillator is implemented as Figure 1; including VCO core and buffer which is for measurement purpose. The output of the VCO is differential sinusoidal signal which means the phase of the signal is different from 180°. The core of the oscillator contributes continuous sinusoid millimeter wave to provide the mixing LO signals. And the buffer contributes the 50 Ohm impedance for measurement instruments. In this design, the VCO core and buffers are all designed on chip.

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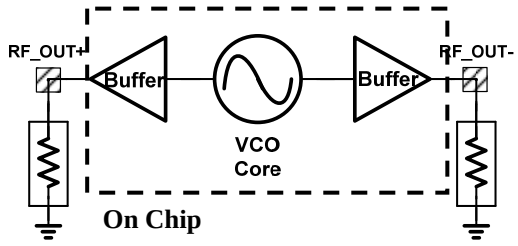

Figure1 Oscillator for Measurement Purpose

The circuit schematic of the Ka-Band voltage controlled oscillator is shown in Figure 2. M_1, M_2 are the cross coupled pair; L_1, L_2, L_3, L_4, C_1, C_2 are consisting of the LC-Tank; and M_3, M_4 are the source follower. NMOS cross coupled pair M_1, M_2 contributes the negative g_m for the VCO core and the condition of oscillation is expressed in equation (1). The LC-Tank determines the center frequency F_c of the oscillator which is expressed in equation (2). The capacitor C_1, C_2 are voltage controlled capacitors; the capacitance will be varied by the control voltage. Therefore, the center frequency F_c of the oscillator will also be changed. In Standard Logic CMOS 90nm process, the top metal is not ultra thick metal (UTM) and there are no standard inductors in foundry design kit (FDK). Therefore an accurate electro-magnetic (EM) simulation for inductor design is necessary and important.

$$g_m > 2/R_P \tag{1}$$

$$F_c = \frac{1}{2\pi\sqrt{L_1 \| L_2 (C_1 + C_p)}} \tag{2}$$

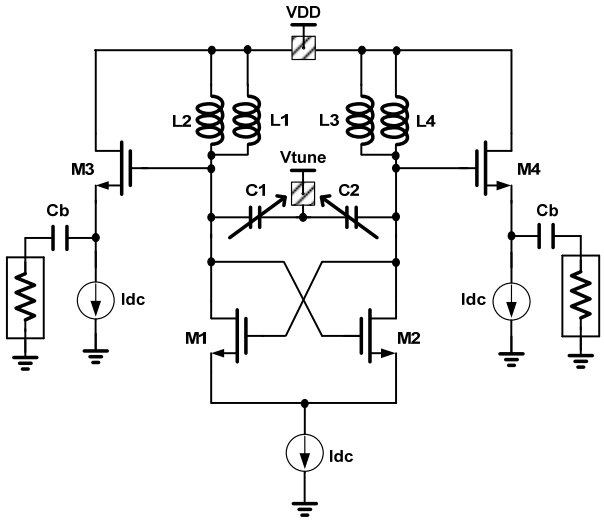

Figure2 Circuit of Voltage Controlled Oscillator

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The simulation results from electro-magnetic tool are illustrated in Fig. 3 and Fig. 4. The equivalent inductance of the parallel inductor is shown in Figure 3; the inductance at 33GHz is 181.5pH. And the quality factor (Q-Factor) is 17.35 and which is shown in Figure 4.

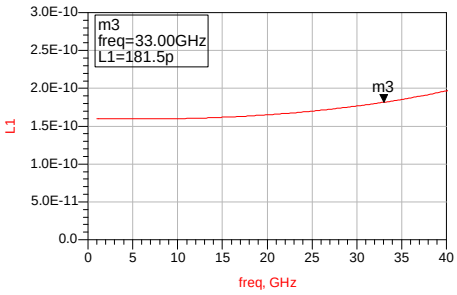

Figure3 Equivalent Inductance of Load

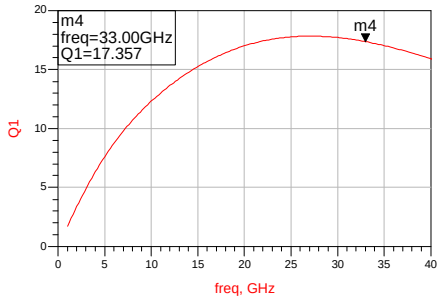

Figure4 Quality Factor of Load

III. Experiment Results

The core circuit of VCO draws 4.39mA current while consuming 4.39mW power through 1.0V supply voltage. The spectrum measurement results illustrated in Fig. 5 to Fig. 6; the oscillator frequency can be varied from 32.09GHz to 34.59GHz by 1.0V tuning controlled voltage; and this VCO has 2.50GHz tuning range. The output power of the VCO at 32.09GHz is -21.64dBm and at 34.59GHz is -18.08dBm. Phase noise of Ka-Band VCO is not able to measure directly in Signal Source Analyzer, thus down-conversion of the oscillated signal is necessary. There are two helpful solutions, one is dividing the frequency, and the other is mixing the mm-wave frequency. In this case, we choose to divide the mm-wave signal which is shown in Fig. 7. The divisor is set as 8, and the measurement frequency is down-converted into 4.235GHz. In Figure 7, the VCO oscillated signal will go through a pre-amplifier in order to make the divider sense the weak signal from VCO. The measured phase noise is -103.3dBc/Hz at 1MHz offset and -134.7dBc/Hz at 10MHz offset which is illustrated in Figure 8. But the phase noise is measured at 4.235GHz; it should be compensated 18.06dB which is expressed in equation (3). After compensating, the actual phase noise at 33.88GHz is -85.24dBc/Hz at 1MHz offset and -116.64dBc/Hz at 10MHz offset. The figure-of-merit (FOM) is expressed in equation (4) where $L(\Delta f_{offset})$ is phase noise at Δf_{offset} frequency offset, f_o is the center frequency of the oscillator, P_{DC} is the power dissipation of the oscillator. Finally, the calculated FOM is -171.90dB/Hz. Table1 is the performance conclusions of this voltage controlled oscillator; and Table2 is the performance comparisons with some recent works. The micro-photography of the chip is shown in Fig. 9. The whole chip size including all pads and all bypass capacitors is 0.45mm X 0.64mm and total area is 0.29mm^2.

$$PN_{comp} = 20 * \log(8) = 18.06dB \tag{3}$$

$$FoM = L(\Delta f_{offset}) - 20 * \log(\frac{f_o}{f_{offset}}) + 10 * \log(\frac{P_{DC}}{1mW}) \tag{4}$$

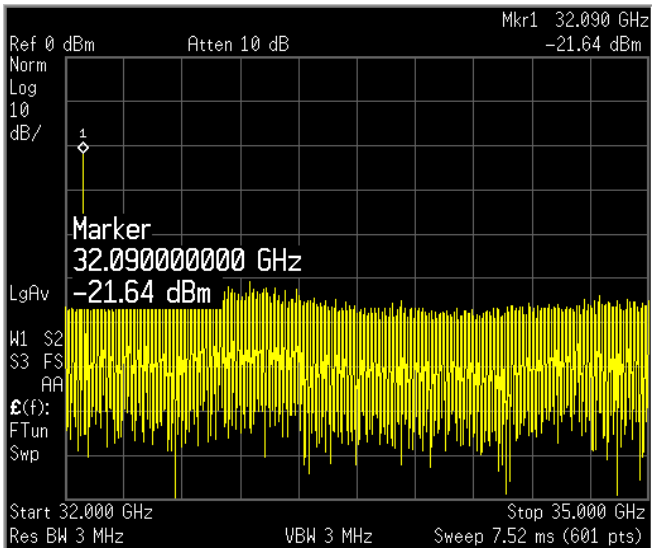

Figure5 Oscillation Frequency (Vtune=1.0V)

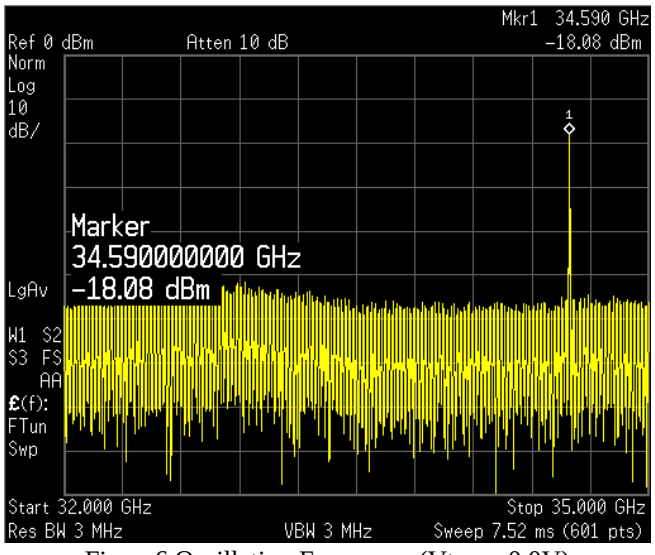

Figure6 Oscillation Frequency (Vtune=0.0V)

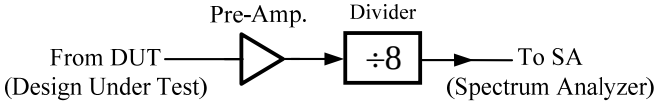

Figure7 Down-Conversion for Phase Noise Measurement

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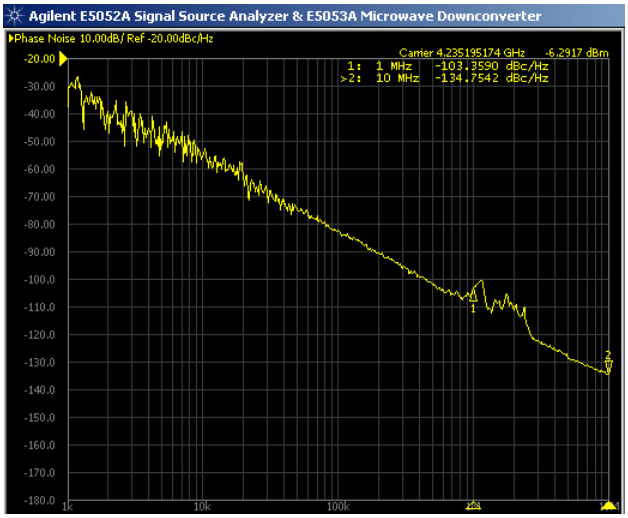

Figure8 Phase Noise @ 1MHz Offset from Center Freq.

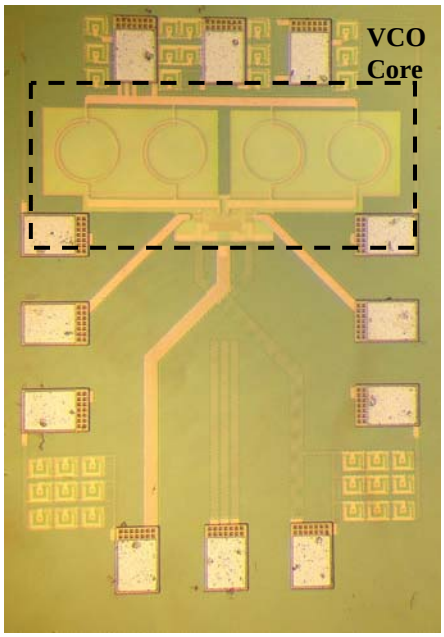

Figure9 Micro-Photography of Chip

IV. Conclusions

A 1V 4.39mW 32.09GHz-34.59GHz CMOS Voltage Controlled Oscillator (VCO) is designed and implemented in 90nm Logic CMOS technology for mm-wave high speed wireless communication system. The VCO is offering a center frequency of 33.34GHz and the tuning range of 2.5GHz (32.09GHz-34.59GHz). The oscillator core consumes 4.39mW through 1.0V supply voltage and the total area is 0.29mm^2. The phase noise is -85.2dBc/Hz at 1MHz offset and -116.6dBc/Hz at 10MHz offset from the center frequency. The calculated figure-of-merit (FOM) is -171.90dB/Hz.

TABLE1 Performance Conclusions

Technology	90nm Logic CMOS
Supply Voltage	1.0V
Oscillation Freq.	32.090 GHz ~ 34.590 GHz
Tuning Range	2.50 GHz
Output Power (w/i buff.)	-21.64dBm ~ -18.08dBm
Phase Noise (@1MHz offset)	-82.1dBc/Hz ~ -87.5dBc/Hz
Power Dissipation	4.39 mW
FOM	-171.90 dB
Chip Area	0.29mm^2 [0.45 X 0.64mm]

Acknowledgment

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TABLE2 Performance Comparisons

	Process	Osc. Freq. [GHz]	Output Power [dBm]	P.N. @1MHz [dBc/Hz]	Power Diss. [mW]	FOM [dBc/Hz]
[1]	InGaAs HBT	39.0	+2	-95.0	42.0	-170.6
[2]	GaAs pHEMT	28.3	+11.8	-102.0	80.0	-172.0
[3]	SiGe HBT	33.0	-17.0	-99.0	3.7	-183.7
[4]	GaAs	34.0	+4.0	-108.0	157.5	-176.7
[5]	CMOS SOI	40.0	-8.0	-90.0	11.3	-171.5
This Work	CMOS	33.34	-18.0	-85.2	4.4	-171.9

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