A Study on Retest Strategy Considering DUT Reliability for Memory Test

Chul-Min Lee, Jee-Hyong Lee

Abstract—**Yield is one of key factors determining the quality of semiconductor production process as well as production costs. Although continuous improvements have been carried out to enhance yield through hundreds of processes, the increase of the yield for mature products is not easy even by 0.1%.**

The yields of products are eventually determined at the test step. The types of failure at the test step are one of the intrinsic failure, the marginal failure and the facility failure. The intrinsic and marginal failure is related to the quality of devices, but the facility failure is due to poor test equipments irrelevant to the quality of devices. However, it is impossible to identify the type of failure at the test step, all devices which are tested as failure pass though the test step once more, which is call retest.

In this paper, we discuss how the current retest process efficiently removes the facility failure. Then, we estimate the portion of the facility failure in all types of failure in order to verify how much yield can be improved by removing the facility failure. Finally, we propose a device distributing strategy for retest steps that can minimize the facility failure by evaluating the reliability of DUTs.

Index Terms—**Semiconductor, Package Final Test, Retest, Raising Yield, DUT**

I. INTRODUCTION

THE semiconductor manufacturing process largely consists of three processes: the FAB (Fabrication) process of manufacturing wafers; the assembly process of producing packages from wafers by cutting wafers into individual devices (chips) and bonding those to lead frames; and the test process of inspecting whether products normally operate or not.

The test process is divided into the EDS test process, which is performed on wafers, and the package test, which is performed on package chips. The test process has two purposes. First, the test process intends to guaranty the operational specifications of devices. The other is to improve the reliability of the fabrication process [1][2].

The test equipments for the package test consist of tester, handler and socket/board. The tester generates electronic signals to be sent to packages under test. The handler inserts packages to the socket/board and after testing, moves out packages outside. The socket/board transmits electronic signals generated by the tester to packages.

In the package test, packages are tested for the reliability of DC characteristics, operating functions, voltage ranges, read/write functions of individual memory cells, power operation ranges, etc. For the test of those items, each package device is loaded on a test unit in the socket/board, called a DUT [1]. Through DUTs, electric signals are transmitted to each device for the package test.

If devices fail to pass the package test, those are determined as defective ones and discarded. The failure of devices can be divided into the intrinsic failure, the marginal failure, and the facility failure. The intrinsic failure is caused by actual defects in products, the marginal failure is a decisive problem of devices of which quality is on the border of non-defective and defective, and the facility failure is caused by the problems of test equipments, DUTs, even though products are not defective.

The facility failure usually occurs because of various problems including the electrical contact errors between devices and DUTs, and between DUTs and the tester, as well as the skew and deviations of test signals. These kinds of failure problems are not related to the product quality. Those products are manufactured without any defects but classified as defective ones. These wrongly classified products make the cost for hundreds of processes to produce the semiconductor devices in vain, and result in lowering the yield. Thus, the facility failure should be reduced for yield enhancement. However, it is impossible to identify the type of failure at the test step. For this reason, all the products determined defective at the test step are tested once more. This process is called “retest”. But in the current reset process, the large portion of the facility failure still remains even after the retest process because the retest is performed by the same test equipments, which may have some problems. The devices can be still placed on poor test equipments, DUTs, at the retest. Thus, this retest system does not meet the demands for the retest process.

In the current memory package system, a tester has tens or hundreds of DUTs. So, that number of devices can be tested simultaneously. Usually, the number of DUTs in a tester is 32, 64, 128, 256, 512, etc. In processing the first test, all DUTs in a test are loaded with devices to finish the test in the shortest time. But when the retest is being done, the number of retest devices is smaller than the number of DUTs. So, a handler does not need to load all DUTs in the retest step. Generally, a handler loads only 30~60% of DUTs.

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[1] DUT means device under test. In this paper, a DUT means a hardware unit for testing a package which includes a socket and socket board

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As mentioned, the facility failure mainly occurs because of the electrical contact errors between devices and DUTs, and between DUTs and the tester. Among electrical contact problems, those between devices and DUTs are easy to occur but hard to find. Even though a device is determined defective, it is hard to determine whether it originates from the device or the test equipments, DUTs. Also, the contact between DUTs and devices is exposed to outside, and it can have a lot of damage by devices and foreign substances more than other inner contact points. If we observe the yield variation of DUTs in the same system is higher than the expected one even considering with the quality variation of devices, which suggests that the reliability of each DUT in a system also varies much. In order to prevent yield drop by the facility failure, poor DUTs need to be avoided. However, it is not easy to determine whether a DUTS is poor or not. Even more, if we simply exclude poor DUTs, it can lead to productivity decrease. Thus, simple exclusion of poor DUTs is not a suitable solution to prevent the facility failure.

In this paper, we propose a new method to minimize the facility failure without any extra cost and any productivity degradation. This paper consists of four parts. Firstly, we draw the proportion of each failure by analyzing the first yield, the 1st retest yield, and the 2nd retest yield. Secondly, we analyze the tester reliability and the yield decrease due to the facility failure. Thirdly, we discuss the method of ranking the reliance in testing DUTs in order to maximize the yield by minimizing the defective proportion. Finally, we propose the handler retest input strategy of preferentially filling the excellent DUT.

The yield is a core index of the semiconductor manufacturing process, so there has been much effort to improve yield in the package test process since semiconductor industry launched. The efforts to improve the yield in test processes have focused on the improvement in the FAB processes. Based on the test result, engineers try to search for the root causes of yield decreasing.

Lee [3] presented a scheme of efficiently analyzing the root causes for decreasing yield by integrating the test data, such as defect wafer maps, die sort maps, and parametric test results. Bergeret [4] studied a method of searching for the processes causing the yield decrease by analyzing the defects found during the test processes and unit manufacturing processes which cause those. But in the memory processes where a number of mature products currently show a yield close to 100%, it is difficult to apply this scheme, as the number of defects is not sufficient to find out the causes for the yield decrease which is not limited to single manufacturing step.

To improve the yield in the processes of testing semiconductors, Sherry and Haupt [5] carried out a research. In this research, a strategy for hardware development was presented to raise the reliability of the test processes by analyzing the electrical contacts in the tester. This study is an effort to resolve the yield decreasing due to defective facilities in aspects of hardware in test facilities. But this approach can be applied to developing new test equipments but has limits to improving yield without improving the hardware of the test equipments which are already operating.

In this paper, we propose the method that can be applied without any hardware investment and is more effective to the products of which yield is very close to 100%.

II. Problem Analysis and Observation

The final test process is carried out by a unit of lots, which are composed of thousands of devices. If a lot is inputted into test facilities, the suitable test temperature and program for products are set up. Then, the handler repeats to place devices on DUTs as many as possible which can be tested at once until the test of the current lot finishes. Based on the test results, the products of the current lot are divided into non-defective and defective.

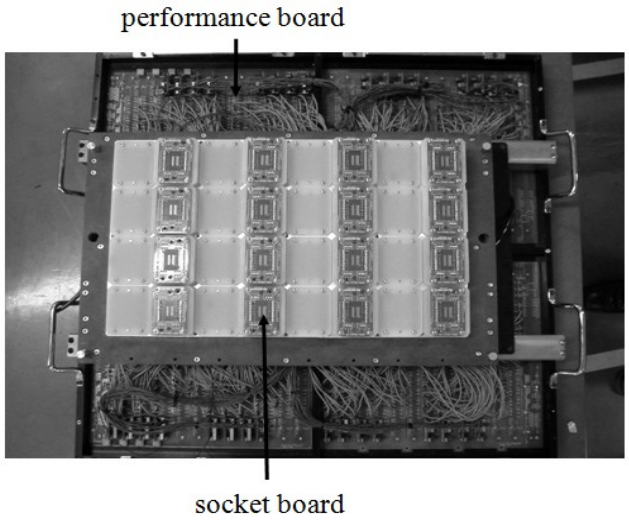

Figure1. Performance board and socket board

Figure1 shows a board which consists of a performance board and a socket board. To test device quality, the board transmits voltage or pulse which is supplied by the tester to device through socket.

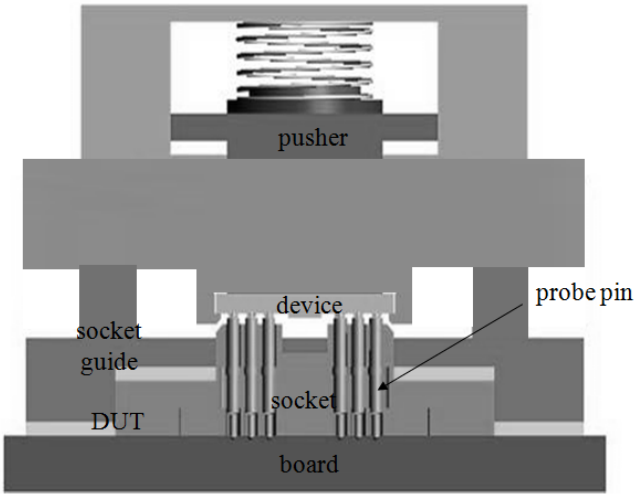

Figure2. Contact between device and socket. DUT is a unit which is tested being placed device, in above picture guide, socket and board are called collectively.

The socket is a bridge, linking a socket board to a device. Since sockets contact device, the performance of sockets is getting worse due to aging and harmful foreign substances. It is usually used till 70,000 contact times, or for

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3~5months. Figure2 shows a DUT. In a DUT, probe pins contact to a device to transmit test signals.

As mentioned before, a handler loads only 30~60% of DUTs. It is because each lot undergoes the test process separated from other lots not to be mixed up with others despite the decline in productivity. Mostly, lot merge has been prohibited for quality reasons.

There are three types of failure. But so far, there was no analysis on the ratio of each type in the total failure. Especially, to confirm occurrence of facility failure is necessary. It is essential that we decide to be worth improving. In this paper, we analyzed the portions of the three kinds of failure and the tester reliability to remove the facility failure. For the analysis, we define some terms as follows:

P: The ratio of actual non-defective devices
F: The ratio of actual defective devices
M: The ratio of devices that are on the margin of decision
R: The reliability of the test facilities
A_1: The ratio of non-defective devices in the first test
A_2: The ratio of defective devices in the first test
B_1: The ratio of non-defective devices in the1st retest
B_2: The ratio of defective devices in the 1st retest
C_1: The ratio of non-defective devices in the 2nd retest
C_2: The ratio of defective devices in the 2nd retest

Since all the devices under test are actually non-defective, actually defective or marginal, the sum of *P*, *F*, and *M* is equal to 1 as (1).

$$P + F + M = 1 \tag{1}$$

The tester reliability is the probability that non-defective products are determined to non-defective. There is little chance that defective products are determined to be non-defective products and it is reasonable that 50% of devices on the margin of decision can be determined to be non-defective. Thus, the ratio of non-defective products in the first test will be

$$PR + 0.5MR = A_1 \tag{2}$$

The ratio of non-defective products in the first test is A_1. *PR* is the ratio of being determined to be non-defective in actual non-defective products and *0.5MR* is the ratio that the devices in margin are determined to be non-defective products.

The ratio of defective products in the first test will be

$$P(1-R) + F + 0.5M(2-R) = A_2 \tag{3}$$

The ratio of defective products in the first test is A_2. *P(1-R)* is the ratio of being determined to be defective in actual non-defective products and *F* is the ratio of actual defective and *0.5MR(2-R)* is the ratio that the devices in margin are determined to be defective products.

The following equation (4) and (5) are related to 1st retest. Since the ratio of non-defective products in 1st retest is B_1 and detective in 1st retest are only input 2nd retest step, the ratio of non-defective products in the 1st retest will be

$$P(1-R)R + 0.25M(2-R)R = B_1 \tag{4}$$

P(1-R)R is the ratio of being determined to be non-defective in actual non-defective products among A_2 and *0.25M(2-R)R* is the ratio that the devices in margin are determined to be non-defective products among A_2.

The same way, since the ratio of defective products in 1st retest is B_1 and detective in 1st retest are only input 2nd retest step, the ratio of defective products in the 1st retest will be

$$P(1-R)(1-R) + 0.25M(2-R)(2-R) = B_2 \tag{5}$$

P(1-R)(1-R) is the ratio of being determined to be defective in actual non-defective products among A_2 and *0.25MR(2-R)(2-R)* is the ratio that the devices in margin are determined to be defective products among A_2.

Finally, the following equation (6) is related to 2nd retest and the ratio of non-defective products in the 2nd retest will be

$$P(1-R)(1-R)R + 0.125M(2-R)(2-R)R = C_1 \tag{6}$$

The ratio of non-defective products in the 2nd retest is C_1. *P(1-R)(1-R)R* is the ratio of being determined to be non-defective in actual non-defective products among B_2 and *0.125M(2-R)(2-R)R* is the ratio that the devices in margin are determined to be non-defective products among B_2.

If we know some constants such as, the ratios of non-defective and the ratios of defective devices in each test, we can solve equations (1), (2), (4) and (6). By observing the real *p*ackage test process, we obtain those constants as shown in Table1.

TABLE1. EXAMPLE OF DEFECTIVE/NON-DEFECTIVE PORTION IN PACKAGE TEST PROCESS

	first test	1st retest	2nd retest
non-defective (%)	97.78	1.58	0.14
defective (%)	2.22	0.64	0.50
total (%)	100.00	2.22	0.64

By solving equations (1), (2), (4) and (6) with the constants in Table1, we obtain the reliability of the test facilities, *R*, the ratio of non-defective, *P*, the ratio of defective devices, *F*, and the ratio of the devices in margin, *M*. The reliability *R* in the package test facility is 98.63%, the ratio of non-defective products *P* is 98.65%, the ratio of real defective products in the total volume *F* is 0.38%, and the ratio in margin *M* is 0.97%. Among the products determined to be defective in the first test, 2.22% of products, there are 1.35% points of non-defective products caused by the facility failure, which is 60.8% of the total failure in the first test. And among the products determined to be defective in the first test, 0.64% of products, , there are 0.02% points of non-defective products caused by facility failure. The portion of the three failure types in each test step is shown in Table2.

We found that 0.02% points yield drop was occurred even after the 1st retest step. If one more additional retest, the 2nd retest, is conducted, the facility failure will be almost removed. But, to carry out the additional retest, it may cause additional problems such as delivery, test facilities' capacity, and cost.

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TABLE2. EXAMPLE OF THE CAUSES FOR BEING DETERMINED TO BE DEFECTIVE IN PACKAGE TEST PROCESS

	first test	1st retest	2nd retest
Facility failure (%)	1.35	0.02	0.00
Intrinsic failure (%)	0.38	0.38	0.38
Marginal failure (%)	0.49	0.24	0.12
Total (%)	2.22	0.64	0.50

The facility failures occur because the reliability of tester is low. The reliability of tester is influenced by it of DUTs because the tester consists of DUTs as an independent unit in point of contacting the device to the tester. So, we need to analyze the reliability of each DUT. To make a detailed analysis for the reliability, the yield of each DUT was examined by supplying enough devices and analyzing, to overcome the statistical error.

TABLE3. YIELD BY DUT

DUT NO.	total	pass	yield(%)
177	931	799	85.8%
178	974	949	97.4%
179	966	955	98.9%
180	967	948	98.0%
181	974	962	98.8%
182	974	967	99.3%
183	974	967	99.3%
184	974	965	99.1%
185	973	968	99.5%
186	973	964	99.1%

Table3 shows 10 of 256 DUT in real mass-produce tester yield by DUT for a week. As seen in Table3, 0.1~13.2% of yield gap occurs. It suggests that the test reliability on all DUTs is not same and the defectiveness which is related to the facility failure intensively occurs in certain poor DUTs.

III. IMPROVED ALGORITHM

To effectively remove the facility failure as much as possible by conducting the retest only one time without additional retests, this paper focuses on two facts.

First, the number of devices loaded on the tester at once is lower than the total available DUTs. Second, the facility failure is strongly dependent to the DUT reliability. Thus, this paper proposes a scheme of preferentially inputting devices into the highly reliable DUTs. This strategy could refrain from inputting the devices into the poor DUTs and improve the facility failure which is caused by the low reliability on a tester.

A. Test Reliability Algorithm by DUT

The retest step is conducted because the defective/non-defective determination in the first test is not perfect and the retest step is conducted only using devices determined defective in first test step. If the device is tested in a very high reliable DUT, it will be determined defective in the retest as it was still determined in the first test. But if it is tested in a low reliable DUT, it could be occasionally determined non-defective in the retest as different as being tested in the first test. Therefore, if the device which was determined non-defective in the retest was wrongly classified because of facility failure in the first test, and the DUT which determined the device defective in the first test has low reliability. On the other hand, if the device which was determined defective in the retest was rightly classified, and the DUT which determined the device defective in the first test has high reliability. This paper proposes the algorithm to determine reliability for each DUT by using these kinds of accumulated results.

If the device determined defective in retest, 1 point is added at DUT that the device was determined defective on in the first test, and if not, 1 point is deducted. Under these calculations, the higher the score is, the higher reliability of the DUT is, on the other side, the lower score is, the lower reliability of the DUT is. But there is an error. In an assumption that as a result from the first test yield reaches 98% and the retest yield is 70%. If 1,000 devices by each DUT have been tested, 20 defective products occur on average as a result of the first test. Of this volume of 20 defective products, 14 ones are expected to be non-defective and the others expected to be defective. Under the algorithm suggested above, the score is expected to be -8. In this case, the expected score is estimated depending on the first test, the retest yield, and the number of first test devices. The larger the number of test devices is, the lower their scores are than expected. In other words, when the number of the first test devices is larger even if DUTs are same reliability, lower scores are estimated.

To revise this error, the expected score is subtracted from the score acquired by each DUT depending on the number of first test devices by DUT and divided by the expected score, Then, the final score (S) is drawn as follows:

$$E = d(1-P)(1-R) - d(1-P)R \tag{7}$$

$$S = \frac{(f-g)-E}{E} \tag{8}$$

where

P: The first test yield

R: The retest yield

d: The number of devices by a DUT in the first test

f: The number of devices determined defective by a DUT in the first test

g: The number of devices determined non-defective in the retest among the devices determined defective by a DUT in the first test

E: The expected score of a DUT

S: The score of a DUT

B. The procedure of applying prioritization by DUTs in the Retest step

In order to apply prioritization by DUT to retest policy, the tester should determine the priority order by score algorithm and the handler should control loading the device on DUT, as following three steps.

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First of all, the priority order should be determined by score algorithm. Next, calculate how many retest cycle[2] is necessary by dividing the number of DUTs into the number of total devices that are needed retest step. And, determine the number of devices each retest cycle by dividing the number of retest cycle into the number of total devices that are needed retest step. In the end, determine the number of excellent DUTs for each retest cycle. Figure3 illustrates that the flow chart of applying prioritization by DUT to retest policy.

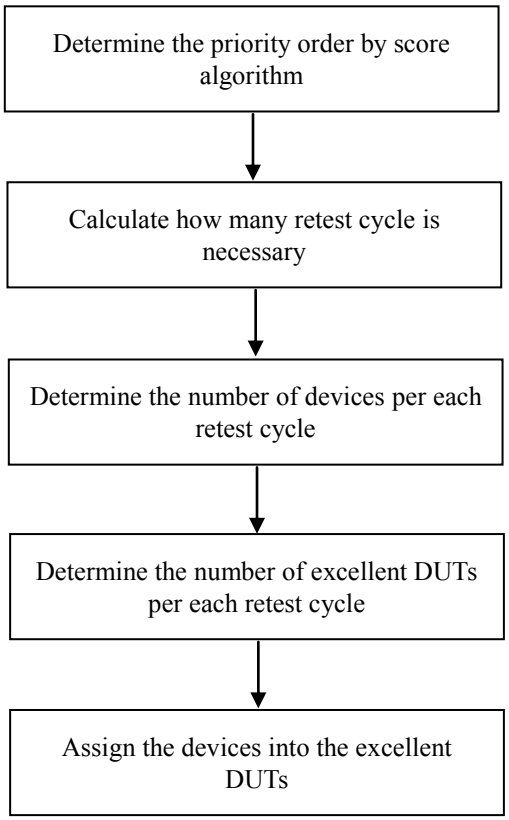

Figure3. The flow chart of applying prioritization by DUTs in retest step

For example, the procedure of 4,000 devices being tested in a tester which has 64 DUTS is following. If the yield is 98%, 80 devices are determined defective and then they are loaded to retest. First of all, the priority order should be determined by score algorithm based on previous test data. Next, because this tester can test 64 DUT in a cycle, 2 retest cycles are needed. And each cycle has 40 devices because 80 devices will be tested in two cycles. Finally, excellent 40 DUTs are chosen to contact with device each cycle.

IV. Evaluation and Analysis

In this paper, the reliability of DUTs were estimated and ranked. Based on this, this paper proposed a scheme of loading devices on DUTs for the improvement the final yield by minimizing the facility failure. To verify the effect of this loading scheme, it is compared to the current loading scheme.

We chose a 128 DUTs-tester for verification. And 35 lots which consisted of 122,196 devices were tested in it for 7 days in current retest method. 2,179 devices which determined defective in first test were collected by lots. The reliability scores of DUTs were calculated using the results of defective/non-defective determination in the first test and retest. Finally, the priority of each DUT was calculated.

TABLE4 The Ratio of Defective/Non-defective Decision by the verification tester that 122,196 devices determined in for 7 days

	First test	1st retest	2nd retest
Non-defective (%)	98.10	1.45	0.10
Defective (%)	1.90	0.45	0.35
Total (%)	100.00	1.90	0.45

TABLE5. The Causes for Defective Decision in Facilities by the verification tester that 122,196 devices determined in for 7 days

	First test	1st retest	2nd retest
Facility failure (%)	1.35	0.02	0.00
Intrinsic failure (%)	0.27	0.27	0.27
Marginal failure (%)	0.32	0.16	0.08
Total (%)	1.90	0.45	0.35

Table4 shows prime test, 1st retest and 2nd retest yield respectively which 35 lots have been tested for 7 days. Table5 shows result that each portion of detective kind has been analyzed by analysis method which is suggested in chapter 2.

Table6 shows the result that each DUT of the tester prioritized by suggested in chapter 3.

TABLE6. The Results of the Reliability Test of DUTs

order	DUT No.	first test			retest			detective in first test			expected score (E)	score (S)
		total	pass	yield (%)	total	pass	yield (%)	total	pass	yield (%)		
1	248	1000	993	99.2	27	18	66.7	8	1	12.5	-10.7	1.6
2	197	996	990	99.4	32	23	71.9	6	0	0.0	-10.7	1.6
3	203	991	986	99.5	20	16	80.0	5	0	0.0	-10.6	1.5
63	168	969	965	99.6	9	9	100	4	2	50.0	-10.4	1.0
87	143	984	971	98.7	15	11	73.3	11	10	90.9	-10.5	0.1
88	249	982	964	98.2	22	16	72.7	18	14	77.8	-10.5	0.0
105	145	963	937	97.3	10	9	90.0	23	21	91.3	-10.3	-0.8
113	193	989	949	96.0	32	23	71.9	37	32	86.5	-10.6	-1.6
114	216	965	922	95.5	38	27	71.1	39	33	84.6	-10.3	-1.6
118	225	868	813	93.7	20	12	60.6	46	39	84.8	-9.3	-2.4
119	242	951	900	94.6	23	15	65.2	49	43	87.8	-10.2	-2.6
127	131	860	756	87.9	7	4	57.1	99	96	97.0	-9.2	-9.1
128	177	931	799	85.8	5	2	40.0	131	124	94.7	-10.0	-10.7

2,179 devices, which were determined to be defective in the first test, were loaded into DUTs in their priority and the retest proceeded again by original lots. For the comparison of the prioritization scheme, two another DUT prioritization schemes were evaluated, which are based on the first test yield and the retest yield, respectively. The retest process progressed in the same way. Figure4 shows the retest and final yield of each method. Figure4 illustrates that the system of the proposed scheme, which preferentially loads devices into the reliable DUTs based on the scoring method, is more effective than the current method. This profit is 0.09% of the

[2] Cycle means the repeat count of test. Usually, the number of DUTs in a tester is 32, 64, 128, 256, 512, etc. So, that number of devices can be tested simultaneously. If DUT in a tester is 64 and inputting device is 100, then 2 test cycles are needed.

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final yield. This yield improvement means that the facility failure was complete cleared and the marginality failure is also improved. In other words, the devices were often determined lower quality than actual their quality in poor DUT. This wrong determination has improved by restriction on inserting device into poor DUT. Therefore, amount of device which was determined to detective is able to be determined non-detective.

In addition, the results from applying the retest scheme by prioritizing them using the first test yield or the retest yield by DUTs showed satisfactory results, compared with current method. In case it is difficult to apply the prioritization based on the scoring system by DUTs, it is recommendable to review the prioritization using the first test yield or retest yield.

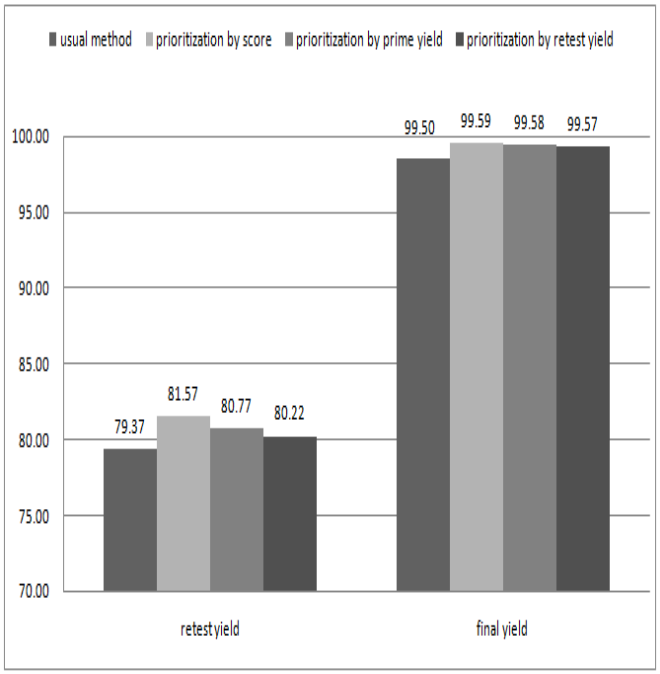

Figure4. The Comparison of Yields during Retest in Applying a Scheme of Inputting Devices into DUTs

As shown in Figure4, the retest scheme of loading devices into the excellent DUTs firstly, is expected to replace the current method. Even though the yield improvement is about 0.09% point the economical effect is not ignorable. If one billion products were produced in a month and 0.09% of the yield improved, it is obvious to secure 900,000 non-defective products which were discarded due to the facility failure. Thus, if the unit cost per device is 1 dollar, at least 900,000 dollars per month and 10,800,000 dollars per year of profits are expected.

V. Conclusions

This paper made a statistical analysis on the types of failure in the memory test processes and inferred the ratio of failure in various aspects of intrinsic failure, marginal failure, and facility failure. To improve the facility failure which is caused by the low reliability on test facilities, we proposed a retest strategy, which preferentially place devices on the excellent DUTs in the retest process.

This strategy is expected that the reliability on tester will be improved. And it could make a contribution to improve the yield in semiconductor manufacturing processes by minimizing the facility failure.

The yield in semiconductor manufacturing processes is an index that can determine the outcome of the company. In a situation where individual semiconductor manufacturers are doing their utmost to improve the yield, the strategy proposed in this paper is an efficient scheme that may improve the yield, as it can apply to all other product groups without any additional investment on hardware.

References

[1] Segers, R., “If It's All about Yield, Why Talk about Testing?”, Test Symposium, 2007. ETS '07. 12th IEEE European, pp. 1-3.

[2] O’Neill, P. M., “Statistical test: A New Paradigm to Improve Test Effectiveness & Efficiency”, INTERNATIONAL TEST CONFERENCE, 2007, pp. 1-10.

[3] Lee, F. and Smith, S., “Yield analysis and data management using Yield Manager™”, Advanced Semiconductor Manufacturing Conference and Workshop, 1998. 1998 IEEE/SEMI, pp. 19-30.

[4] Bergeret, F. and Le Gall, C., “Yield Improvement Using Statistical Analysis of Process Dates”, IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, vol. 16, no. 3, august 2003, pp 535-542.

[5] Sherry, J. and Haupt, D., “Optimizing the whole test system to achieve optimal yields and lowest test costs”, ELECTRONICS MANUFACTURING TECHNOLOGY SYMPOSIUM, 2004. IEEE/CPMT/SEMI 29th International, pp. 282-294.

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