An on-chip Low Drop-Out Voltage Regulator with 150mA Driving Capability

Lv Xiaopeng, Bian Qiang, Yue Suge

Abstract—To realize DC voltage conversion from 3.3V to 1.8V for SoC application, a fully on-chip Low Drop-Out (LDO) voltage regulator with 150mA driving capability is presented. Implemented in 0.18μm CMOS technology, the proposed LDO voltage regulator utilizes paralleled input differential pairs and current amplifiers to provide fast transient response, achieving 1.4μs settling time with transient variation less than 155mV.

***Index Terms*—Capacitor-less LDO; Frequency compensation; Transient response; Power supply rejection.**

I. Introduction

As an essential building block of the power management system, the Low Drop-Out (LDO) voltage regulators based on feedback provide an accurate and stable voltage with corresponding load current. Recently, the off-chip output capacitor of several micro farads is eliminated for System on Chip (SoC) application [1]; however, the on-chip output capacitor is deceased to only several tens or hundreds of pico farads, degrading the stability and the transient response.

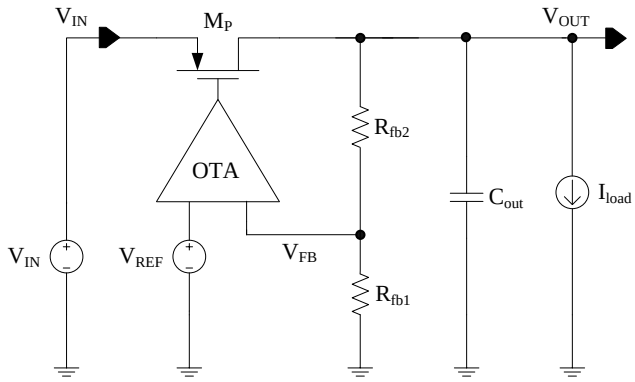

Fig. 1. Structure of on-chip LDO voltage regulator

The structure of fully on-chip LDO voltage regulators implemented in CMOS technology (Fig. 1) often uses the PMOS FET with common source connection as the pass transistor between the input and output voltages. An amplified error signal is fed back to the gate of the pass transistor through the feedback loop to respond to the load current while keeping the output voltage constant. Stability over the full range of load current and small output voltage variation during load current transient are the state-of-art of the on-chip LDO voltage regulators.

Several approaches have been introduced to on-chip LDO voltage regulator for SoC application. Lau *et al.* proposed advanced Q-reduction circuit with minimum load current of 100 μA [2]; Milliken *et al.* adopted differentiator and current amplifier for stability and fast transient response [3]; Ho *et al.* employed active feedback and slew rate enhancement to minimize compensation capacitor and speed up transient response [4].

In this paper, an OTA based on paralleled differential input pairs and current amplifier is adopted to increase GBW and SR, speeding up the transient response; Miller compensation is employed to ensure loop stability with load current from 100μA to 150mA. The proposed LDO voltage regulator with 100pF on-chip output capacitor provides 1.8V output voltage with 150mA driving capability. In section II, stability, transient response and power supply rejection characteristics of the proposed LDO voltage regulator are discussed. In section III, the static-state, dynamic-state and PSR characteristics are simulated and corresponding simulation results are summarized with comparisons. The conclusion is derived in section IV.

II. The Proposed LDO Voltage Regulator

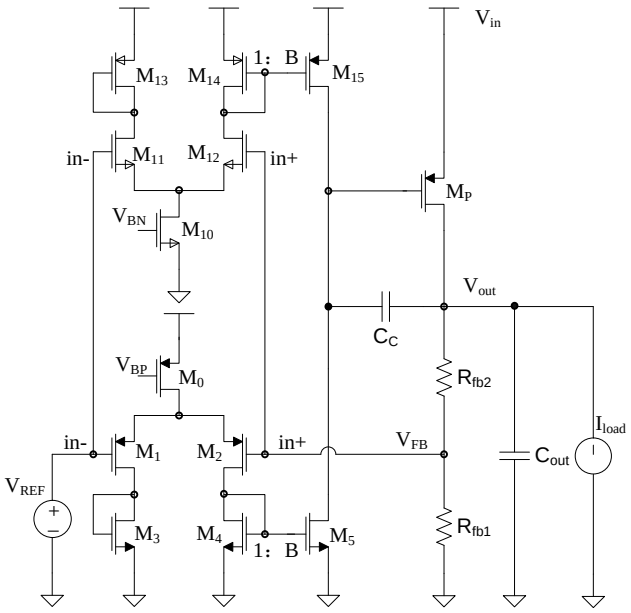

Fig. 2. Schematic of the proposed on-chip LDO voltage regulator

The transistor level implementation of proposed on-chip

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ISBN: 978-988-19251-7-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

LDO voltage regulator is shown in Fig. 2. Transistors M_0-M_5 and M_{10}-M_{15} forms the symmetrical OTA with paralleled input differential pairs, where B is the current gain. The PMOS FET M_P in common source connection is the pass transistor between the input and output voltage. The series feedback network composed of R_{fb1} and R_{fb2} provides the feedback signal V_{FB} to the non-inverting input of the OTA while the reference provides the signal V_{REF} to the inverting input of the OTA.

A. Stability analysis

For stability analysis of the feedback loop, small signal equivalent circuit of the proposed on-chip LDO is shown in Fig. 3, where G_m is the transconductance of the paralleled input differential pairs, R_0, C_0 are the resistor and capacitor at the OTA output. C_{out} is the on-chip output capacitor at the output of the LDO voltage regulator.

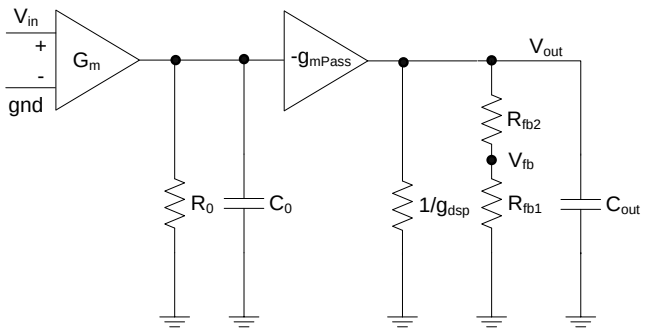

Fig. 3. Small signal equivalent circuit

The small signal loop gain at low frequency can be given as bellow

$$LG = \frac{V_{fb}}{V_{in}}\beta = A_{V\_OTA}A_{V\_P} = G_m R_0 g_{mPass}\left(\frac{1}{g_{dsP}} \| \left(R_{fb1}+R_{fb2}\right)\right)\frac{R_{fb1}}{R_{fb1}+R_{fb2}} \quad (1)$$

Where A_{V_OTA} and A_{V_P} are the voltage gain of the OTA and pass transistor, respectively; β is the feedback factor. The total input transconductance $G_m = B(g_{mN} + g_{mP})$, where B is the current gain; g_{mN} and g_{mP} are the transconductance of the paralleled complementary input differential pairs. g_{mPass} is the transconductance of the pass transistor.

The dominant and non-dominant poles of the feedback loop can be given as

$$f_d = \frac{1}{2\pi R_0 C_0} \quad (2)$$

$$f_{nd} = \frac{1}{2\pi\left(\frac{1}{g_{dsP}} \| \left(R_{fb1}+C_{fb2}\right)\right)_{out}} \quad (3)$$

The gain bandwidth product (GBW) of the feedback loop can be obtained from equations (1) and (2)

$$GBW = LG \times f_d = \frac{G_m A_{V\_P}\beta}{2\pi C_0} \quad (4)$$

Since the operating state of the pass transistor is dramatically changed with the load current, the small signal gain of the pass transistor A_{V_P} and the capacitor C_0 at the OTA output are dramatically affected. Correspondingly, the non-dominant pole f_{nd} locating at the LDO voltage output will change with load current, degrading the stability of the feedback loop.

To ensure the stability of the feedback loop and improve the transient response, a Miller compensation capacitor C_C is adopted for the worst case frequency compensation. The non-dominant pole f_{nd} should be 3 times beyond the GBW, given as bellow,

$$\frac{1}{2\pi\left(\frac{1}{g_{dsP}} \| \left(R_{fb1}+C_{fb2}\right)\right)_{out}} > 3\times\frac{G\beta_m}{2\pi C_c} \quad (5)$$

The simulation demonstrates that the capacitor should be 7pF for a minimum load current of 100μA. The simulated frequency response of the feedback loop with 7pF Miller compensation capacitor is given in Fig. 4, where the load currents are at the minimum and maximum level respectively.

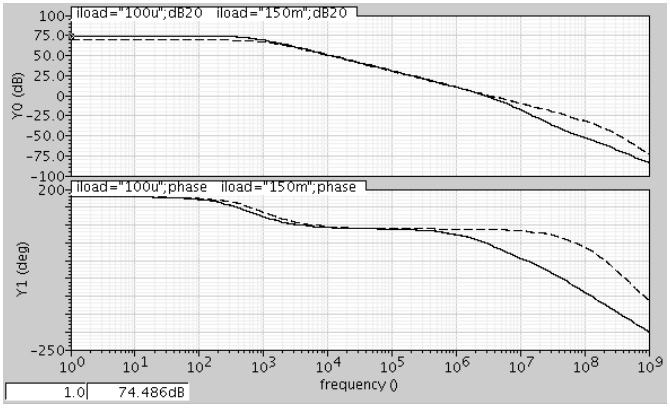

Fig. 4. Frequency response under different load current

(——solid for 100μA; ------dashed for 150mA)

The simulated Phase Margin (PM) under different load current is given in Fig. 5, where the PM is at least 50 degree, ensuring the stability of the feedback loop with load current from 100μA to 150mA.

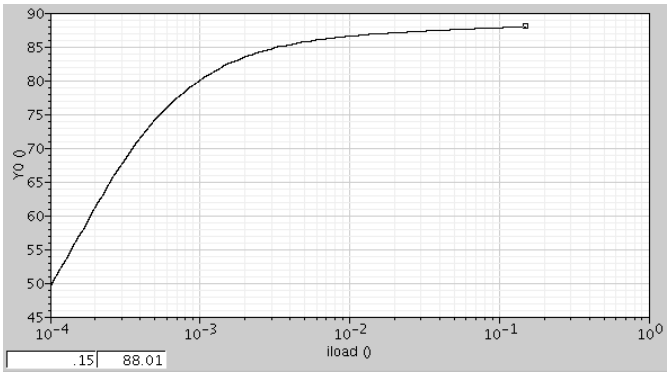

Fig. 5. Phase Margin under different load current

B. Transient analysis

Comparing with the conventional LDO voltage regulator with off-chip output capacitor of several micro farads, the on-chip LDO uses the power line capacitor of several tens pico farads as the output capacitor. During the load transient between different levels, the feedback loop can't respond

ISBN: 978-988-19251-7-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

immediately; the output voltage is sustained through charging or discharging the output capacitor. Thus, the variation of the output voltage can be given as

$$\Delta V_{out} = \frac{\int_{t_0}^{t_1} i(t)dt}{C_{out}} = \frac{\int_{t_0}^{t_1} [i_{load}(t) - i_{Mp}(t)]dt}{C_{out}} \quad (6)$$

where t_0 is the moment when the load current changes, t_1 is the moment when the feedback loop settles; the transient current i(t) passing through the output capacitor C_{out} is the differential current between the load current $i_{load}(t)$ and the current $i_{Mp}(t)$ provided by the pass transistor. Even for on-chip output capacitor of 100pF, the variation needs to be controlled within 10% of the output voltage, requiring the feedback loop respond to the load current as fast as possible.

The transient regulation characteristic of the LDO voltage regulator during large current transient depends on the slewing rate (SR) and gain bandwidth product (GBW) of the feedback loop [5]. Large parasitic capacitor at the gate of the pass transistor causes slew effect, degrading load transient response. In the proposed LDO voltage regulator, paralleled input differential pairs and the current amplifiers increase both SR and GBW with a factor of current gain B, thus, the variation of the output voltage is decreased through speeding up transient response during load current transient.

C. Power supply rejection analysis

For the power supply plagued by noise in the SoC environments, the LDO voltage regulator with a high PSR over a wide frequency range shields noise-sensitive blocks from high frequency ripples in the power supply [6]. However, several paths between the input and output voltage of the LDO voltage regulator cause finite PSR over a limited frequency range [7]. Considering the direct path through the transconductance g_{mPass} and conductance g_{ds} of the pass transistor, the PSR of the proposed LDO voltage regulator can be approximately given as

$$PSR = \frac{1 + A_{V\_P}}{1 + \frac{1}{g_{dsP}(R_{fb1} + R_{fb2})} + \frac{1}{sC_{out}} + \frac{LG}{1 + s/2\pi f_d}} \quad (7)$$

Where A_{V_P} is the voltage gain of the pass transistor; LG is the loop gain at low frequency; f_d is the frequency of the dominant pole. Concludingly, the PSR at low frequency is mainly determined by the loop gain. However, the loop gain is reduced at higher frequency due to the dominant pole f_d, degrading the PSR at higher frequency. To obtain a high PSR over a wide frequency range, both high loop gain and dominant pole of high frequency have to be realized at the same time.

III. Simulation Results

The performance of the proposed LDO voltage regulator is simulated under 0.18μm CMOS technology. The input, output and reference voltage are 3.3V, 1.8V and 1.2V respectively, while the series feedback resistors are 30kΩ and 60kΩ with feedback factor of 2/3. The transistor dimensions and bias conditions are summarized in Table I.

TABLE I.
TRANSISTOR DIMENSIONS AND BIAS CONDISIONS

Transistor	W(μm)	L(μm)	I_D (μA)
M_0	5	1	20
M_1, M_2	12	1	10
M_3, M_4	1.5	1	10
M_5	3×1.5	1	30
M_{10}	2	1	20
M_{11}, M_{12}	2	1	10
M_{13}, M_{14}	8	1	10
M_{15}	3×8	1	30
M_P	15×100	0.26	20

A. Static-state regulation characteristics

• Line regulation

The output voltage of the proposed LDO voltage regulator with the input voltage swept from 1.8V to 4V is given in Fig. 6.

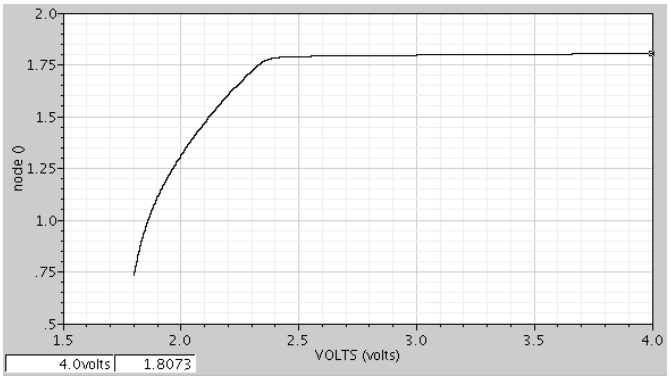

Fig. 6. Line Regulation

The simulation result illustrates that the output voltage variation is 22mV when the input voltage changes from 2.4V to 4V with the drop-out voltage higher than 600mV, resulting in the line regulation of 13.75μV/mV.

• Load regulation

The output voltage of the proposed LDO voltage regulator with the load current swept from 0 to 150mA is given in Fig. 7.

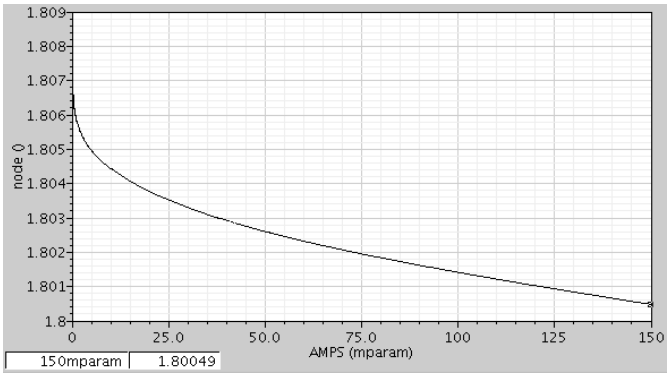

Fig. 7. Load Regulation

ISBN: 978-988-19251-7-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

The simulation result illustrates that the output voltage variation is 7.6mV with the load current changing from 0 to 150mA, resulting in the load regulation of 51μV/mA.

Both line regulation and load regulation specify the static-state regulation characteristics of the output voltage for a given range of input voltage and load current, which can be improved through increasing the feedback loop gain.

B. Dynamic-state regulation characteristics

The load transient response of the proposed LDO voltage regulator with 100pF on-chip output capacitor is given by Fig. 8. The load current varies between 1mA and 150mA with rising and falling time of 1μs.

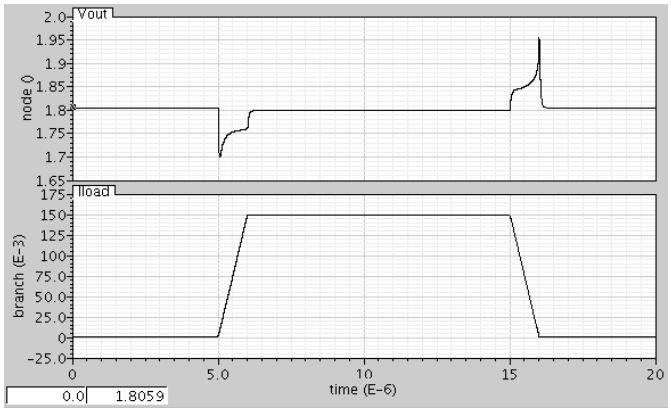

Fig. 8. Load transient response

The simulation results illustrate that the output voltage variation is 108mV, 153mV respectively; with settling time of 1.2μs, 1.4μs.

C. Power supply rejection characteristics

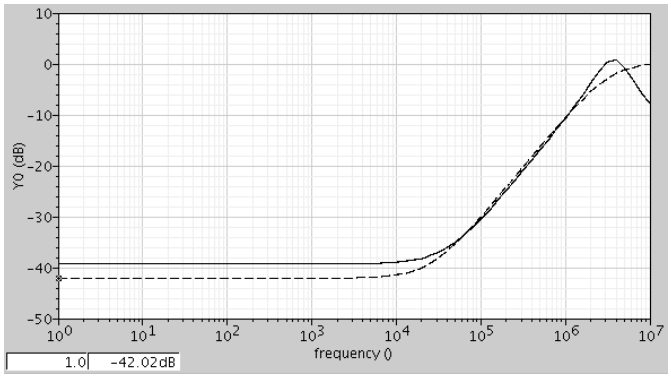

Fig. 9. Power supply rejection

(——solid for I_{load}=100μA; ------dashed for I_{load}=150mA)

The power supply rejection under minimum and maximum load currents is given in Fig. 9. The simulated result illustrates that the PSR is around -40dB at low frequency and -30dB at frequency of 100 kHz.

D. Summarized characteristics and comparisons

The characteristics of the proposed on-chip LDO voltage regulator with 100pF on-chip output capacitor are summarized in Table II, and compared with references [2], [3] and [4] implemented in 0.35μm CMOS technology.

TABLE II.
SUMMARY AND COMPARISON

Paper	[2]	[3]	[4]	This work
C_{com}(pF)	6	21	7	7
I_Q(μA)	100	65	20	90
I_{load}(mA)	100	50	100	150
Line regulation	344 μV/V	1%	57.4 μV/mV	13.75 μV/mV
Load regulation	388 μV/mA	2%	109 μV/mA	51 μV/mA
ΔV_{out} (mV)	<50	<90	<100	<155
Δt(μs)	30	15	9	<1.4
PSR(dB)	NA	-55@DC	-40@10k	-40@DC -30@100k

IV. CONCLUSION

The proposed on-chip LDO voltage regulator implemented in 0.18μm CMOS technology realizes DC voltage conversion between 3.3V and 1.8V with 150mA driving capability while consuming only 90μA quiescent current. The load transient can be recovered within 1.4μs with variation within 10% of the output voltage.

ACKNOWLEDGMENT

The author would like to thank Guo Wei for his discussions and technical supports on the LDO voltage regulator design.

REFERENCES

[1] Dennis D. Buss, "Technology in the Internet Age," ISSCC 2002
[2] S. K. Lau, P. K. T. Mok, and K. N. Leung, "A low-dropout regulator for SoC with Q-reduction," *IEEE J. Solid-State Circuits*, vol. 42, no. 3,pp. 658–664, Mar. 2007.
[3] R. J. Milliken, J. Silva-Martínez, and E. Sánchez-Sinencio, "Full on-chip CMOS low-dropout voltage regulator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 9, pp. 1879–1890, Sep. 2007.
[4] Edward N. Y. Ho and Philip K. T. Mok, "A Capacitor-Less CMOS Active Feedback Low-Dropout Regulator With Slew-Rate Enhancement for Portable On-Chip Application," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 2, pp. 80–84, Feb. 2010.
[5] C. T. Chuang, "Analysis of the settling behavior of an operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-17, NO.1, pp. 74–80, Feb. 1982.
[6] V. Gupta and G. A. Rincon-Mora, "A Low Dropout, CMOS regulator with High PSR over Wideband Frequencies," *ISCAS*, vol. 5, pp. 4245-4248, 2005.
[7] Mohamed El-Nozahi, Ahmed Amer, Joselyn Torres, Kamran Entesari, and E. Sánchez-Sinencio, "High PSR Low Drop-Out Regulator With Feed-Forward Ripple Cancellation Technique," *IEEE J. Solid-State Circuits*, vol. 45, NO.3, pp. 565–577, Mar. 2010

ISBN: 978-988-19251-7-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)