Fault-Tolerant Application-Specific Network-on-Chip

Fathollah Karimi Koupaei[1], Ahmad Khademzadeh[2] and Majid Janidarmian[3]

Abstract*—The fast scaling in technology has caused the components of a Network-on-Chip (NoC) to be more susceptible to faults; therefore, there is a need for methods to maintain circuit reliability. A fault-tolerant NoC should be able to detect a fault and recover the system to correctly operate the mapped application. In this paper, a fault-tolerant NoC architecture designed in VHDL and synthesized using Xilinx ISE is presented which not only is able to recover from single permanent router failure, but also improves the average response time of the system. In this design, a new component, called Link Interface (LI) is also developed to reduce hardware overhead.

Index Terms— **Deadlock-Free Routing Algorithm, Fault-Tolerant Design, Link Interface, Mapping Algorithm, Network-on-Chip.**

I. Introduction

THE number of processor, memory and accelerator cores on systems on chip is rapidly increasing to support evolving standards and new applications. Computation and communication complexity is skyrocketing, and scalability-centric design paradigms are critically needed [1]. Networks-on-Chip (NoCs) have emerged as the best alternative to provide high performance in communication for futures Systems-on-Chip (SoCs) with dozens of cores integrated on a single silicon die. Mapping an application to on-chip network is the first and the most important step in the design flow as it will dominate the overall performance and cost [2]. Several approaches have been proposed in literature in the context of topological mapping in NoCs [3]. Mapping algorithms are mostly focused on 2D mesh topology which is the most popular topology in NoC design due to its layout efficiency, good electrical properties and simplicity in addressing on-chip resources. Another concern in NoC implementation is selecting an efficient routing strategy while providing freedom from deadlock. The routing algorithm determines the path that each packet follows between a source-destination pair. In the future chip generations, faults will appear with increasing probability due to the susceptibility of shrinking feature sizes to process variability, age-related degradation, crosstalk, and single-event upsets. To sustain chip production yield and reliable operation, very large numbers of faults will have to be tolerated [4, 5]. This argument strengthens the notion that chips need to be designed with some level of built-in fault tolerance. Furthermore, relaxing the requirement of 100% correctness in the operation of various components and on-chip channels profoundly reduces the manufacturing cost as well as cost incurred by test and verification [6].

The remainder of this paper is organized as follows: In Section 2, an overview of some fault-tolerant research efforts in NoC is given. Section 3 illustrates the basic concepts of application-specific NoC design, and a new fault-tolerant architecture is introduced in section 4. Simulation results i.e. average response time and hardware overhead will be presented in section 5 followed by the concluding remarks in Section 6.

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II. Related Work

Scaling of interconnects exacerbates the already challenging reliability of on-chip networks. As process technology scales, the integration of billions of transistors comes with an increased likelihood of failures. Smaller dimension circuits are getting more sensitive to a particle strike, increasing the probability that the charge due to a high-energy particle flips the value in a cell [7]. With technology trends in device scaling, high clock frequencies, and supply voltage decreases, fault rates are increasing, which makes a reliable design a real challenge. Transient and Permanent errors are two main kinds of errors which generally occur in an NoC. The most common transient error recovery technique is the retransmission mechanism following error detection techniques like coding [8]. Many recently developed solutions focus on methods keeping the system working in spite the fact that some parts of the system are shut down [9]. Permanent faults in NoCs due to fabrication challenges in sub-65 nm CMOS technologies and due to wearout underscore the need for fault-tolerant design [10]. Fault-tolerant routing algorithms are recently investigated to bypass the failed hardware. The inherent redundancy in NoCs due to multiple paths between packet sources and sinks can greatly improve communication fault resiliency [10]. Fault-tolerant routing algorithms should be able to find a path from source to destination in presence of the faults in NoC with a certain degree of tolerance [11]. Many algorithms in this area have been proposed which follow their own optimization aims. To name just a few, in [10], the authors propose a novel low-overhead neighbor aware, turn model based fault-tolerant routing scheme (NARCO) for NoCs which combines threshold-based replication in network interfaces, a parameterizable region-based neighbor awareness in routers, and the odd–even and inverted odd–even turn models. [12] presents the scalable and fault-tolerant distributed routing (SFDR) mechanism. It

ISBN: 978-988-19251-7-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

supports three routing modes including corner-chains routing, boundary-chains routing and fault-ring routing. Inspired by divide-and-conquer concept, system is partitioned into nine regions. Each region promises fault-tolerance of one's own when packets bounded into its area to guarantee total fault tolerance. The main problem with the fault-tolerant routings is that if a router fails, considering mesh architecture, recovery cannot be accomplished only by rerouting. In addition, hardware redundancy is inevitable in order to repair the lost connection to the network of the core directly connected to the failed router. A fault-tolerant mesh-based NoC architecture with the ability of recovering from single permanent failure is presented in [13]. This method adds a redundant link between each core and one of its neighboring routers, resulting in significant improvement in reliability while has little impact on performance. In this architecture, only one spare router should be selected among all possible alternative ones. This has an influential effect on overall performance in terms of the average response time and reliability of the system. Regarding to this work, in [14] a new fast and optimum algorithm based on performance measurement and extra communication cost is proposed to find the best configuration that also results in a more reliable system. It also shows that mapping algorithm has a great impact on mentioned parameters. Following this concept, in this paper, a hardware and performance-aware design for the fault-tolerant NoC architecture is presented which takes in to account the specific application mapped onto mesh topology.

III. PREREQUISITES OF APPLICATION-SPECIFIC NOC DESIGN

A. Mapping Problem

To formulate mapping problem in a more formal way, we need to first introduce the following two concepts borrowed from [15]:

Definition 1: The core graph is a directional graph $G(V,E)$, whose each vertex $v_i \in V$ shows a core, and a directional edge $e_{i,j} \in E$ illustrates connection between v_i and v_j. The weight of $e_{i,j}$ that is shown as $comm_{i,j}$, represents the communication volume from v_i to v_j. The IP core along with a router connected to it by Network Interface (NI) is displayed as a tile.

Definition 2: The NoC architecture graph is a directional graph $A(T,L)$, whose each vertex $t_i \in T$ represents a tile in the NoC architecture, and its directional edge that is shown by $l_{i,j} \in L$ shows a physical link from t_i to t_j.

The core graph mapping $G(V,E)$ on NoC architecture graph $A(T,L)$ is defined by a one to one mapping function.

$$map: V \to T, s.t. map(v_i) = t_j, \forall\, v_i \in V, \exists t_j \in T, |V| \le |T|$$

Mapping algorithms are mostly focused on 2D mesh topology (Architecture Graph) which is the most popular topology in NoC design due to its suitability for on-chip implementation and low cost. The definitions are presented in Fig. 1.

B. Routing Algorithm

The routing algorithm determines the path that each packet follows between a source-destination pair. Routing algorithms noticeably affect the cost and performance of NoC parameters i.e. area, power consumption and average message latency [16]. Due to determined sources and destinations in application-specific NoC, minimum-distance routing algorithms are mostly considered in this area which is computed off-line and admissible paths stored into the routing tables.

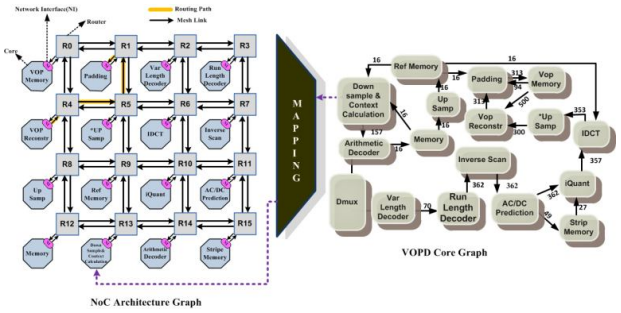

Fig.1: Mapping problem concepts

In general, every routing algorithm should include deadlock freedom feature [17]. So channel dependency graphs (CDG) is used to avoid any possible deadlocks. The CDG is a directed graph with the network channels as the vertices and the direct dependencies between the two channels as the edges. A dependency exists between the links $l_{i,j}$ and $l_{j,k}$ whenever there is a path to route packets from v_i to v_k through v_j which uses those links. An extension to CDG as a sub graph is the concept of application specific channel dependency graph (ASCDG) introduced in [18]. The ASCDG is a sub graph of the CDG and an edge in CDG between channels, $l_{i,j}$ and $l_{j,k}$ is removed if there was no application-specific dependency between $l_{i,j}$ and $l_{j,k}$. Deadlock is inevitable when there are any cycles through ASCDG graph. A cycle in the ASCDG is a succession of application specific direct dependencies, $D = \{d_1, d_2, \cdots, d_n\}$, where $d \in D$ is a pair $(l_{i,j}, l_{j,k})$ with $l_{i,j}, l_{j,k} \in L$. If there is any cycle, we need to break it. By removing a dependency, all of the corresponding paths to that dependency will be removed. Using this method guarantees that routing algorithm is still deadlock-free. It is worth noting that using deterministic routing algorithm and efficient mapping algorithm, a few existing cycles can be easily broken.

Although the proposed methodology is topology and application agnostic, the state-of-art mapping algorithm proposed in [17] is used to map Video Object Plan Decoder (VOPD) cores onto mesh topology. We have also used two minimum-distance routing algorithm in mesh i.e. XY and YX. In XY (YX) routing algorithm, a packet is routed first in the X(Y) direction and then along the perpendicular Y(X) dimension. Because of using both algorithms together to router and reroute the packets, deadlock problem which is easily solved by described ASCDG graph should be taken into consideration.

ISBN: 978-988-19251-7-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

IV. The Proposed Fault-Tolerant Application-Specific Architecture

In the mesh-based architecture which is the simplest and most dominant topology for today's regular network on chips, each core is connected to a single router as depicted in Fig. 1. If a failure occurs in a router in this topology, the failed router cannot be used any more for routing packets and the directly connected core obviously loses its communication with the network, so the expected requirements of the mapped application are not satisfied and the whole system breaks down. As shown in Fig. 1, each router consists of five identical input/output ports and each port is a bidirectional link with a circular FIFO on its input side. In order to recover the inaccessibility of the core, a fault-tolerant architecture which each core is connected to two routers i.e. main and spare have been proposed [13] shown in Fig. 2. The spared router is used while a permanent fault is detected in the main one and in this situation; average response time of the system degrades due to rerouting phase. All essential modifications in Network Interface (NI), routers and packets were explained in [13]. The authors also supposed that fault detection is done by self testing facilities embedded in each router which is responsible for continuously testing its operation. A router can inform the neighbors about its faulty status by setting a fault_status flag. This flag is checked by the neighboring routers and cores before starting any communication with the router.

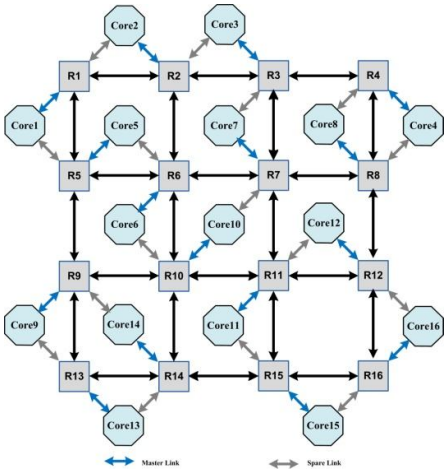

Fig.2: The proposed architecture in [13]

Adding one port to all non-edge routers in this architecture leads to a great waste of hardware. Although it is able to tolerate one permanent router failure, it does not exploit the full potential of the architecture. However, in this paper the provided path diversities between adjacent routers are used to improve performance of the system and a new component called Link Interface (LI) instead of router port is developed to reduce hardware overhead.

According to the mentioned architecture shown in Fig.2, after mapping an application onto mesh topology, an efficient spare router selection should be considered to find the best spare router for any core. To minimize the hardware cost, only one of the possible spare routers for a core is chosen [13]. On the other hand, with respect to the possible places for each core as shown in Fig. 2, there are two constraints to select a spare router.

1. Each router is limited to be linked as a spare by only one core.
2. Each core is located in neighborhood of its local and adjacent routers and all cores should be placed in different locations.

The spare router selection algorithm in [14] called FERNA results in better average response time, extra communication cost and system reliability than greedy algorithm and has a polynomial time complexity. Since both main and spare routers can be used at the same time in the developed solution, we need to modify FERNA algorithm with regards to more routing path opportunities (explained in details in Fig. 3).

```
Initialize (G (E, V));
For (All Routers)
   Router_Unused[i] =1;
Do
{
   Selected_Core=Find_Max_Comm (G (E, V));
   Available_Palces=Find_All_Available_Places (Selected_Core);
   K=1;
   For (All Neighbor Routers)
      If (Router_Unused[i] =1)
      {
         Attach (Router[i], Selected_Core (Backup_Port));
         Response_Time[k] =Calculate_Response_Time (Architecture);
         Detach (Router[i], Selected_Core (Backup_Port));
         K=K=1;
      }
   Selected_Router=Find_Best_Neighbor_Router (Response_Time []);
   If (Selected_Router_Unused_Port=True)  // Edge Routers
         {
      Attach (Router[i], Selected_core (Backup_Port));
      Router_Unused [Selected_Router] =0;
         }
   Else //Non-Edge Router
            Attach (Link_Interface, Selected_Core (Backup_Port));
   Update_Available_Places;
} While (Find Spare Router For All Cores);
```

Fig.3: The pseudo code of spare router selection algorithm

As you can see in Fig. 4, in the proposed architecture, each core is connected to its router via main local port and to the links using Link Interface via backup local port. The architecture of LI will be discussed in the following subsection.

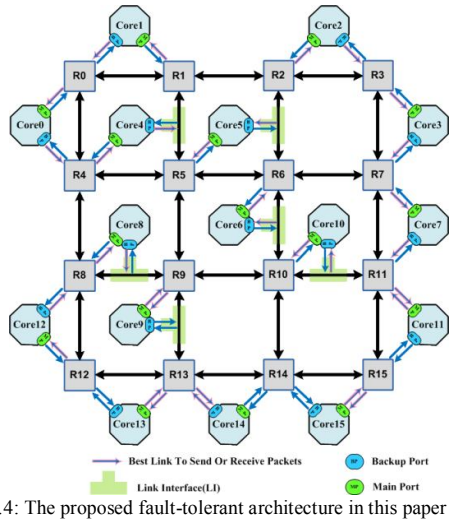

Fig.4: The proposed fault-tolerant architecture in this paper

ISBN: 978-988-19251-7-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

In this architecture, if both main and spare routers are working properly, the best (minimum-distance) paths to send and receive packets are derived from path diversities and if main (spare) is faulty, spare (main) will be responsible to transfer packets through rerouting paths. Because this architecture is supposed to recover from only single permanent failure, all the best and rerouting paths are easily found while are deadlock-free by applying the ASCGD concept. For example, the ASCDG graph has been drawn in Fig. 5 while all routers are working properly. All admissible paths are offline stored into the routing tables and used with regards to routers conditions.

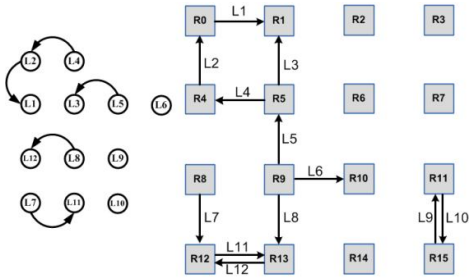

Fig.5: The ASCDG when all routers are working properly

A. *Link Interface:*

In the previous design [13], it is necessary to add one port to all non-edge routers resulting in much hardware redundancy. In order to reduce the overhead, in this section a Link Interface is suggested. After entrance of header flit into this module, destination address is decoded. As an example, if the address shows that connected core is the destination, header and its following flits will be sent to backup network interface of the core, otherwise they are routed to another output towards next router.

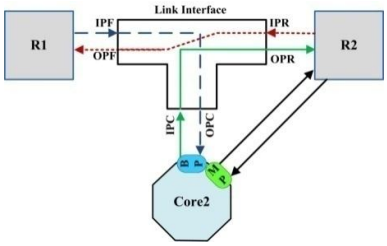

Fig.6: The proposed Link Interface

This module has been implemented with three processes which run concurrently; therefore it is able to transmit three dataflow as shown in Fig. 6. This module has been also designed without using clock pulse that leads us to achieve better response time and power consumption. To this end, as soon as data_ready line is activated; the input port will run its process of management and data control flow to guide flits towards output port. It is worth noting that if two input ports simultaneously request one output port, priority mechanism is used to tackle with this problem (Fig. 7). In order to prevent overwriting, a flag has been also considered for each output port to inform its free or busy status.

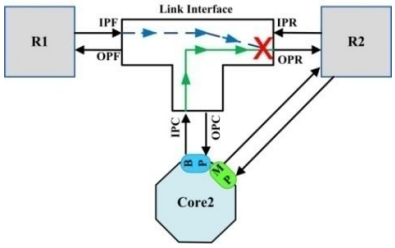

Fig.7: The possible conflict in the Link Interface

V. EXPERIMENTAL RESULTS

In order to compare the average response time and hardware cost of the reliable architecture and traditional mesh, they have been designed in VHDL and synthesized using Xilinx ISE (on FPGA – Xilinx VitexE). [14] shows the effect of mapping algorithm on system reliability, so Video Object Plan Decoder (VOPD) as a case study has been mapped on a 4x4 mesh topology using the best mapping technique proposed in [17]. For our experiments, packets are generated according to a uniform distribution with the rates that extracted from VOPD core graph. As can be seen in Fig. 8, it takes 137,265 cycles to reach all packets to the destination routers in the traditional mesh. As mentioned before, the proposed architecture is able to tolerate one router failure and guarantees the 100 percent packet delivery.

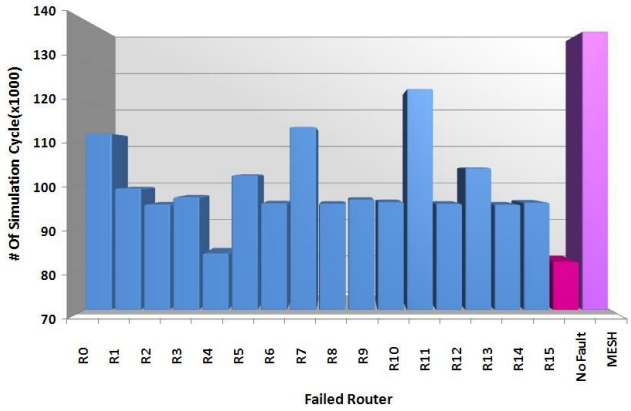

Fig.8: Average response time of system in different situations

Because it potentially is possible both main and spare routers are used to send or receive packets by each core, the proposed architecture also significantly decrease the average response time on the faultless and 16 possible faulty routers compared with the mesh architecture as illustrated in Fig. 8. It should be pointed that it actually is a great achievement to develop a fault-tolerant NoC design which also has better performance. To explain in details, when all routers are correctly operating, new architecture improves the average response time by 41% comparing to mesh. The worst observed average response time (123,377 cycles) occurs when the eleventh router fails, and in this case it also improves the response time by 10%. Conclusively, we observe that the proposed approach allows to decrease the response time of system by 27% and tolerate permanent failure of each single router (Fig. 9).

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ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

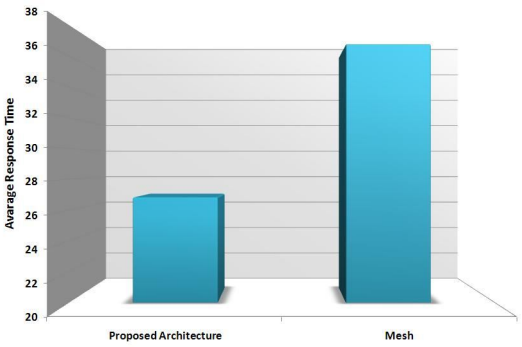

Fig.9: Comparing proposed architecture with mesh in terms of average response time (all situations are considered)

To recover from a permanent fault, hardware redundancy is mandatory and reduction of this overhead has always been an important issue in this area. In our design, we do not add any router port contrary to what [13] does and instead a link interface was developed which helps to achieve less hardware overhead. The router port and LI have been designed and implemented in the VertexE FPGA (v50ecs144-6). Synthesized results (Fig. 10) indicate that LI overhead translates to approximately 32% of router port area. Therefore, the proposed fault-tolerant architecture (with only 6 LI) introduces better overhead compared to previous work in literature.

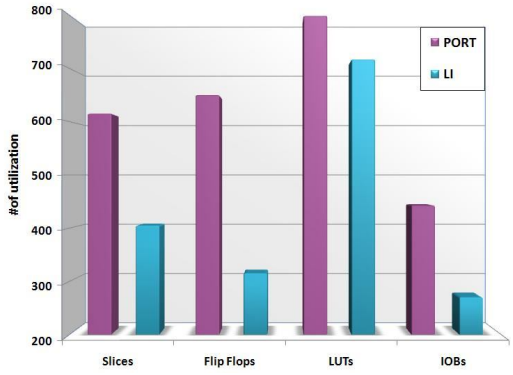

Fig.10: Hardware overhead of router port and Link Interface (LI)

VI. Conclusion

In this paper, a new fault-tolerant application-specific network-on-chip was proposed which is able to tolerate one router failure and guarantees the 100% packet delivery. Considering fault tolerance in designing forces us to accept performance degradation. However, this architecture also improves the average response time of system by 27% comparing to traditional mesh. Link Interface as a solution for reducing hardware redundancy was suggested and synthesized results demonstrated that each new router port is almost equal to three Link Interfaces in terms of hardware overhead. Although the proposed methodology is topology and application agnostic, best mapping algorithm to map Video Object Plan Decoder (VOPD) cores onto 2D mesh topology was simulated and investigated.

References

[1] L. Benini, "Application Specific NoC Design," date, vol. 1, pp.105, Proceedings of the Design Automation & Test in Europe Conference Vol. 1, 2006.

[2] Wein-Tsung Shen, Chih-Hao Chao, Yu-Kuang Lien, An-Yeu (Andy) Wu, "A New Binomial Mapping and Optimization Algorithm for Reduced-Complexity Mesh-Based On-Chip Network," nocs, pp.317-322, First International Symposium on Networks-on-Chip (NOCS'07), 2007.

[3] Atena Roshan Fekr, Majid Janidarmian, Vahhab Samadi Bokharaei and Ahmad Khademzadeh, "Yield Enhancement with a Novel Method in Design of Application-Specific Networks on Chips," Electrical Engineering and Applied Computing, Volume 90, 247-257, 2011.

[4] S. Furber, "The future of computer technology and its implications for the computer industry," Comput. J., vol. 51, no. 6, pp. 735–740,2008.

[5] Shekhar Borkar, "Designing Reliable Systems from Unreliable Components: The Challenges of Transistor Variability and Degradation," IEEE Micro, vol. 25, no. 6, pp. 10-16, Nov./Dec. 2005.

[6] Tudor Dumitraş, Radu Mărculescu, "On-Chip Stochastic Communication," date, vol. 1, pp.10790, Design, Automation and Test in Europe Conference and Exhibition (DATE'03), 2003.

[7] Premkishore Shivakumar, Michael Kistler, Stephen W. Keckler, Doug Burger, Lorenzo Alvisi, "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic," dsn, pp.389, International Conference on Dependable Systems and Networks (DSN'02), 2002.

[8] M. Ali, M. Welzl, S. Hessler, and S. Hellebrand, "An Efficient fault tolerant mechanism to deal with permanent and transient failures in a network on chip," International Journal of High Performance Systems Architecture , vol. 1, no. 2, pp. 113-123, 2007.

[9] Ville Rantala, Teijo Lehtonen, Pasi Liljeberg, Juha Plosila, " Multi Network Interface Architectures for Fault Tolerant Network-on-Chip," isscs , pp.1-4, International Symposium on Signals, Circuits and Systems, 2009.

[10] Yong Zou, Sudeep Pasricha, " NARCO: Neighbor Aware Turn Model-Based Fault Tolerant Routing for NoCs," Embedded Systems Letters, IEEE, Vol. 2, pp. 85-89, 2010.

[11] T. Dumitras, S. Kerner and R. Marculescu, "Towards on-chip fault-tolerant communication", In Proc. Asia and South Pacific Design Automation Conference, 2003.

[12] Zewen Shi, Kaidi You, Yan Ying, Bei Huang, Xiaoyang Zeng, Zhiyi Yu, " A Scalable and Fault-Tolerant Routing Algorithm for NoCs," iscas, pp.165-168, International Symposium on Circuits and , 2010.

[13] F. Refan, H. Alemzadeh, S. Safari, P. Prinetto, Z. Navabi, "Reliability in Application Specific Mesh-Based NoC Architectures, " On-Line Testing Symposium, 2008. IOLTS apos;08. 14th IEEE International, pp.207 – 212 ,Jul. 2008.

[14] Majid Janidarmian, Melika Tinati, Ahmad Khademzadeh, Maryam Ghavibazou, Atena Roshan Fekr, "Special Issue on a Fault Tolerant Network on Chip Architecture" AIP Conf. Proc., Volume 1247, pp. 191-204, 2010.

[15] M. Janidarmian, A. Khademzadeh, M. Tavanpour, "Onyx: A new heuristic bandwidth-constrained mapping of cores onto tile-based Network on Chip", IEICE Electron. Express, Vol. 6, No. 1, pp.1-7, January 2009.

[16] Majid Janidarmian, Vahhab Samadi Bokharaie, Ahmad Khademzadeh, Misagh Tavanpour, "Sorena: New on Chip Network Topology Featuring Efficient Mapping and Simple Deadlock Free Routing Algorithm," cit, pp.2290-2299, 2010 10th IEEE International Conference on Computer and Information Technology, 2010.

[17] M. Janidarmian, A. Roshan Fekr, V. Samadi Bokharaei, "Application-Specific Networks-on-Chips Design", IAENG International Journal of Computer Science, 38:1, pp16-25, 2011.

[18] M. Palesi, R.Holsmark, S.Kumar, —a methodology for design of application specific deadlock-free routing algorithms for NoC systems□, Hardware/Software Codesign and System Synthesis, CODES+ISSS '06. Proceedings of the 4th International Conference,pp. 142-147, Oct. 2006.