Low Power 8-bit 200MSPS Time-Interleaved Pipelined ADC

Song jinghui, Wang zongmin, Zhang zhuo. Zhou liang

***Abstract*—A low power 8bit 200MSPS analog-to-digital converter (ADC) is described. The prototype ADC achieves low-power consumption by time-interleaved and stage scaling technique. The pipeline stage and amplifier are designed to guarantee the PVT variation with less current. The ADC is implemented in TSMC 0.35um double-poly-triple-metal CMOS technology and achieved 47.7dB signal-to-noise and distortion (SNDR) at 200MHz with a 41MHz input frequency. The power consumption is 120mW with a 3V supply excluding the output buffer.**

***Index Terms*—** low power, pipeline, time-interleaved, stage scaling.

I. INTRODUCTION

Mobile wireless communication systems are major applications of recent analog-to-digital converters (ADCs). The high AC performance, in terms of signal-to-noise-ratio (SNR) and spurious-free-dynamic-range (SFDR), enables wider cellular coverage, more carriers, better quality and reliability. The power consumption and die area are also essential for the modern mobile wireless communication systems.

Among various ADC architectures, a pipelined ADC is suitable for high-speed, high-resolution. There is great demand for better performance with less power consumption. Opamp sharing and switched-opamp techniques are widely used to reduce the power consumption [1-3]. But such techniques only suitable for low speed design. In this paper, some techniques are approved to save the power without sacrificed performance. The ADC can operate at 200MHz with 47.7 dB SNR, and the current is only 40mA.

This paper is organized as follows. Section 2 presents the architecture of pipelined ADC. Section 3 describes the circuit implementation such as amplifier, pipeline stages, reference generator and some other circuit. Section 4 gives the final measurement.

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II. ARCHITECTURE OF PIPELINED ADC

The pipelined ADC have two channels, each one operates at 100MHz and composes five 1.5-bit stages and a 3-bit flash ADC. Traditionally, the first stage of pipelined ADC will have a large resolution, for example 3.5-bit or 4.5-bit. But in this paper, 1.5-bit is chosen. There are two reasons: firstly, the ADC is time interleaved. It have two channels, any mismatch between two channels will degrade the performance. Because there are many capacitor and switch in multi bits stage, multi bits in first stage will incur more mismatch than 1.5-bit. Secondly, the amplifier do not cost much power in a 8bit 100MHz design, so the multi bits in first stage will not save much power compare to the all 1.5-bit architecture using stage scaling technique. The architecture is shown below:

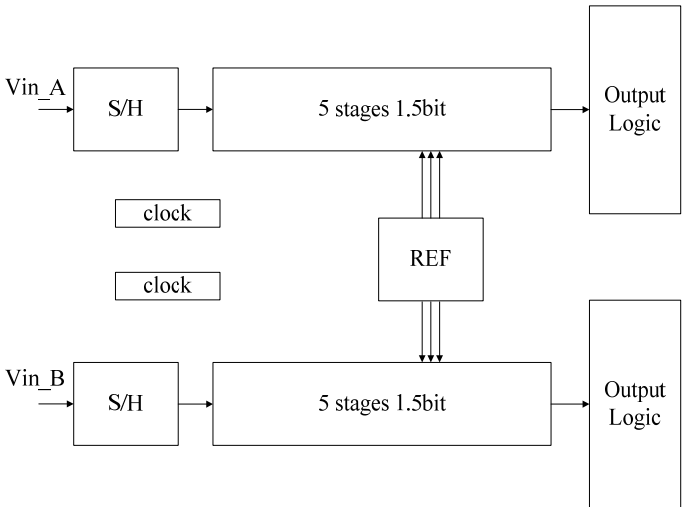

Figure 1 the architecture of pipelined ADC

There are also other circuits in the pipelined ADC such as reference generator and clock generator and so on. The reference generator circuit should satisfy the PVT variation, so careful design should be made to meet the requirement; the clock generator distributes clocks to all stages, the skew will degrade performance seriously. The driver of clocks should be designed properly; it will cost much power if the driver is too strong. There are some parasitic capacitances in the layout, so proper margin should be made to guarantee the performance.

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III. CIRCUIT IMPLEMENTATION

A. Pipeline stage

The pipeline stage can implement in 3 ways: open loop, charge transfer closed loop and capacitor flip-over closed loop [4]. The open loop way can alleviate the requirement of amplifier, but it usually need background or foreground digital correction because of serious nonlinear. In 8-bit 100MHz pipeline ADC, the amplifier is not bottle-neck, so the open-loop way is not approved. Two closed loop architectures are shown below:

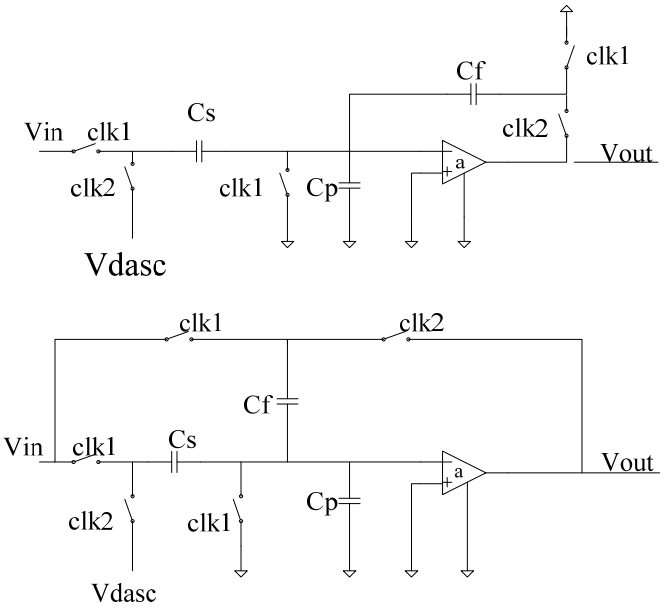


Figure 2 two architecture of MDAC

They have same function ideally, but if the capacitor mismatch is taken into consideration, they show different behavior. The charge transfer has transfer function shown below [5] (C_s/C_f=1 and all the non ideal are not take into consideration):

$$Vout = (2+\Delta)(Vin - D\cdot\frac{1}{2}Vref) \quad (1)$$

Where Vin is the input signal, Δ is capacitor mismatch, D is digital output, Vref is reference.

The capacitor flip-over has transfer function shown below:

$$Vout = (2+\Delta)Vin - (1+\Delta)D\cdot Vref \quad (2)$$

The figure below show the two transfer function at 10% mismatch (Δ=-0.1).

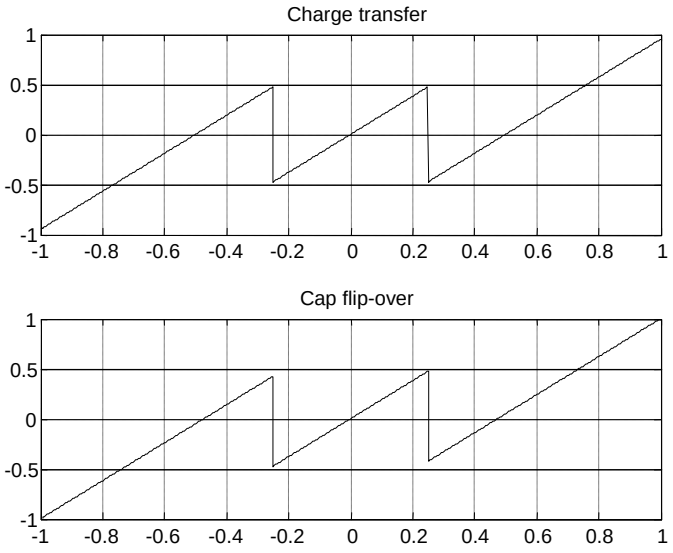
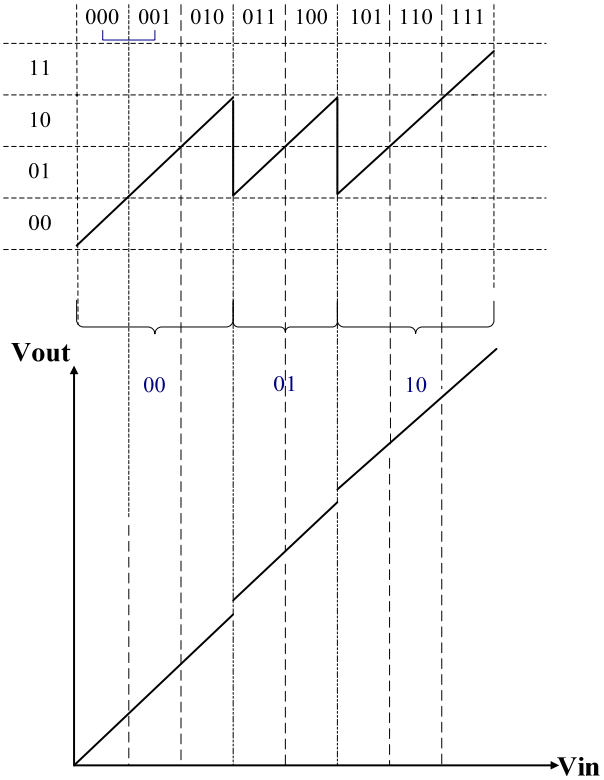


Figure 3 transfer function of MDAC (Δ=-0.1)

As the figure shown, the first and last cross point always locate at -1/2 and 1/2 in charge transfer architecture but the amplitude of the output will be affect by Δ. In cap flip-over architecture, the first and last cross point will be affect by Δ, but the amplitude of the output will not affect by Δ. The height at -1/4 and 1/4 in charge transfer architecture is more close to Vref compare to cap flip-over architecture, which are 0.95Vref and 0.9Vref. The pipeline ADC uses redundancy to make correction. If the mismatch occurs at first stage only (for example the other stages are ideal and all have 2-bit). The correction will like this:



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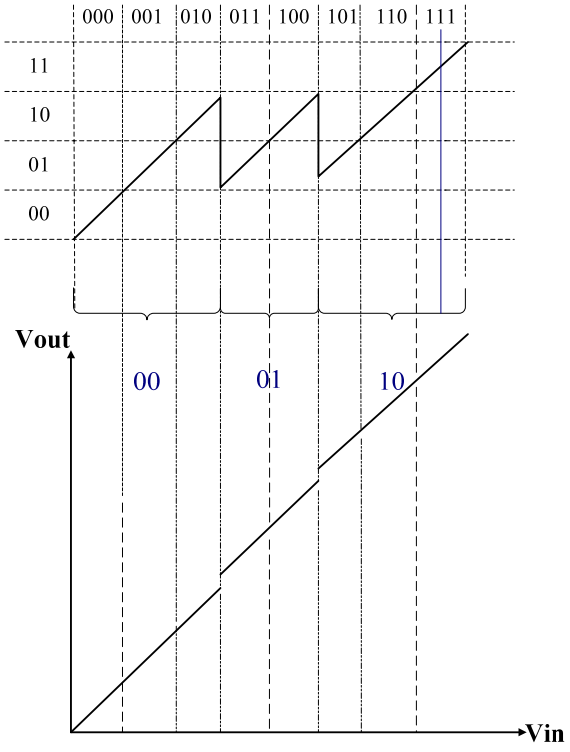

Figure 4 correction logic

(left is charge transfer architecture)

Because the cross points always locate at the -1/2 and 1/2, and the height at 1/4 or -1/4 is larger than cap flip-over architecture, the charge transfer architecture can make correction better.

When the Δ is a positive number, the charge transfer architecture will cause missing code, which is shown below ($\Delta = 0.1$):

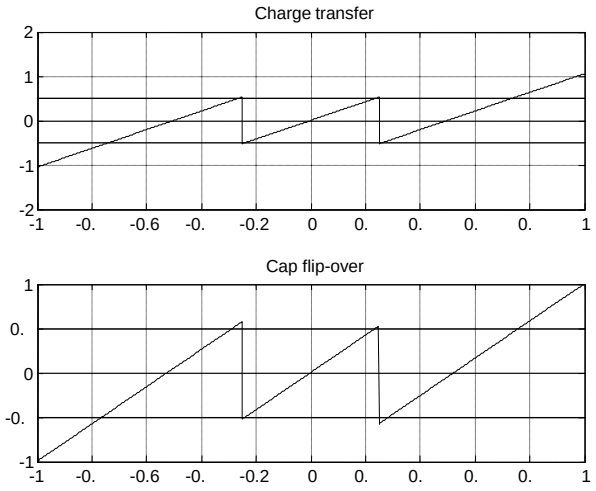

Figure 5 transfer function of MDAC (Δ =0.1)

But compare to the offset of the cross point and height in capacitor flip-over architecture, the error caused by missing code smaller than offset all the same. Here is a capacitor mismatch versus SNR using two architectures

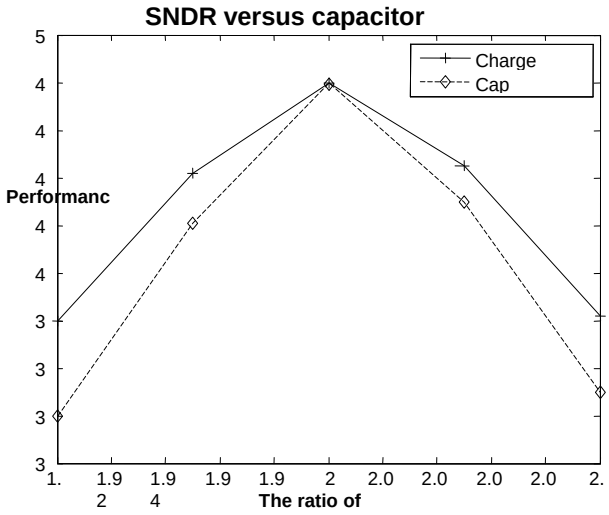

Figure 6 SNR versus capacitor mismatch (one channel)

The charge transfer architecture also has disadvantages, the most important one is smaller feedback factor which will aggravate the requirement of amplifier. But in a 8-bit 100MHZ pipelined ADC, the amplifier is not bottle-neck, and the current cost will be compensated by the performance of anti capacitor mismatch.

B. Amplifier

The amplifier used in this design is not traditional two stage architecture. The first stage is common-source; the second stage is cascode, which is shown below:

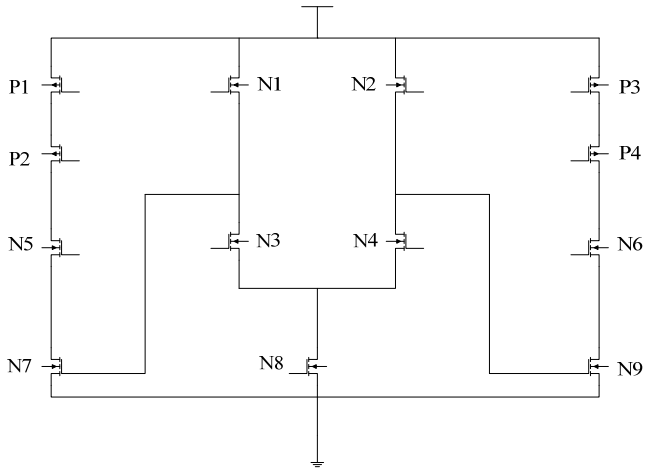

Figure 7 architecture of amplifier

This architecture has two advantages compare to the traditional two stage miller amplifier. Firstly, the gain is better than the traditional one. Because the second stage is cascode, so the output resistance is larger and the gain is also lager than traditional one. Secondly, because the second stage is output stage, so the pole at the output is dominate pole. Through carful design, the dominate pole can far away none dominate pole which is locate at the first stage. That means the miller compensation is needless, the load capacitance can be alleviate, so the larger GBW can be obtained with less current compare to traditional one. That is essential for low power design.[6-8]

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According to the calculation, the gain and GBW requirement can be obtained by the formula below:

$$A > \frac{1}{\beta} \cdot 2^{(b+1)} \tag{3}$$

$$GBW > \frac{8 \cdot fs \cdot (b+1) \cdot \ln 2}{3 \cdot \beta} \tag{4}$$

Because the target is 8-bit 100MHz, so the gain should larger than 61dB, the GBW should larger than 794MHz. The simulation result is shown below.

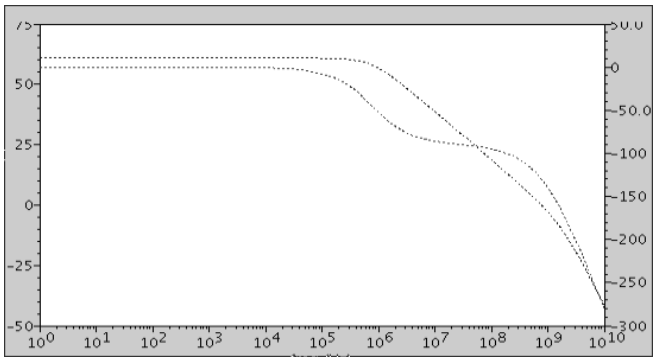

Figure 8 frequency response of amplifier

C. Reference Generator

Traditionally, a PTAT current is generate by band gap reference to be the bias current of all the analog circuit, and a low temperature coefficient voltage is generate by band gap reference to be the reference of ADC. That is reasonable, but in this design, the 8-bit 100MSPS ADC does not need a PTAT current to compensate the temperature effect, the analog circuit (such as amplifier) can work normally with a constant current even a CTAT current. The reference generation circuit is shown below:.

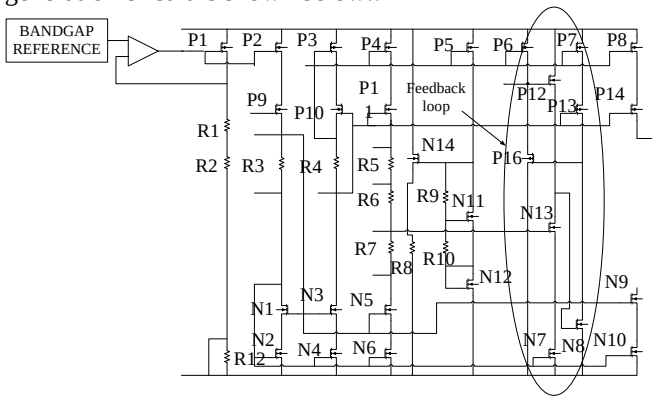

Figure 9 reference generator

Through a LDO, the low temperature coefficient voltage is transfer to a CTAT current (the resistor has positive temperature coefficient and all the resistor are all in one category). Through two groups current mirror N5, N6 and P7, P8, the CTAT current generate the references which are used in sub-ADC and sub-DAC and flash ADC. Because the resistors are all in one category, so the reference voltages are also low temperature coefficient voltage. There is a trade off in the reference generation, the current and the resistance. Because the voltage is used as the reference of ADC, so they can be treat as voltage source. Any disturbance on it, the performance of ADC will be degraded. So the large current and small resistance is chosen, that choice will cost more current but is indispensible. In the design, abundance simulation should be taken to trade off the power dissipation and the performance.

The CMFB circuit is used in amplifier, and it also needs two reference voltages. According to charge conservation, the function of CMFB can be express as below:

$$V_{fb} = V_b - V_{cm} + \frac{(out1 + out2)}{2} \tag{5}$$

Where V_{fb} is feedback voltage, V_b is reference voltage, V_{cm} is output common mode reference voltage, out1 and out2 are output voltage. Through this equation, the V_b and V_{cm} can decide output voltage. Large variation of output common mode voltage caused by the PVT variation is not acceptable, because it can serious affect the performance of amplifier, so the performance of ADC is degraded too. In this design, the V_{cm} and V_b are not generated separately, they generate together. Through a feedback loop, if V_{cm} increases V_b increases too, if V_{cm} decreases V_b decreases too. So the output common mode voltage will not variate much along with PVT variation.

D. Other Consideration

In order to save current, some power saving techniques are approved. Firstly, the stage scaling technique is used in this design. In pipelined ADC, the requirement of front stages are strict than back-end stages, because all the error introduced by back-end stages can be scaled by the gain of front-stages. So the circuits in back-end stage do not need same performance as front stages such as amplifier, switch and sample capacitor. They all can be scaled in an appropriate coefficient. Abundance simulation should be taken to trade off the performance and power dissipation. In this design, the scaling factor 3/4, 2/4, 6/16, 4/16 is chosen. Secondly, the number of switch in SH and MDAC circuit is optimized, fewer switches are used than traditional architecture, so reduce the need of driven capacity of clock. The clock generator is also design carefully, ten clocks are generated separately. Five clocks are used in even stages; five clocks are used in odd stages. The clock generator is shown below:

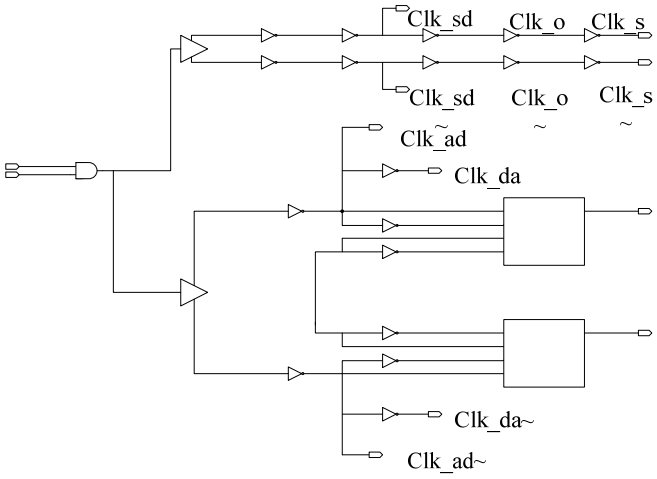

Figure 10 clock generator

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The clock_s, clock_sd, clock_o, are used in analog part, clock_ad, clock_da are used in digital part. The inverter can be design with a reasonable size, and the clock tree buffers are not need in the layout. This design consumes less current, but also need careful simulation to guarantee the performance.

IV. MEASUREMENT RESULT

The prototype ADC is implemented in 0.35-um TSMC CMOS technology and occupies a die area of 4mm^2, which include all the auxiliary circuits such as band gap reference buffer, output buffer, pad and de-couple mos capacitor. Two channels are perfect symmetric. The reference generate circuits are in the middle of layout, and the clock generators are place beside the pipeline stages. Such placements guarantee the performance.

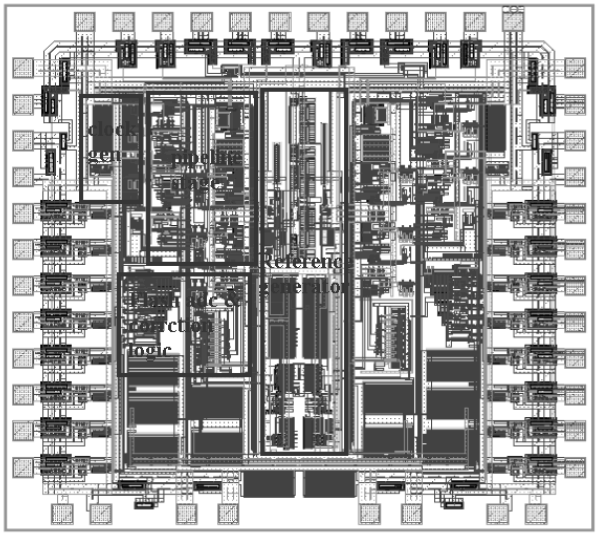
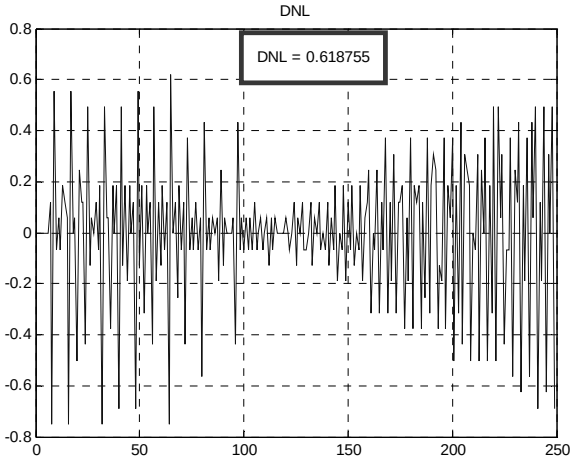


Figure 11 layout of pipelined ADC

Figure 11 is the layout. Static measurements are made first. As it is shown in figure 12, the DNL and INL are less than 0.61dB and 0.53dB, respectively. After that, the dynamic measurements are made. Figure 13 is the performance versus input and sampling frequency. The performance does not degrade for input frequency up to 41MHz and sampling frequency up to 300MHz. The total power is 40mA excluding the output buffer.



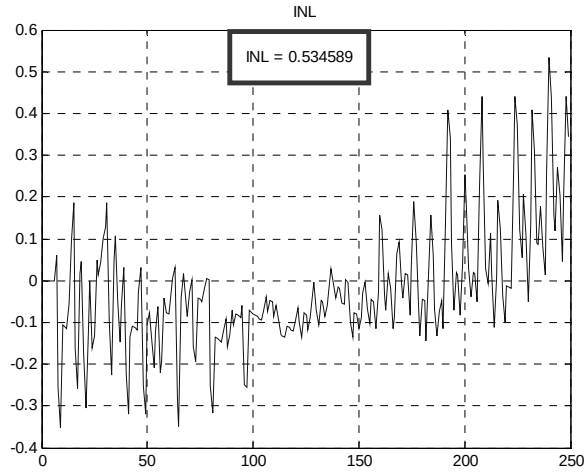
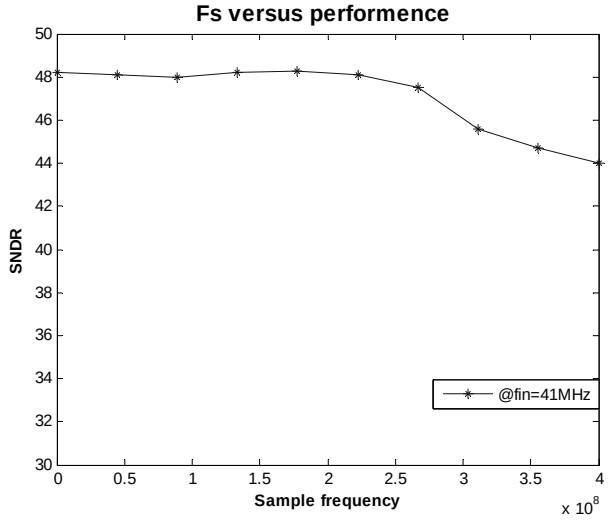


Figure 12 DNL and INL



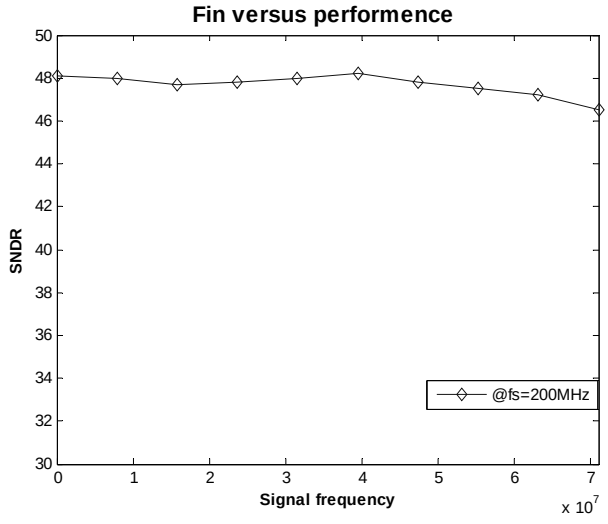


Figure 13 dynamic measurements

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V. CONCLUSION

In this paper, a 8-bit 200MHz pipelined ADC is proposed. Time-interleaved and stage scaling techniques are approved to reduce the power consumption. The pipeline stages, amplifier and reference generator are designed to guarantee the PVT variation. The ADC can operate at 200MHz with 47.7 dB SNDR, and the current is only 40mA.

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