A Current-Mode Controllable Logarithmic Function Circuit using MOSFET in Subthreshold

Munir A. AL-Absi and Karama M. Altamimi

Abstract: **—A novel CMOS current-mode controllable low-voltage and low-power logarithmic function circuit is introduced. It consists of an OTA and two PMOS transistors biased in weak inversion region. The proposed design provides high dynamic range, controllable amplitude, high accuracy and it is insensitive to temperature variation. The circuit operates from ± 0.5V power supply and consumes 110nW. The functionality of the proposed circuit was verified by simulation using HSPICE with 0.35µm CMOS process.**

***Index Terms*—weak inversion, logarithmic function, current mode**

I. Introduction

Nowadays, a significant increase in the use of CMOS technology for realization of analog circuits has been observed. Current-mode circuits received more attention than their voltage-mode counterparts. CMOS circuits with nonlinear functions will greatly enhance signal processing capabilities, such as clock recovery, waveform generation, adaptive filtering..etc. Logarithmic functions and amplifier produces an output that is proportional to the logarithm of the input. These type of circuits are used in applications that require compression of analog input data, linearization of transducers that have exponential outputs, and analog multiplication and division. Logarithmic functions are also widely used in many signal processing applications. For this purpose, a number of logarithmic function design topologies already introduced in the literature [1–7]. However, all these realizations have at least one of the following drawbacks:

- Absence of low voltage operation capability [2, 3, 6]
- Limited dynamic range [3, 4],
- Employment of BJT transistors [2, 3, 6],
- Doesn't enjoy Current-Mode [1, 3, 5, 6],
- Realize a logarithmic function for input equal to or greater than unity [3, 4, 6, 7],
- Temperature dependent [2, 3],
- Relatively high power consumption [6, 7],
- No gain controllability [3, 4, 5, 6],
- To some extent, linearity error is high [5, 6, 7],
- Use passive elements i.e. resistors [2, 3, 4, 6],
- Complexity [6, 7].

In this paper, we propose a compact current-mode CMOS logarithmic circuit capable of performing the logarithmic of normalized input signal greater than zero. Simulation results are also presented to verify the theoretical analysis.

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II. Proposed Circuit

The proposed design concept is shown in Fig 1. It consists of an Operational Transconductance Amplifier (OTA) and two PMOS transistors, M5 and M6 biased in weak inversion region.

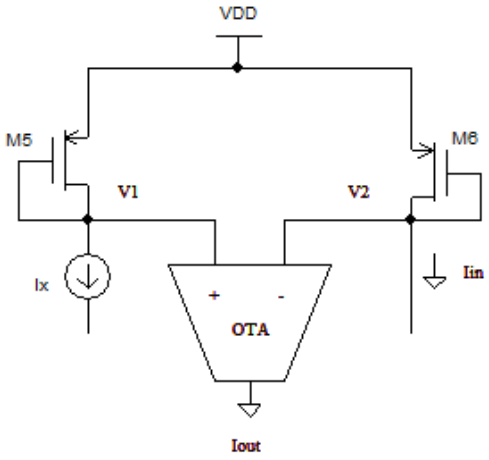

Fig. 1 Proposed logarithmic circuit

It is well known the output current of the OTA is given by:

$$I_{out} = g_m(V_1 - V_2) \quad (1)$$

where g_m is the transconductance of the MOSFET pair used in the OTA, V_1 and V_2 are the OTA's two input voltages. For the MOSFET to work in weak inversion forward saturation, the following two conditions must be satisfied [8]:

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$$V_D - V_S \geq 3V_t \text{ for nMOS},$$
$$V_S - V_D \geq 3V_t \text{ for pMOS} \quad \text{and}$$
$$I_D < 2n\frac{KW}{L}V_t^2$$

Transistors M5 and M6 are biased in weak inversion region and are used to convert currents I_x and I_{in} to voltages $V_1$and V_2 respectively in logarithmic form as shown in equations (2) and (3) respectively:

$$V_1 = V_{DD} - V_{sg5} = V_{DD} - nU_T \ln\left(\frac{I_x}{I_{Do}}\right) \quad (2)$$

$$V_2 = V_{DD} - V_{sg6} = V_{DD} - nU_T \ln\left(\frac{I_{in}}{I_{Do}}\right) \quad (3)$$

Where, V_{DD} is the supply voltage, V_{sg} is the source-to-gate voltage, $U_T = \frac{KT}{q}$ is the thermal voltage, n is the slope factor and I_{Do} is the leakage current of the MOSFET.
Combining equations (2) and (3) yields:

$$\left[\frac{(V_1 - V_2)}{nU_T}\right] = \ln\left(\frac{I_{in}}{I_x}\right) \quad (4)$$

Combining (4) and (1), one can easily get the output current I_{out} expressed by:

$$I_{out} = g_m nU_T \ln\left(\frac{I_{in}}{I_x}\right) \quad (5)$$

The complete circuit diagram of the proposed design is shown in Fig 2. Transistors M1-M4 forms the OTA.

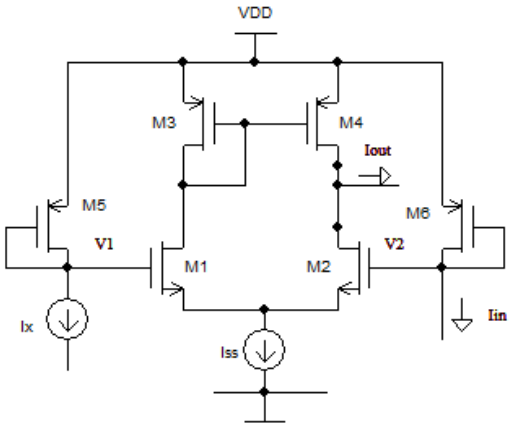

Fig. 2 The complete circuit diagram

The transconductance g_m of the transistor in weak inversion region is given by:

$$g_m = \frac{I_D}{nU_T} \quad (6)$$

Where, I_D is the drain current of MOSFETs M1 and M2 and is given by:

$$I_D = \frac{I_{ss}}{2} \quad (7)$$

From (5) and (6) the output current can be written as:

$$I_{out} = I_D \ln\left(\frac{I_{in}}{I_x}\right) \quad (8)$$

With reference to equation (8), if the current I_x is fixed, the output current I_{out} is proportional to the logarithm of the input current I_{in}. The amplitude of the output current can be controlled by the varying the current I_D of the OTA.

III. Simulation Results

The functionality of the proposed circuit was carried out using HSPICE level 49 in 0.35µm CMOS technology. The simulation results are shown in Fig3 for $I_{ss} = 100$nA (i.e.$I_D = 50$nA),and VDD = -VSS=0.5V. It is evident from Fig 3 that the simulated results are in excellent agreement with the calculated values. The input dynamic range is 300nA and the maximum linearity error is 2% at 300nA below this value , the linearity error is 0.01%. The circuit was simulated for controllability by varying the bias current ID, for $I_D = 40, 45$ and 50 nA. The simulation result for different bias current is shown in Fig 3.
The circuit was simulated against temperature variation for three different values of temperature, namely 20, 25 and 30 °C. Simulation result is shown in Fig 5. It is clear from the figure that the proposed design is temperature insensitive

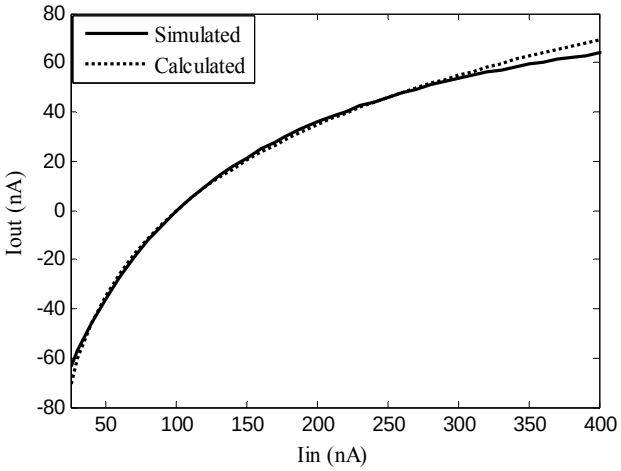

Fig. 3 DC transfer characteristics of logarithmic

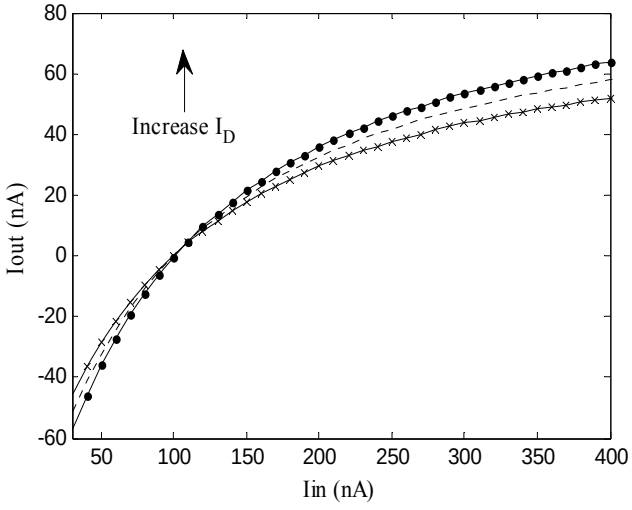

Fig. 4 Output current with different values of I_D

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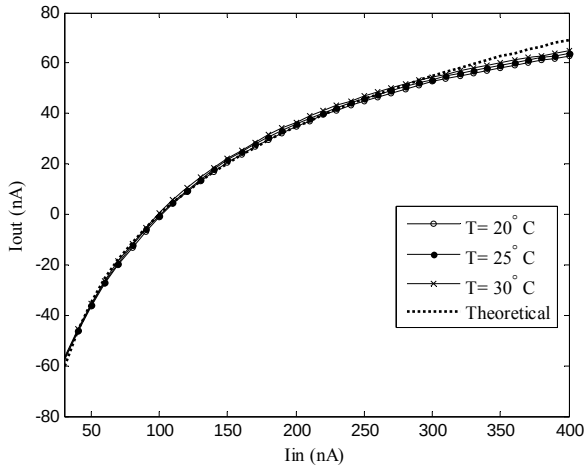

Fig. 5 Output current for different temperatures

IV. Conclusion

A novel CMOS current-mode logarithmic function circuit was developed. The circuit enjoys highly accurate logarithmic function for any value of I_{in} greater than zero. The design has a controllable gain and is temperature insensitive. The performance of the proposed logarithmic circuit was verified using HSPICE 0.35µm CMOS process. The circuit consumes around 110 nW and has a linearity error of .01%.

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