Metaheuristics Based CMOS Two-Stage Comparator Optimization

Revna Acar Vural, Ufuk Bozkurt and Tulay Yildirim

Abstract—**This paper investigates nature-inspired metaheuristics for optimized sizing of a CMOS comparator with PMOS input driver. The aim is to minimize MOS transistor area using two nature-inspired metaheuristics, differential evolution and harmony search. Simulation results demonstrate that design specifications are closely met and required functionalities are accommodated in short computational time while area optimization criterion is satisfied.**

Index Terms—**constrained optimization, analog integrated circuits, automated design, transistor sizing, metaheuristics**

I. Introduction

TOGETHER with the increase in integrated circuit (IC) complexity, the design and optimization complexity of analog integrated circuits has increased drastically [1]. Even, the design of an analog circuit consists of a few transistors may be more challenging than designing a fairly complex digital circuit. This is mainly due to the lack of predefined libraries of analog standard cells contrary to digital systems [2]. Moreover, characterization of complex tradeoffs between nonlinear objectives while satisfying required specifications and constraints makes analog circuit design a long and tedious process [3,4].

Transistor sizing is a constrained optimization problem and resides between topology selection and actual circuit layout of analog design problem. Considering CMOS IC sizing process, several relations should be hold between width/length ratio of MOS transistors to ensure that constraints and specifications are satisfied. Besides, design parameters such as MOS dimension ratios should be adjusted in order to meet optimization objectives. These complicated and time consuming processes should be automated with high accuracy in a reasonable operation time which requires efficient optimization methods.

Heuristics are proposed to solve high dimensional problems with many criteria. They can be adapted to suit specific problem requirements [5, 6, 7]. Heuristics can be divided into two classes: on the one hand, there are algorithms which are specific to a given problem and, on the other hand, there are generic algorithms, i.e., metaheuristics [8]. Metaheuristics designate a computational method that optimizes a problem by iteratively trying to improve a candidate solution with regard to a given measure of quality. Notable examples of metaheuristics include genetic algorithm (GA), simulated annealing (SA), particle swarm optimization (PSO), genetic programming (GP), ant colony optimization (ACO), differential evolution (DE) and harmony search (HS). A detailed investigation of metaheuristics based analog circuit sizing is reviewed in [9,10].

Much research work has been devoted to metaheuristics based transistor sizing of basic analog building blocks such as operational amplifiers [2-4,11-18], differential amplifiers [3,19] and operational transconductance amplifiers [20-24]. This is mainly due to the fact that they are at the heart of many interface circuit, in particular digital-to-analog converters (DAC), analog-to-digital converters (ADC) and filters. An efficient design of optimal basic analog blocks is thus a cornerstone of a design environment for many applications.

Among those researches, PSO is used for CMOS transistor area minimization of a two-stage operational amplifier [3,4] and maximizing both gain and unity gain bandwidth of a complementary folded cascade operational amplifier [11]. In [12], SA is combined with gm/ID characteristics and ACM MOSFET model for both area and power minimization of a two- stage Miller operational amplifier. A heuristic method is proposed for area optimization of a telescopic cascade amplifier and two-stage operational amplifier [2,13]. ACO is utilized for minimization of both area and power consumption of a two-stage operational amplifier [14]. Competitive co-evolutionary DE method is proposed to minimize power consumption in operational amplifiers [15]. DE method is also used for operational transconductance amplifier (OTA) sizing considering power minimization and gain maximization in [20]. In [21], together with DE, HS is applied to automated sizing of folded cascode OTA. A very detailed operational amplifier synthesis method based on GP is given in [16]. GP is also proposed for minimizing power consumption in different OTA structures [22,23]. GA is probably the most widely used metaheuristics in automation of analog IC transistor sizing. Noise minimization [17] and gain maximization [17,18] objectives of a two-stage operational amplifier are accomplished with GA method. Power consumption of a differential amplifier is minimized using GA based transistor sizing in [19]. In [20], results obtained with DE are compared to that of canonical nondominated sorting GA (NSGA-II). NSGA-II based sizing

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methodology proves its efficiency in optimization of Miller OTA by minimizing power consumption and maximizing gain.

Different from abovementioned studies, this work focuses on optimal sizing of a CMOS comparator with metaheuristics based synthesis methodology. Here, MOS transistor area is aimed to be minimized in short computation time while satisfying design specifications and design constraints. Section II describes metaheuristics used in this study. Design procedure of CMOS comparator is given in section III. Following, simulation results of proposed methods are provided in section IV. Finally, section V concludes with a discussion of metaheuristics based design results and suggests possible extensions.

II. Metaheuristics

Metaheuristics are iterative in nature and may move to not necessarily improving solutions which avoids being stuck at local minima [5,6,25]. DE and HS are two nature inspired metaheuristics used for CMOS comparator sizing. Details of those are provided in the following subsections.

A. Differential Evolution

DE is a real coded population-based optimization method based on parallel direct search method and diverges from GA by adding the weighted difference between two chromosomes to the third in order to generate new ones [26].

DE uses a population P having NP individuals that evolves over G generations to reach the optimal solution. Each individual X is a vector that features a dimension size of D. Each vector in population matrix is assigned follows.

$$X_j=X_{jmin}+\eta_j(X_{jmax}-X_{jmin}),\ \ j= 1,\ldots,D \tag{1}$$

where X_{jmax}, X_{jmin} are the upper, lower bounds, respectively and η_j is a uniformly distributed random number within [0,1] of the j^{th} feature. The optimization process in DE is carried out using three basic operators; mutation, crossover and selection. The mutation operator generates mutant vectors (X') as in (2).

$$X_i'(G) = X_a(G)+F(X_b(G) - X_c(G)),\ a\neq b\neq c\neq I \tag{2}$$

where X_a, X_b and X_c are randomly selected vectors among population matrix including NP different vectors. F is the scaling constant used to improve algorithm convergence. The crossover operation is employed to create trial vectors (X'') by mixing the individuals of the mutant vectors (X') with the target vector (X) according to (3).

$$X_{i,j}^{''(G)} = \begin{cases} X_{i,j}^{'(G)}, if\ (\eta_j^{'} \le CR) or (j = q) \\ X_{i,j}^{(G)}, otherwise \end{cases} \tag{3}$$

where q is a randomly chosen index within [1,NP], guaranteeing that trail vector employs at least one individual from the mutant vector. CR is the crossover constant within [0,1] that controls the population diversity. Finally selection operator compares the fitness values of trial vectors and target vectors. If trial vectors yield better fitness values then they replace the target vectors with which they were compared, otherwise predetermined population member is retained. The above procedure restarts until the chromosomes have been successfully updated to improve their fitness values to a specified value [26, 27].

B. Harmony Search

HS is a metaheuristics method based on the improvisation process of jazz musicians [28]. HS searches an optimal combination of inputs by usage of harmony memory, pitch adjusting and randomization just as musicians seek a fantastic harmony by playing any known tune from their memory, playing a similar tune or composing new and random notes.

Initial population structure of HS is very similar to that of DE as explained in the previous subsection. Here, the total number of individuals is equal to harmony memory size (*HMS*) and individuals are stored in harmony memory (*HM*). Following, a new solution is improvised according to harmony memory considering rate (*HMCR*). A stored value is chosen from *HM* with probability of *HCMR* ($0\le HCMR\le 1$) and *1-HCMR* is the probability of generating it randomly. If the solution is picked from *HM*, it is mutated according to the pitch adjust rate ($0\le PAR\le 1$). After *HM* is updated the fitness values are evaluated. If the improvised solution yields a better fitness than that of the worst member in *HM*, it replaces the worst one. Otherwise the improvised one is eliminated. The above procedure is repeated until a preset termination criterion (maximum iterations or a target fitness value) is met [21, 28].

III. Design Procedure for CMOS Comparator

A comparator is a device that compares two voltages or currents and switches its output to indicate which is larger. They are commonly used in analog-to-digital converters (ADCs), data transmission, switching power regulators, and many other applications [29,30].

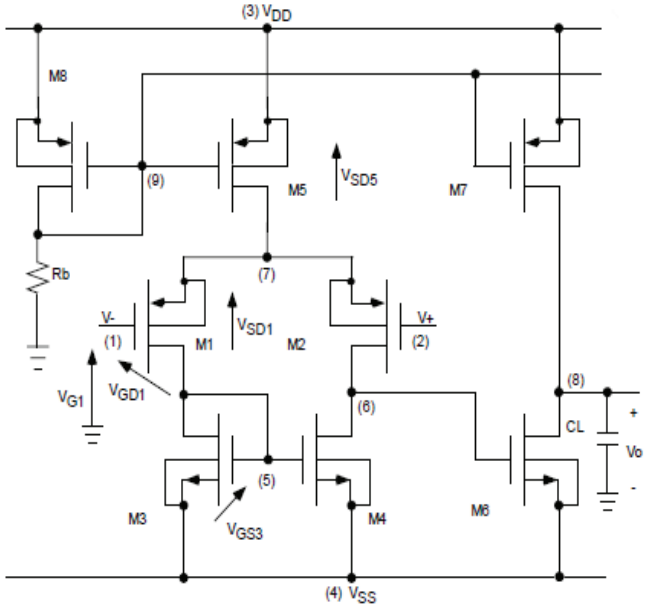

Fig. 1. Comparator with PMOS input driver [29]

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The problem considered here is the optimal selection of CMOS transistor dimensions for comparator with PMOS input driver (Fig.1), which is only a part of a complete analog circuit CAD tool. It can be characterized by a number of specifications as given below.

- Common Mode Rejection Ratio (CMRR)
- Slew Rate (SR)
- Power Dissipation (Pdiss)
- Small Signal Characteristics (Av, f-3dB)
- Input Common Mode Range (ICMR)
- Power Supply Rejection Ratio (PSRR)

These performance metrics as well as design objective(s) have to be formulated in terms of the design variables. Here, design objective which can be defined as CF is the minimization of the occupied MOS transistor area as in (4).

$$\mathrm{CF} = \sum_{i=1}^{T} \left(W_{(i)} x L_{(i)} \right) \tag{4}$$

Providing limits for design constraints of small-signal differential voltage gain (A_v), cutoff frequency (f_{-3dB}), maximum and minimum input common mode voltages ($V_{IC(max)}$, $V_{IC(min)}$), slew rate (SR), power dissipation (P_{diss}) and design variables of external resistor (R_b) and MOS device sizes, general design procedure can be summarized below [30].

• Determine the current drive requirement of $(W/L)_7$ to satisfy the SR specification.

$$I_{D7} = C_L \left(\frac{dV}{dt} \right) = C_L (SR) \tag{5}$$

• Determine the size of $(W/L)_6$ and $(W/L)_7$ to satisfy the output-voltage swing requirement.

$$(W/L)_6 = \frac{2I_{DS6}}{K_P \left(V_{DS6(SAT)} \right)^2} \tag{6}$$

$$(W/L)_7 = \frac{2I_{DS7}}{K_P \left(V_{DS7(SAT)} \right)^2} \tag{7}$$

• Calculate the gain of the second stage.

$$A_{V2} = -\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}} \right) \tag{8}$$

• Calculate the gain of the first stage to satisfy the overall gain.

$$A_V = A_{V1} A_{V2} \geq 10000 \tag{9}$$

• Determine the first stage biasing current using the minimum allowable size of 1

• Consider $(W/L)_4$ and $(W/L)_6$; using the minimum size for $(W/L)_4$, determine the current I_{SD4} that mirror with $(W/L)_6$.

$$I_{DS4} = \frac{(W/L)_4}{(W/L)_6} I_{DS6} \tag{10}$$

$$I_{SD5} = 2I_{DS4} \tag{11}$$

• Consider $(W/L)_5$ and $(W/L)_7$; using the minimum size for $(W/L)_5$, determine the current I_{DS5} that mirror with $(W/L)_7$.

$$I_{SD5} = \frac{(W/L)_5}{(W/L)_7} I_{SD7} \tag{12}$$

$$I_{DS4} = I_{SD5}/2 = I_{DS3} \tag{13}$$

$$I_{SD2} = I_{SD1} = I_{SD5}/2 \tag{14}$$

• Select the larger of the two I_{SD4} and adjust the size of $(W/L)_4$ if necessary.

• Determine the size of $(W/L)_1$ to satisfy the gain requirement. The minimum size of $(W/L)_5$ can be adjusted to satisfy the positive ICMR.

$$(W/L)_1 = \frac{[A_{V1} I_{SD1} (\lambda_N + \lambda_P)]^2}{2K_P I_{SD1}} \tag{15}$$

$$V_{SD5(SAT)} = V_{DD} - V_{G1(\max)} - \sqrt{\frac{2I_{SD1}}{K_P (W/L)_1}} - |V_{T1}| \tag{16}$$

$$(W/L)_5 = \frac{2I_{SD5}}{K_P \left(V_{DS5(SAT)} \right)^2} \tag{17}$$

• Select the larger of the two, $(W/L)_5$ and adjust the size of $(W/L)_7$ for proper mirroring with $(W/L)_5$. The size of $(W/L)_3$ or $(W/L)_4$ can be adjusted to meet the negative input CMR.

$$(W/L)_7 = \frac{I_7}{I_5} (W/L)_5 \tag{18}$$

$$(W/L)_3 = \frac{2I_{DS3}}{K_P \left(V_{G1(\min)} - V_{SS} - V_{T3} + |V_{T1}| \right)^2} \tag{19}$$

• Select the larger of the two $(W/L)_3$.

• Determine the size of $(W/L)_8$ to provide as the main current mirror for the comparator.

$$(W/L)_8 = \frac{2I_{SD8}}{K_P \left(V_{SG8} - V_{TP} \right)^2} \tag{20}$$

• The external resistor R_b connected between V_{G8} and ground must be chosen to provide the required current for $(W/L)_8$.

$$R_b = \frac{V_{G8} - 0}{I_{DS8}} \tag{21}$$

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IV. Simulation Results

In this work, by establishing design parameters and specifications to metaheuristics, the optimal sizing is aimed to be automated by DE and HS. The aim is to minimize total MOS transistor area while satisfying design specifications and design parameter constraints.

First of all, a certain range is determined for both design specifications and design parameters by human designer. The inputs to the DE and HS based design schemes are those abovementioned ranges for each design parameter and specification as well as preferential technology parameters and supply voltage values. Metaheuristics should minimize given CF and obtain design criteria and design parameter values for the given range which provides minimum CF value.

Considering CMOS comparator, DE and HS are utilized for design specifications of V_{DD}=2.5V, V_{SS}=-2.5V, A_V>10000, -1.65V<ICMR<1.65V, P_{diss}<1000µW and SR>10V/us considering an output capacitance of 10pF. Simulations are carried out using TSMC 0.35µm technology parameters. In order to minimize the channel modulation effect, all MOSFET length values are chosen as 2µm. Target value of CF is aimed to be smaller than 500µm2.

Design scheme is implemented with the relationships that describe design specifications to solve for DC currents and dimension ratios of all MOS transistors. Algorithms are constructed using MATLAB R2008a. Here, cost function evaluation and design parameter/specification range control are processed in separate procedural loops. Thereby, updates will not be carried out unless specified ranges are satisfied and better CF values are obtained. Instead of using penalty functions we choose that kind of a "fail" strategy. Flowchart of metaheuristics based design scheme is provided in Fig. 2.

DE based comparator design is concluded in 0.469 s which is approximately ten times faster compared to HS based design method. Computational performance and algorithm parameters of each method are given in Table I.

TABLE I
Comparison of Computational Performance

	DE	HS
Time	0.469 s	4.641 s
Iterations	21	2000
	NP : 10	HMS: 6
Parameters	CR : 1.0	HMCR: 0.9
	F : 0.85	PAR: 0.4-0.9

Design variables obtained with DE and HS methods are tabulated in Table II. Total MOS transistor area and resistor values obtained with both methods are approximately same. Area and resistor value obtained with HS is slightly smaller than the ones obtained with DE. However, DE based design achieves a better ICMR than HS based method.

In order to validate metaheuristics based design is satisfying desired specifications comparator with PMOS input driver is redesigned using the resulting design parameters (Table II) in SPICE simulator. SPICE simulations (Figs 3-8) demonstrate that DE and HS based designs not only satisfy all specifications but also minimize total MOS area as given in Table III. Simulations are run on Intel Core 2 Duo CPU, T7300 @ 2.00GHz.

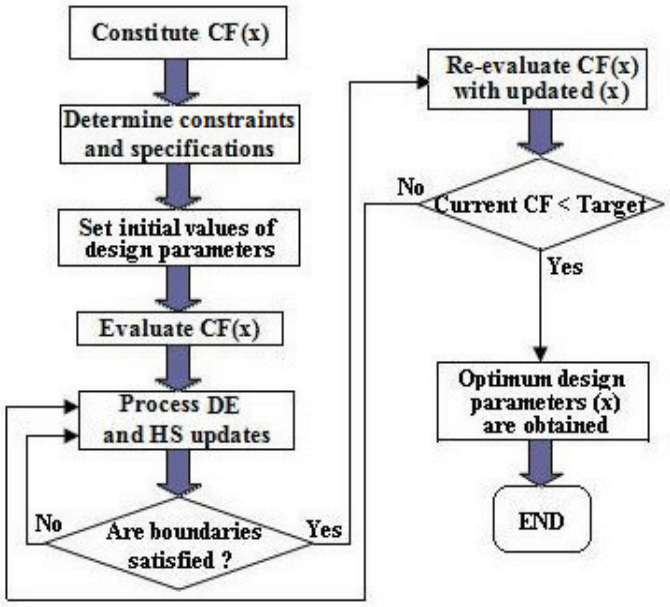

Fig. 2. Flowchart of metaheuristics based design scheme

TABLE II
Design Variables Obtained With MEtaheuristics

Comparator Design Parameters	DE	HS
W1/L1, W2/L2 (µm/µm)	20.057/2	24.230/2
W3/L3, W4/L4 (µm/µm)	2/2	2/2
W5/L5 (µm/µm)	6.899/2	6.386/2
W6/L6 (µm/µm)	58.396/2	58.182/2
W7/L7 (µm/µm)	100.72/2	92.894/2
W8/L8 (µm/µm)	20.071/2	18.579/2
Rb (kΩ)	68.383	67.827

TABLE III
Comparison of DE and HS by Means of Design Criteria

Comparator Design Criteria	Specifications	DE	HS
Slew Rate (V/µs)	≥ 10	160	160
Power Dissipation (µW)	≤ 1000	511	508
Unity Gain Bandwidth (MHz)	≥10	16.055	17.255
Gain (dB)	> 80	82.424	82.932
Vic_{min} (V)	≥ -1.65	-1.6042	-1.6146
Vic_{max} (V)	≤ 1.65	1.6458	1.5938
CMRR (dB)	> 85	87.4715	87.8223
Propagation Delay (us)	< 2	1.165	1.111
Total Area ($x10^{-10}$ m^2)	**<5**	4.60	4.57

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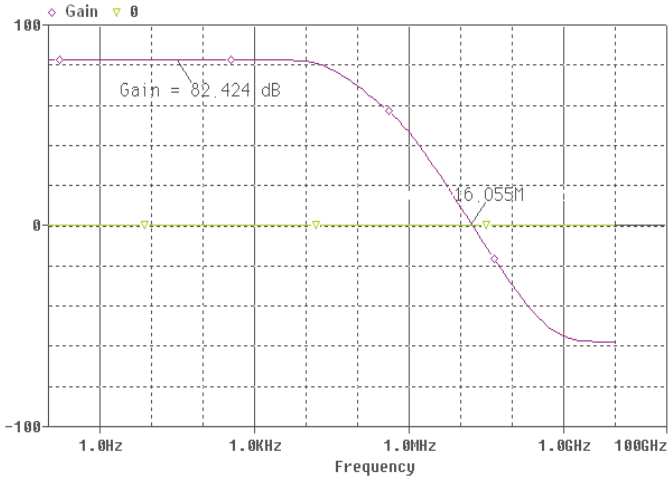

Fig. 3. Gain of DE based comparator design

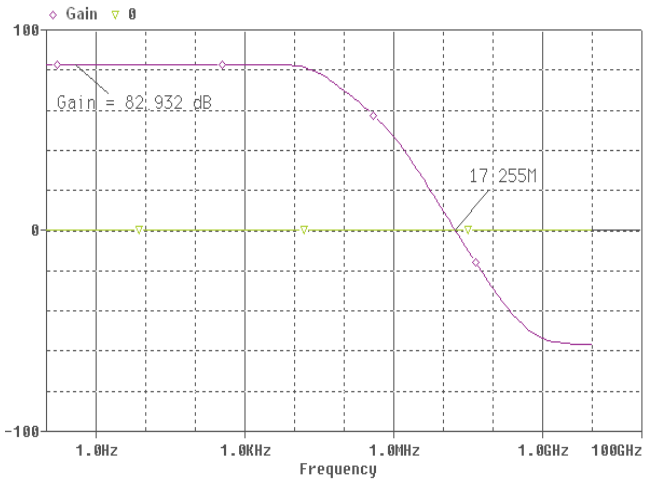

Fig. 6. Gain of HS based comparator design

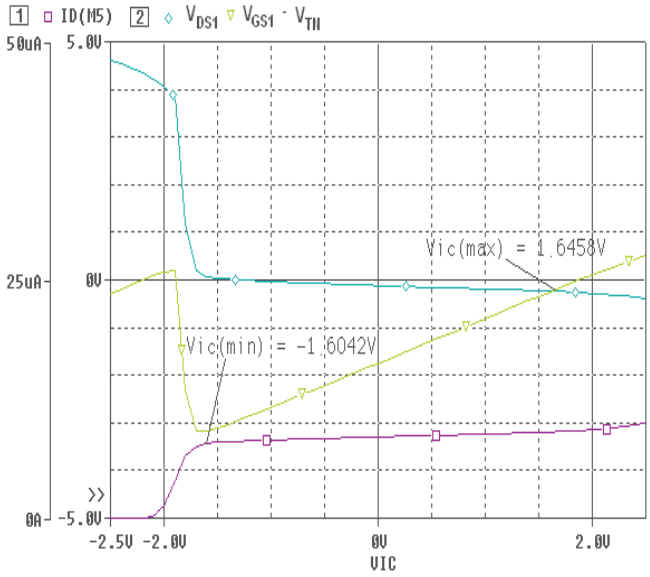

Fig. 4. ICMR of DE based comparator design

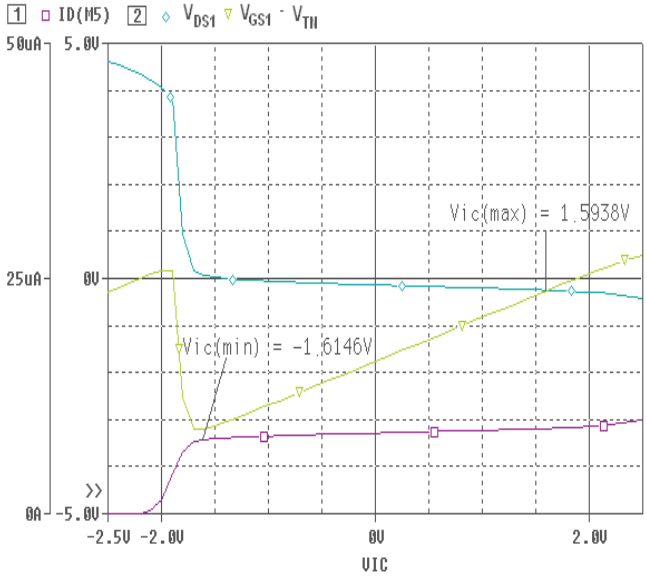

Fig. 7. ICMR of HS based comparator design

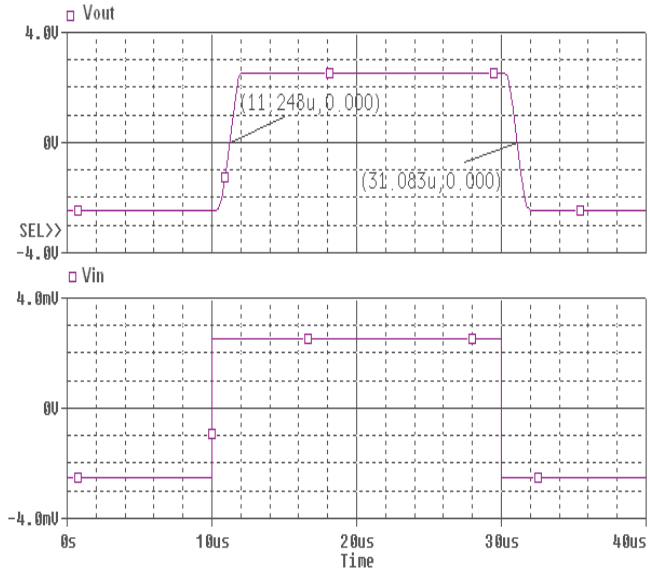

Fig. 5. Propagation delay of DE based comparator design

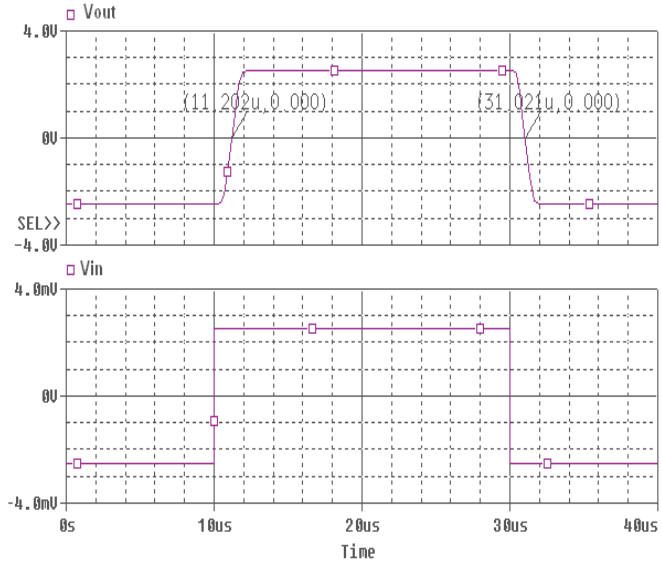

Fig. 8. Propagation delay of HS based comparator design

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V. Conclusion

The problem considered here is the optimal selection of MOS transistor sizes of a comparator structure considering area minimization as the design objective. In addition, particular specifications are aimed to be met by adjusting design variables such as device sizes and resistor. In order to automate those design tasks, metaheuristics are proposed. Simulations demonstrate that DE based design requires very few iterations and is ten times faster than HS. Resulting design variables are utilized for redesign in SPICE simulator in order to validate the exact values of design specifications obtained with metaheuristics. Simulation results proved that DE and HS based design meets all design specifications and also minimizes total MOS area. As further work, performance of other heuristic methods could be investigated by utilizing EKV modeling in analog sizing issues.

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